

US00D570307S

(12) **United States Design Patent** (10) **Patent No.:** **US D570,307 S**
Kobayashi et al. (45) **Date of Patent:** **** Jun. 3, 2008**

(54) **PORTION OF A PRINTED CIRCUIT BOARD**

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(73) Assignee: **Kabushiki Kaisha Toshiba** (JP)

(**) Term: **14 Years**

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(22) Filed: **May 8, 2007**

(30) **Foreign Application Priority Data**

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(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/180**

(58) **Field of Classification Search** D13/180;
29/829; 361/720, 749, 760, 776, 820; 174/250,
174/253, 255

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a portion of a printed circuit board, as shown and described.

DESCRIPTION

FIG. 1 is a front, bottom and right side perspective view of a portion of a printed circuit board, showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a top plan view thereof;

FIG. 5 is a bottom plan view thereof;

FIG. 6 is a right side elevational view thereof;

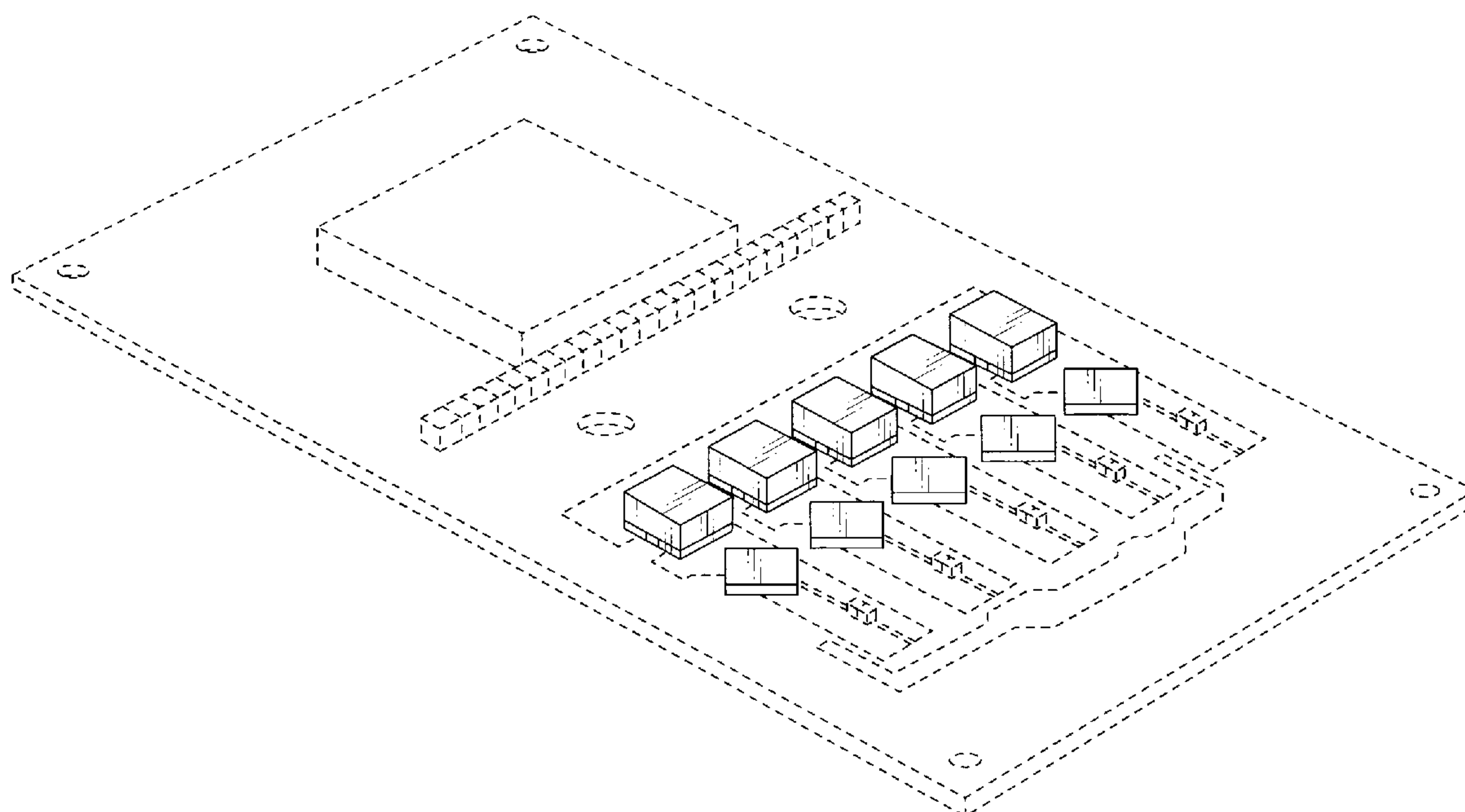
FIG. 7 is a left side elevational view thereof;

FIG. 8 is an enlarged view thereof showing the portion marked with 8—8 in FIG. 6; and,

FIG. 9 is an enlarged view thereof showing the portion marked with 9—9 in FIG. 5.

The broken lines are for illustrative purposes only and form no part of the claimed design.

1 Claim, 6 Drawing Sheets



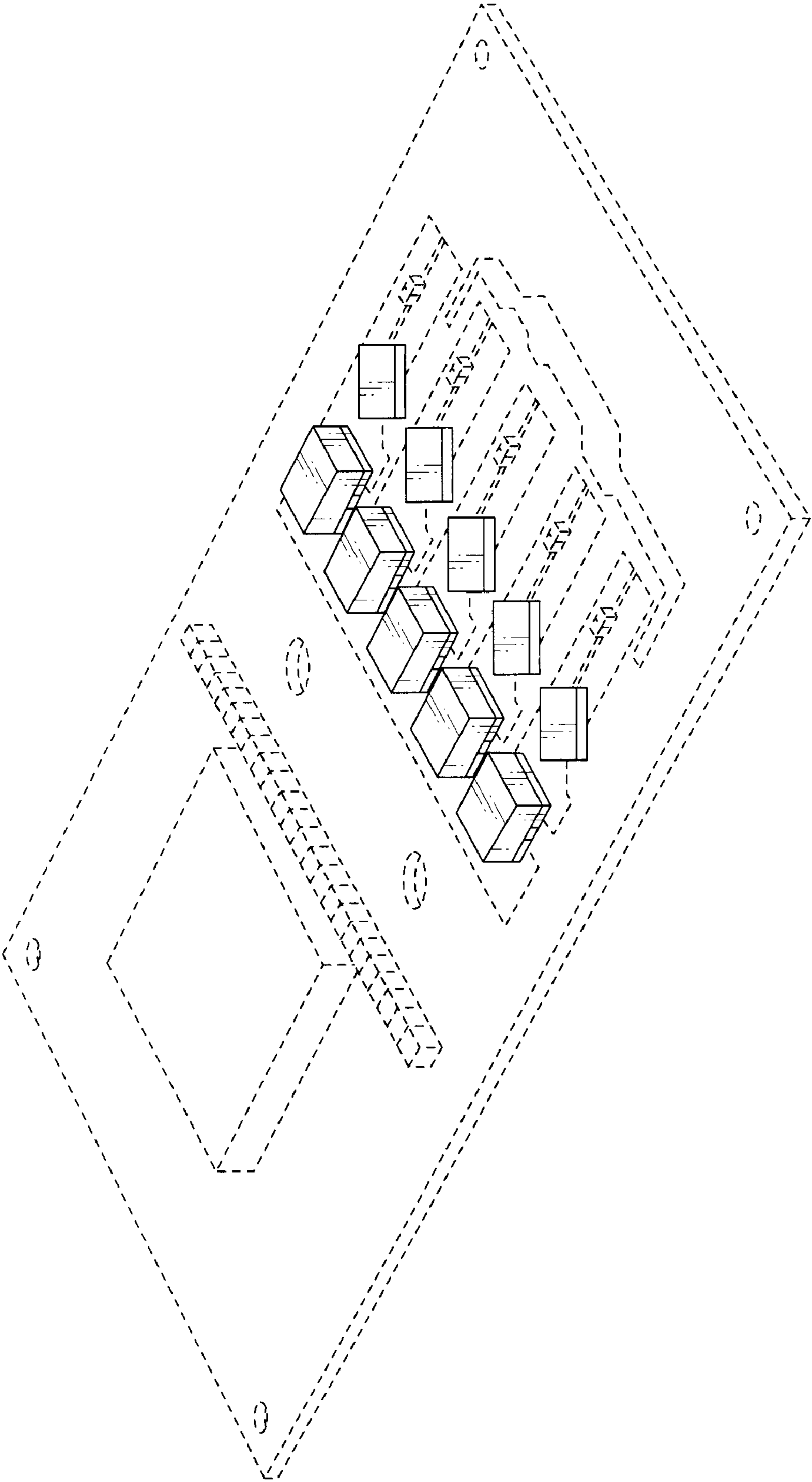


FIG. 1

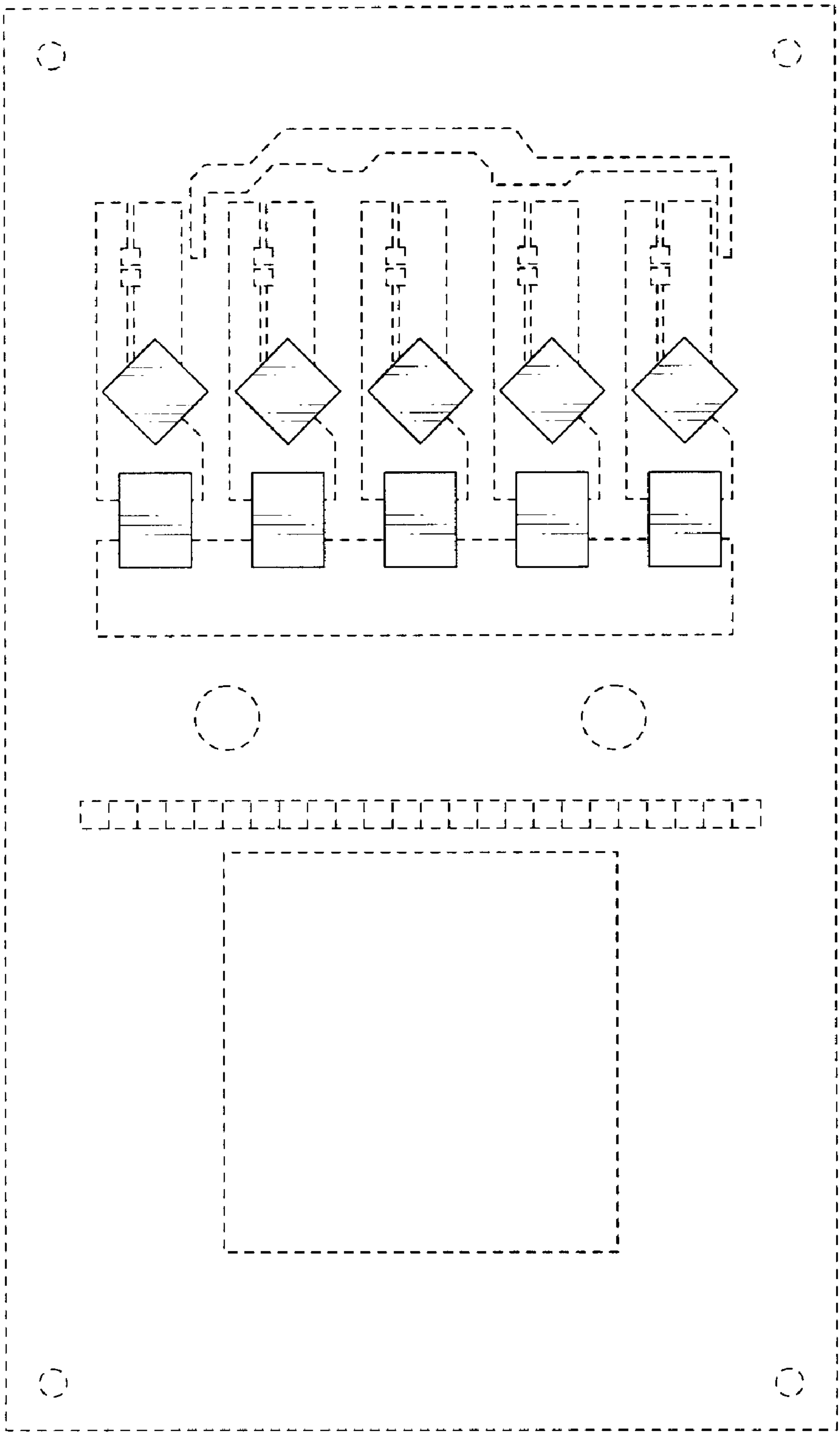


FIG. 2

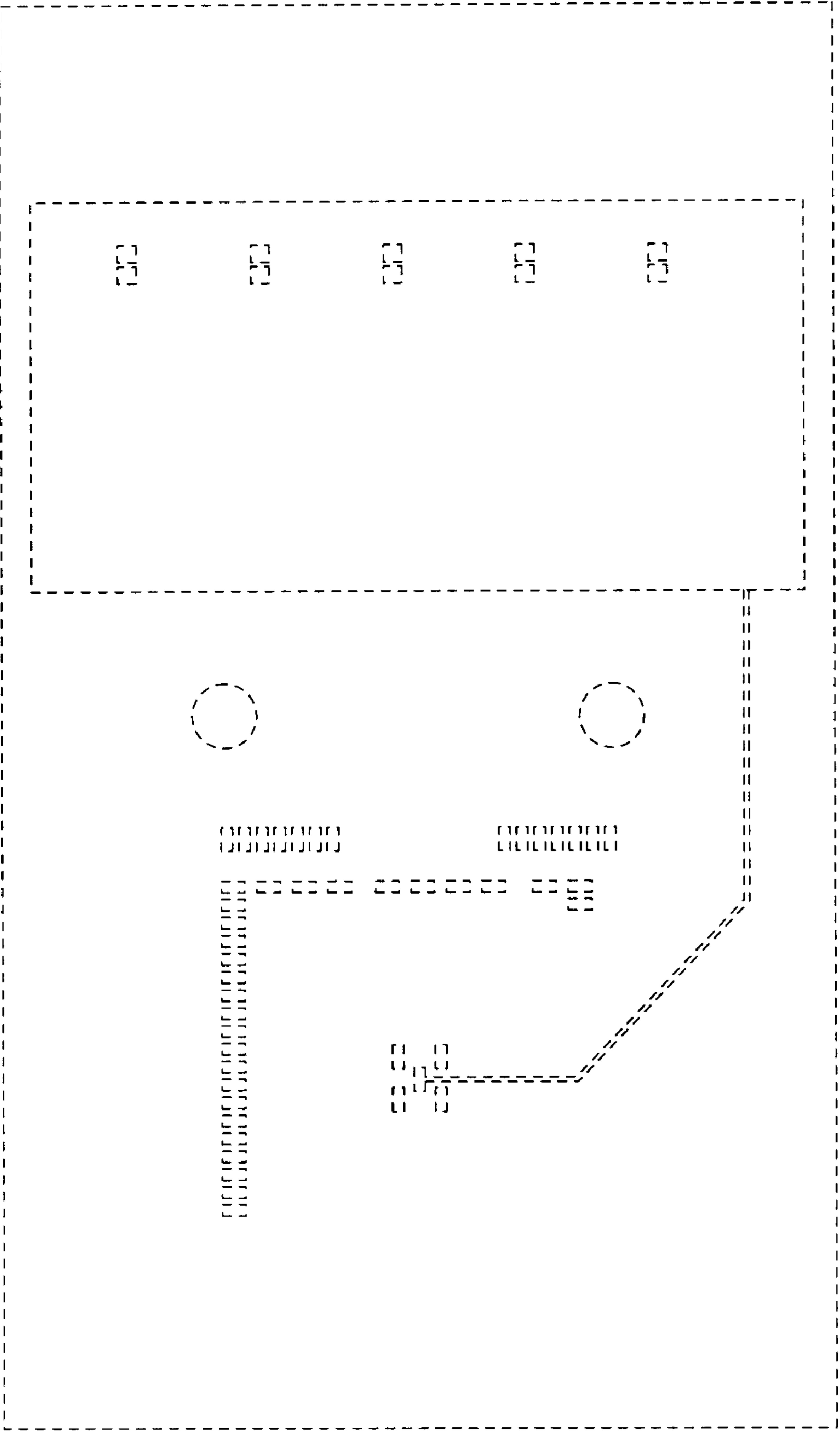


FIG. 3

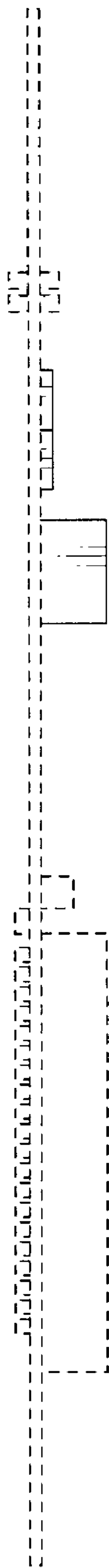


FIG. 4

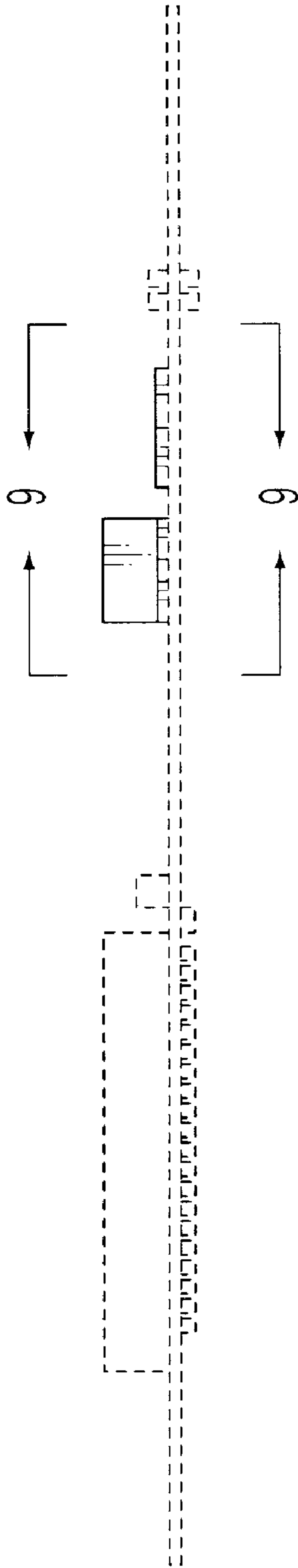


FIG. 5

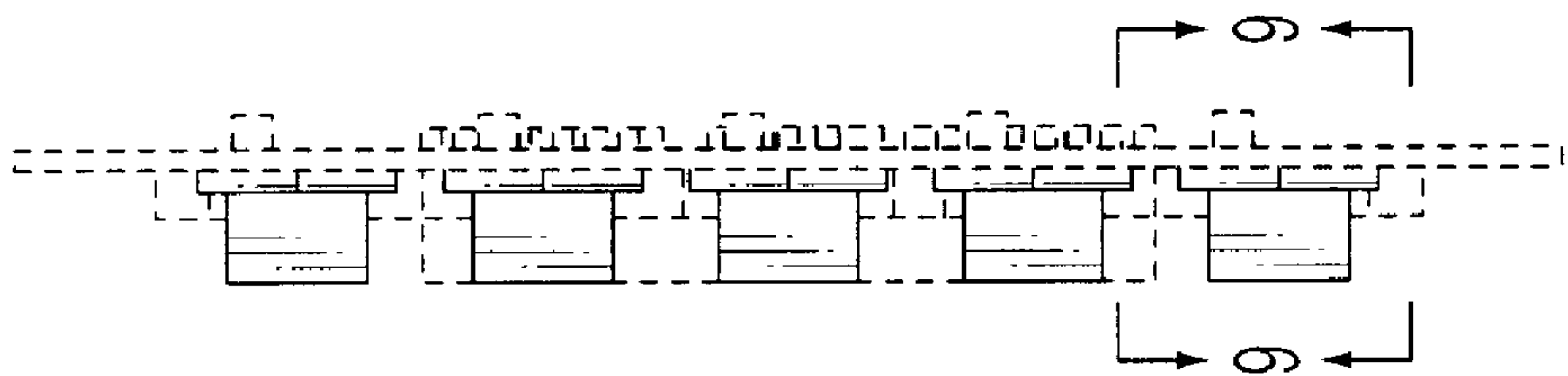


FIG. 7



FIG. 6

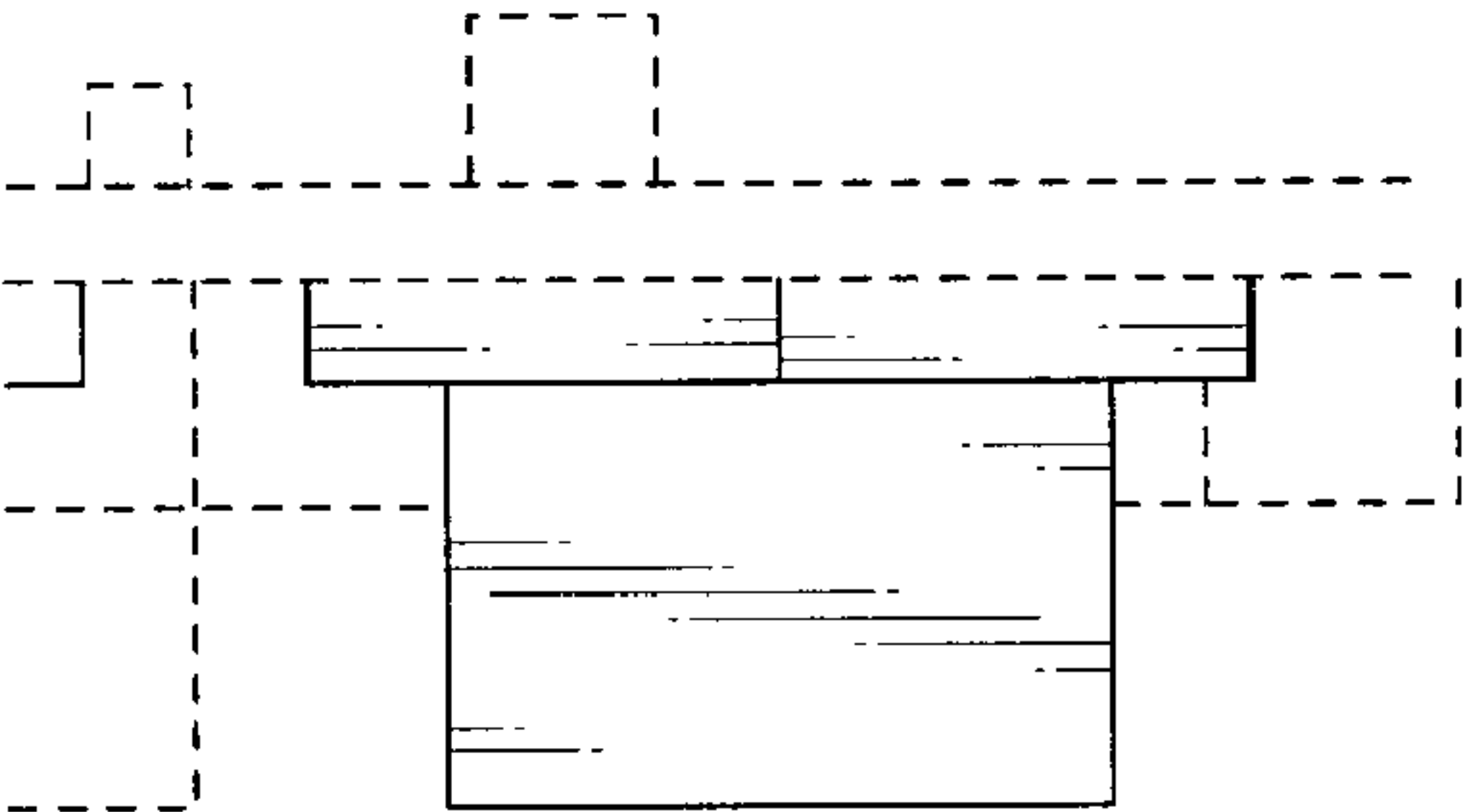


FIG. 8

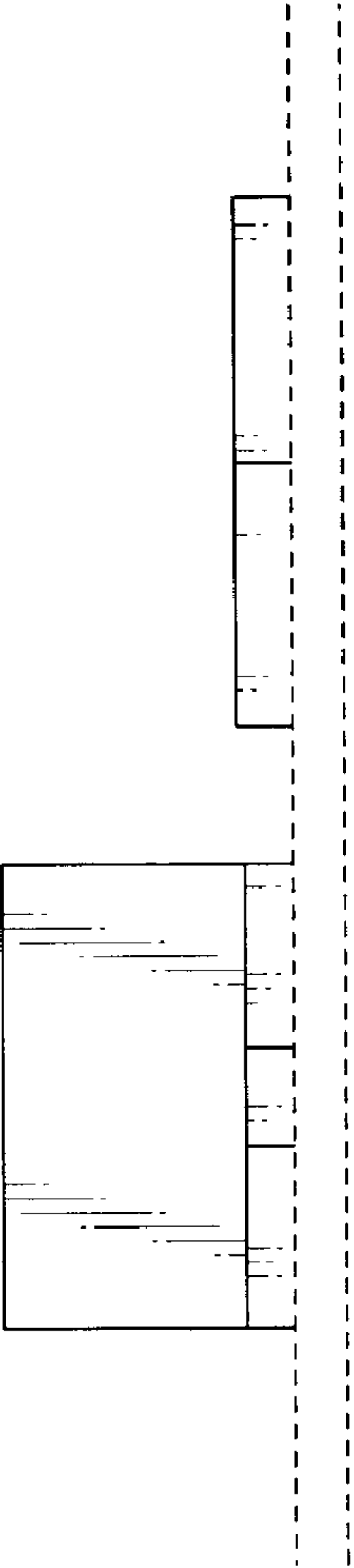


FIG. 9