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(12) **United States Design Patent**  
**Yoshida et al.**

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(54) **CHIP-TYPE SOLID STATE ELECTROLYTIC CAPACITOR**

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(\*\*) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (8) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/125**

(58) **Field of Classification Search** ..... D13/118,  
D13/123-125, 133, 184, 199; 320/2; 361/523,  
361/535, 536, 538, 539, 540, 271, 277, 301.1,  
361/328-330, 763; 429/178

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a chip-type solid state electrolytic capacitor, as shown and described.

**DESCRIPTION**

FIG. 1 is a front, bottom and right side perspective view of a chip-type solid state electrolytic capacitor showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a left side elevational view thereof;

FIG. 5 is a right side elevational view thereof;

FIG. 6 is a top plan view thereof; and,

FIG. 7 is a bottom plan view thereof.

**1 Claim, 4 Drawing Sheets**

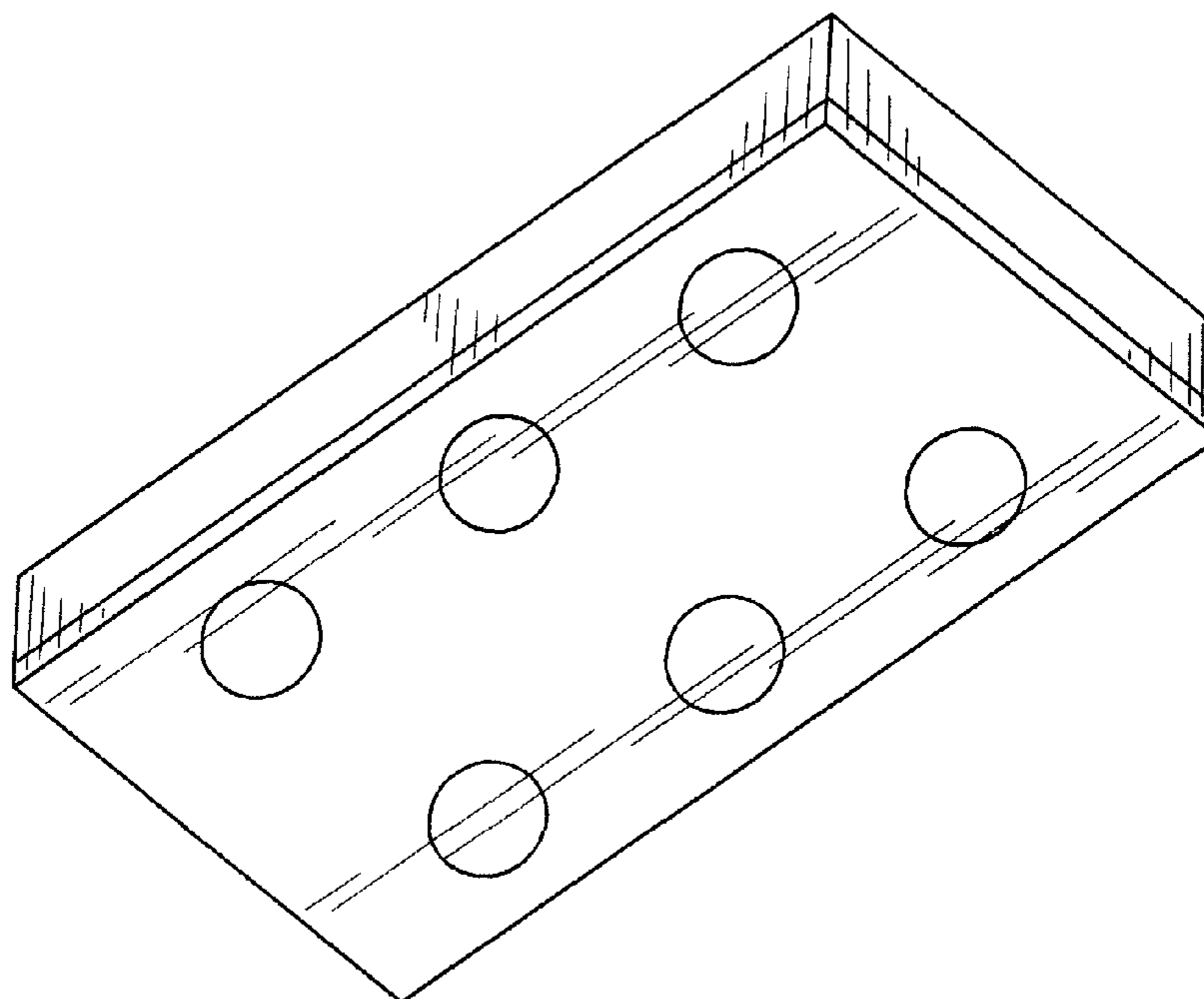


Fig. 1

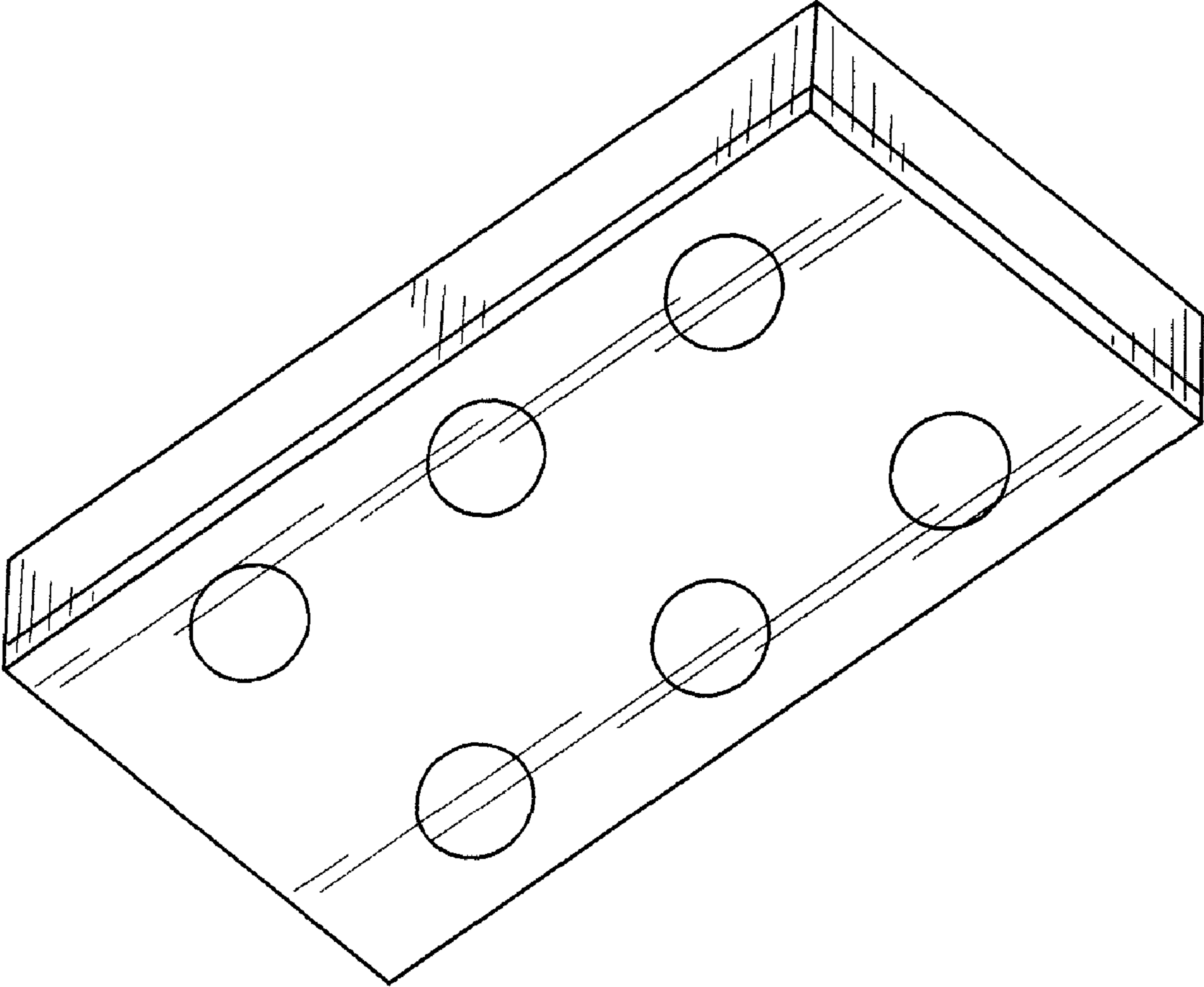


Fig.2

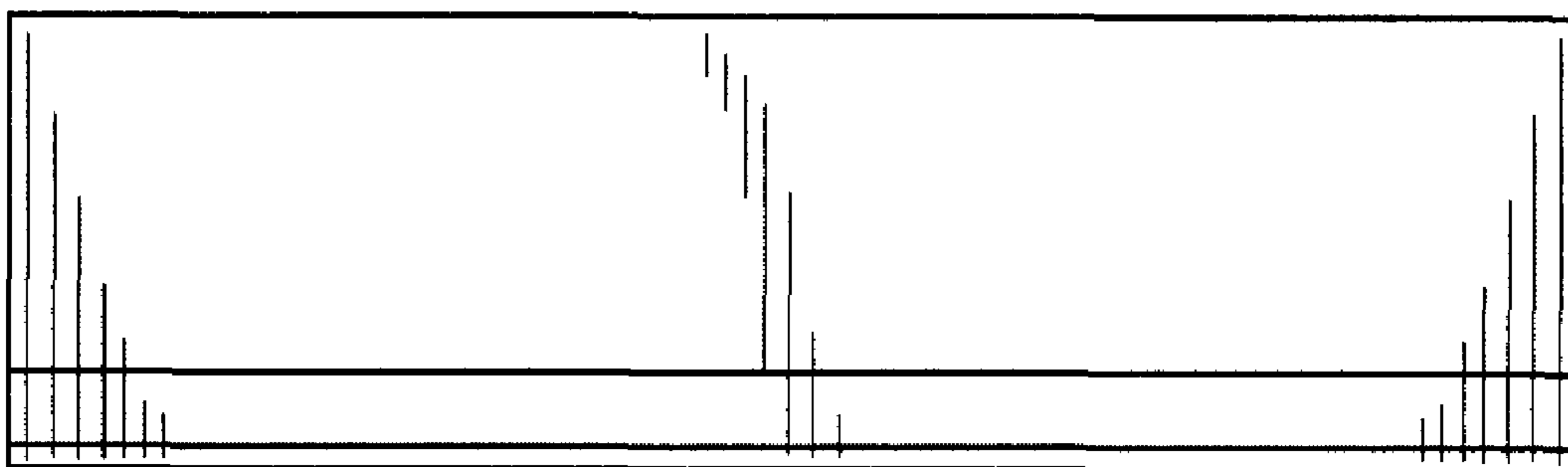


Fig.3

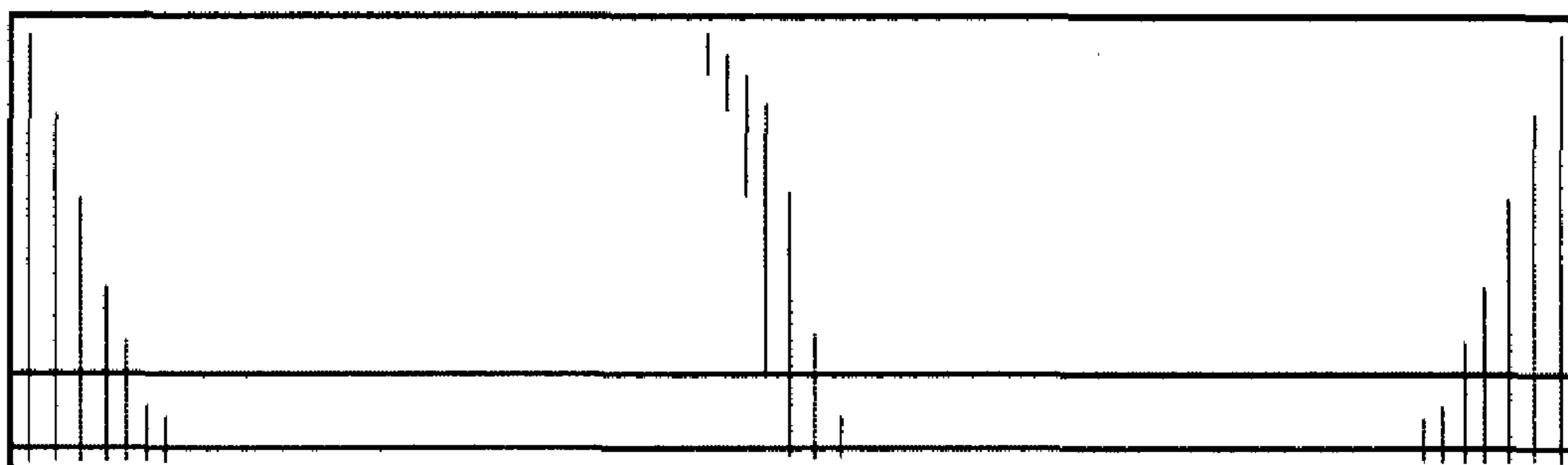


Fig.4

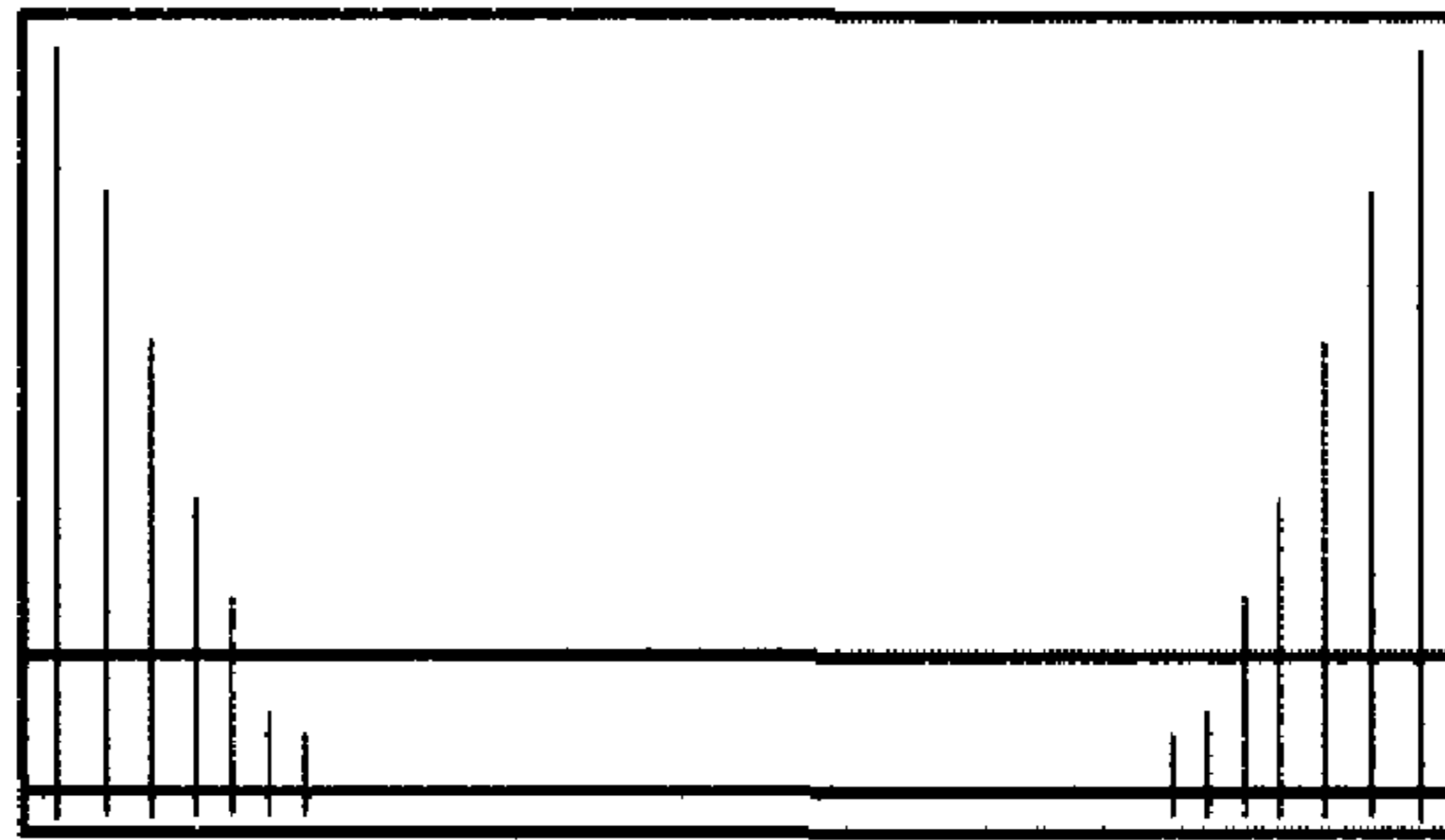


Fig.5

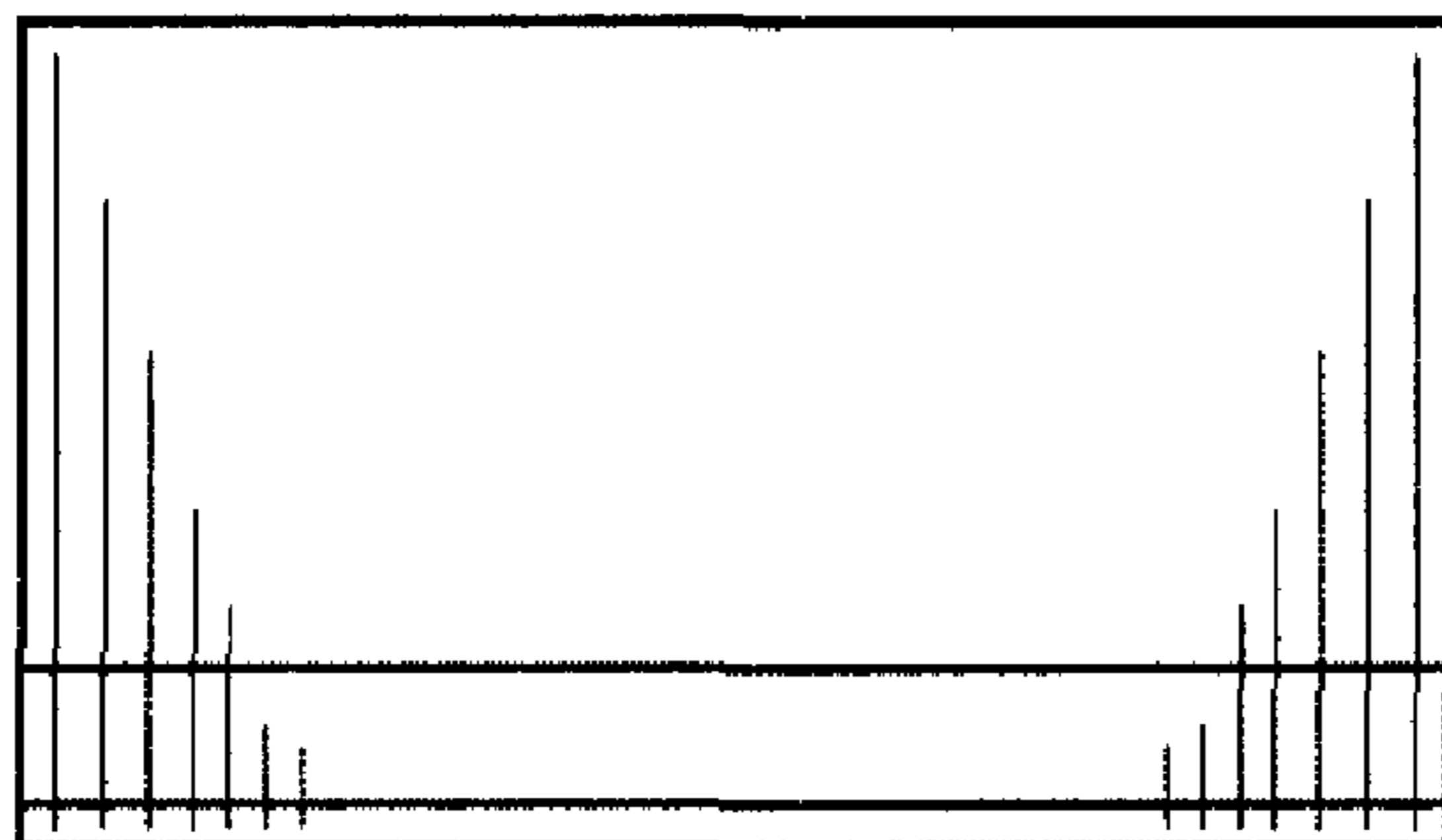


Fig.6

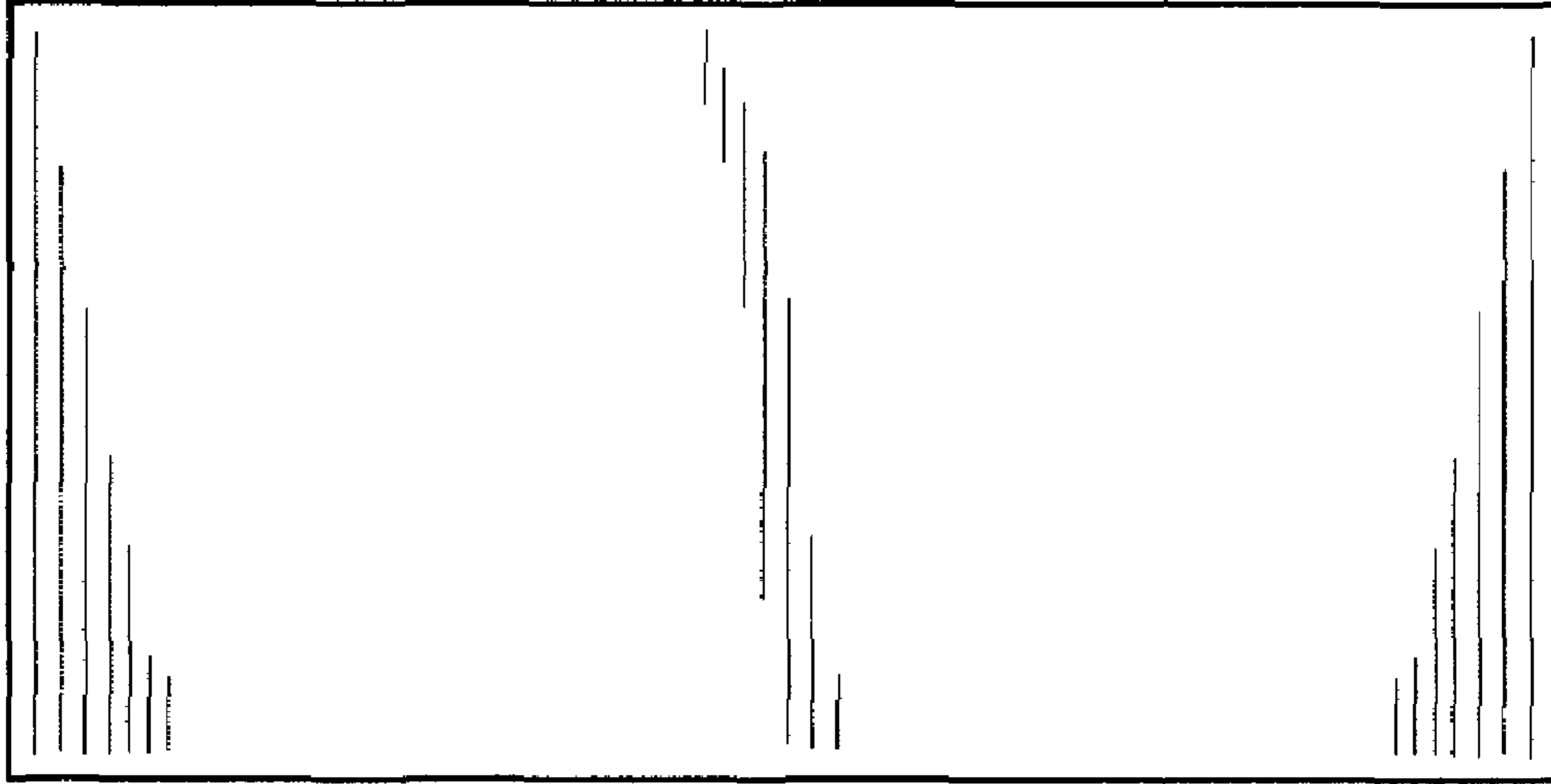


Fig.7

