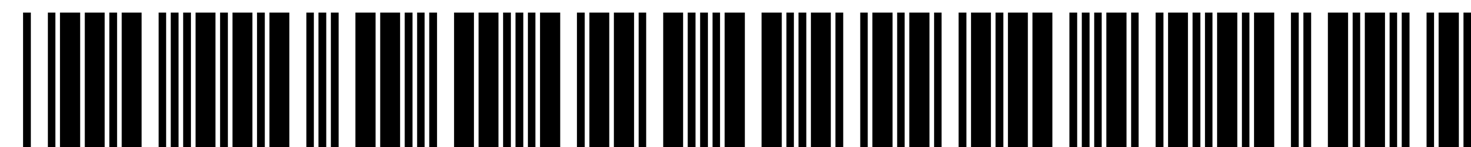

(12) **United States Design Patent** (10) **Patent No.: US D568,838 S**
Terada et al. (45) **Date of Patent: ** May 13, 2008**

(54) **GROOVES FORMED AROUND A SEMICONDUCTOR DEVICE ON A CIRCUIT BOARD**

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(**) Term: **14 Years**

(21) Appl. No.: **29/268,260**

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May 1, 2006	(JP)	2006-011435
May 1, 2006	(JP)	2006-011439
May 1, 2006	(JP)	2006-011440
May 1, 2006	(JP)	2006-011441
May 1, 2006	(JP)	2006-011442

(51) **LOC (8) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; 174/250, 251, 253, 254, 255, 256, 265, 260, 174/261; 361/760, 748, 720; 336/200
See application file for complete search history.

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(74) *Attorney, Agent, or Firm*—Osha Liang LLP

(57) **CLAIM**

The ornamental design for grooves formed around a semiconductor device on a circuit board, as shown and described.

DESCRIPTION

FIG. **1** is a plan view of a first embodiment of the grooves formed around a semiconductor device on a circuit board showing our new design;

FIG. **2** is an enlarged view of the area boxed by the dash-dot-dash line in FIG. **1**;

FIG. **3** is a sectional view taken along line **3**—**3** in FIG. **2**;

FIG. **4** is a sectional view taken along line **4**—**4** in FIG. **2**;

FIG. **5** is a plan view of a second embodiment;

FIG. **6** is an enlarged view of the area boxed by the dash-dot-dash line in FIG. **5**;

FIG. **7** is a sectional view taken along line **7**—**7** in FIG. **6**;

FIG. **8** is a sectional view taken along line **8**—**8** in FIG. **6**;

FIG. **9** is a plan view of a third embodiment;

FIG. **10** is an enlarged view of the area boxed by the dash-dot-dash line in FIG. **9**;

FIG. **11** is a sectional view taken along line **11**—**11** in FIG. **10**; and,

FIG. **12** is a sectional view taken along line **12**—**12** in FIG. **10**.

The broken lines represent unclaimed subject matter.

1 Claim, 6 Drawing Sheets

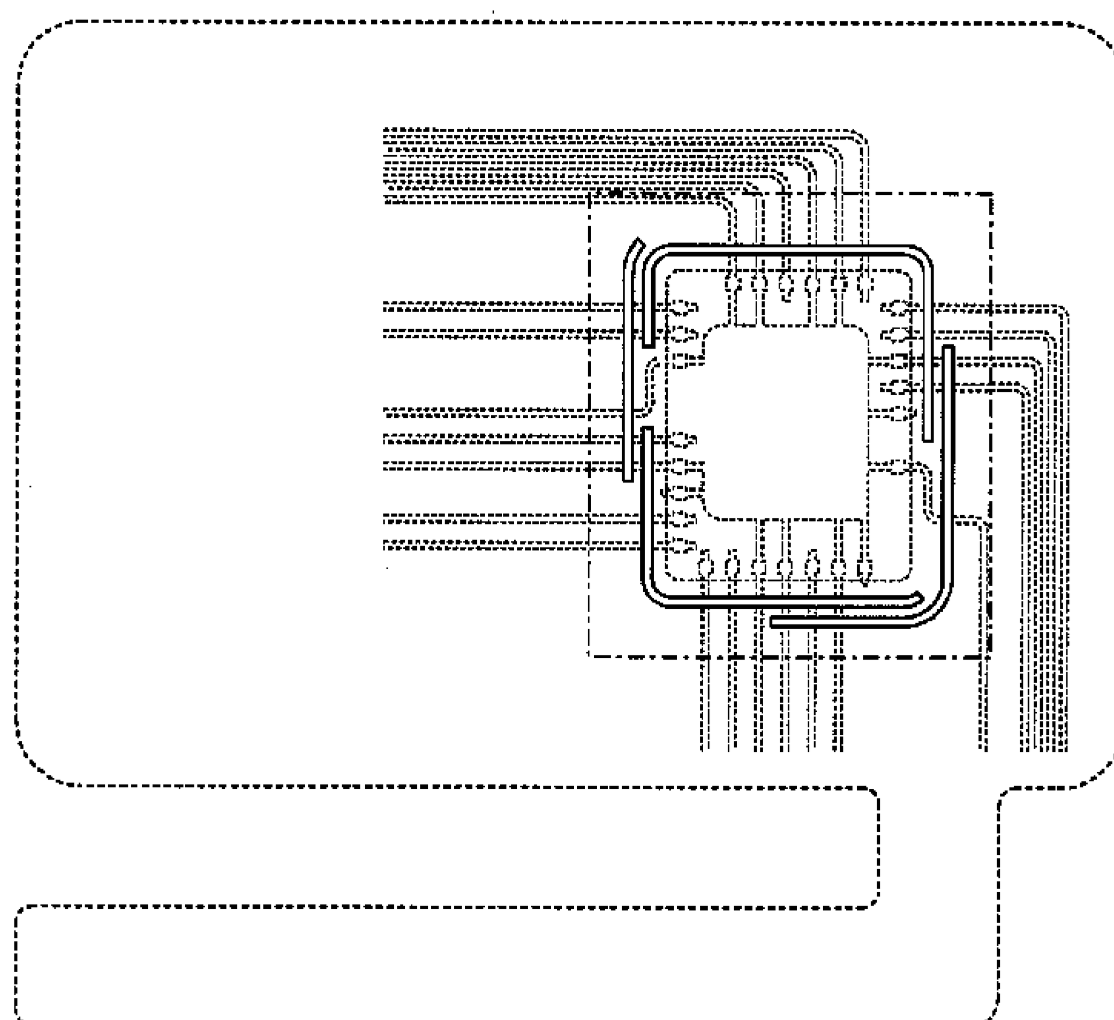
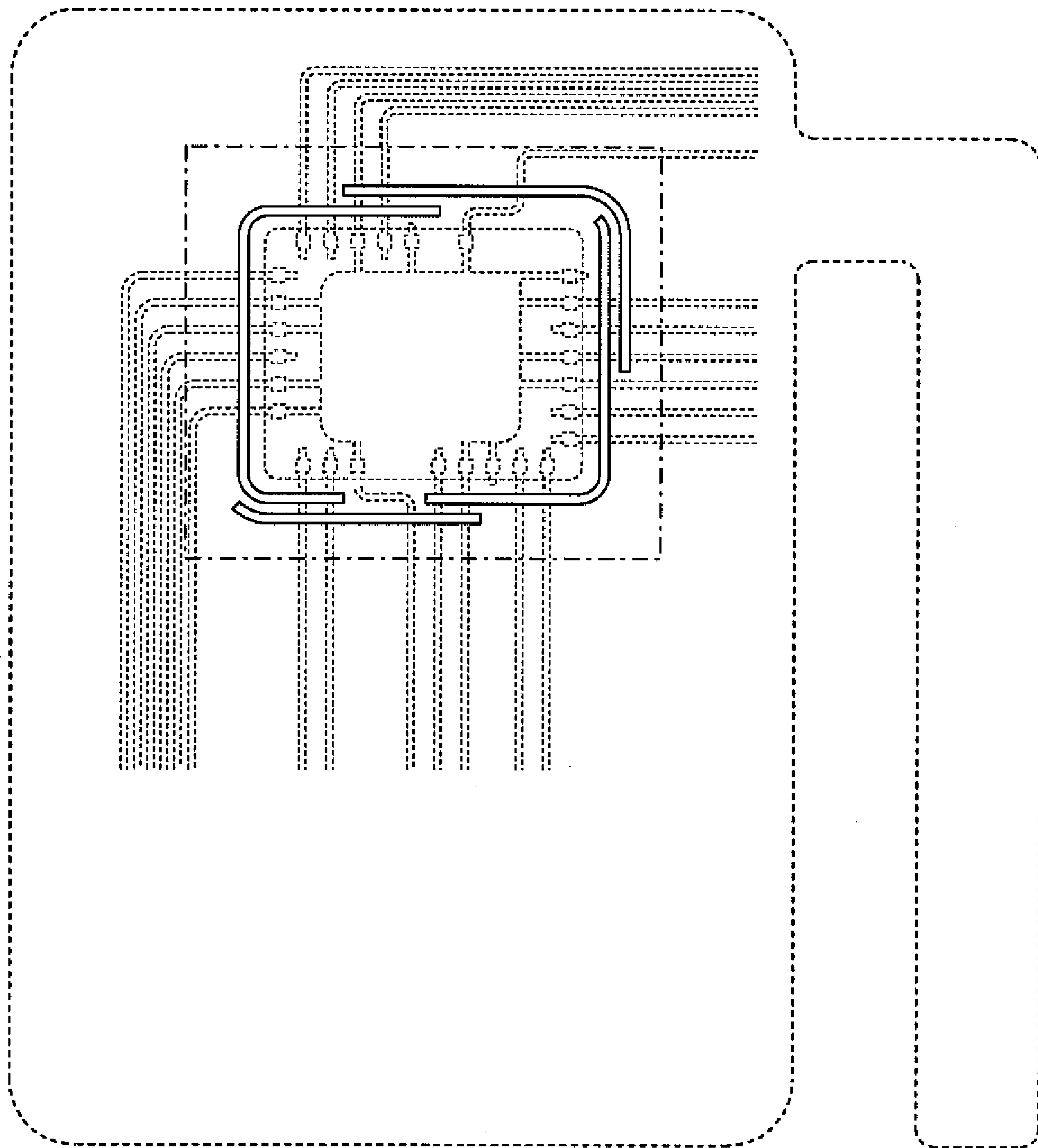


FIG. 1



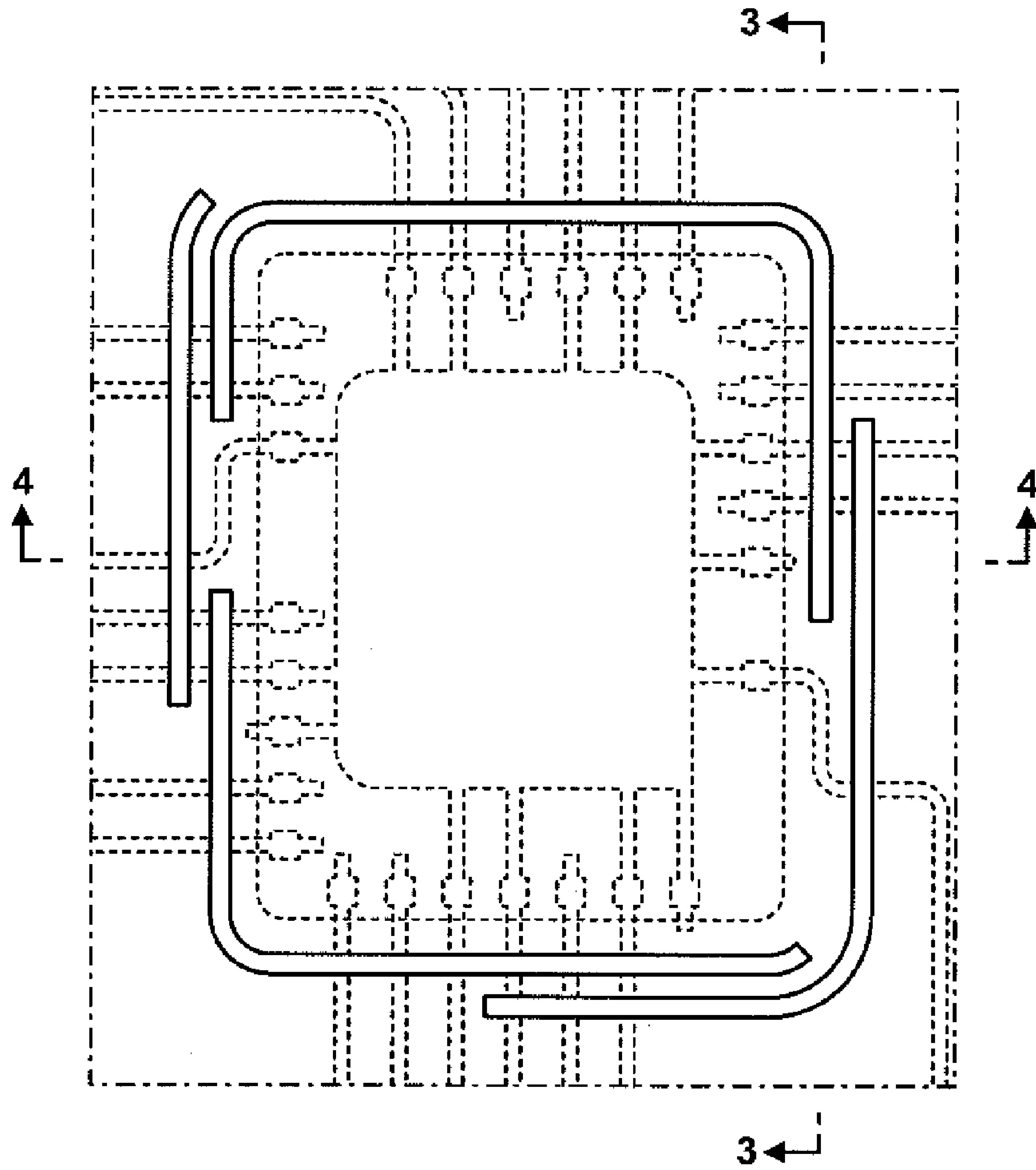


FIG. 2

FIG. 3

FIG. 4

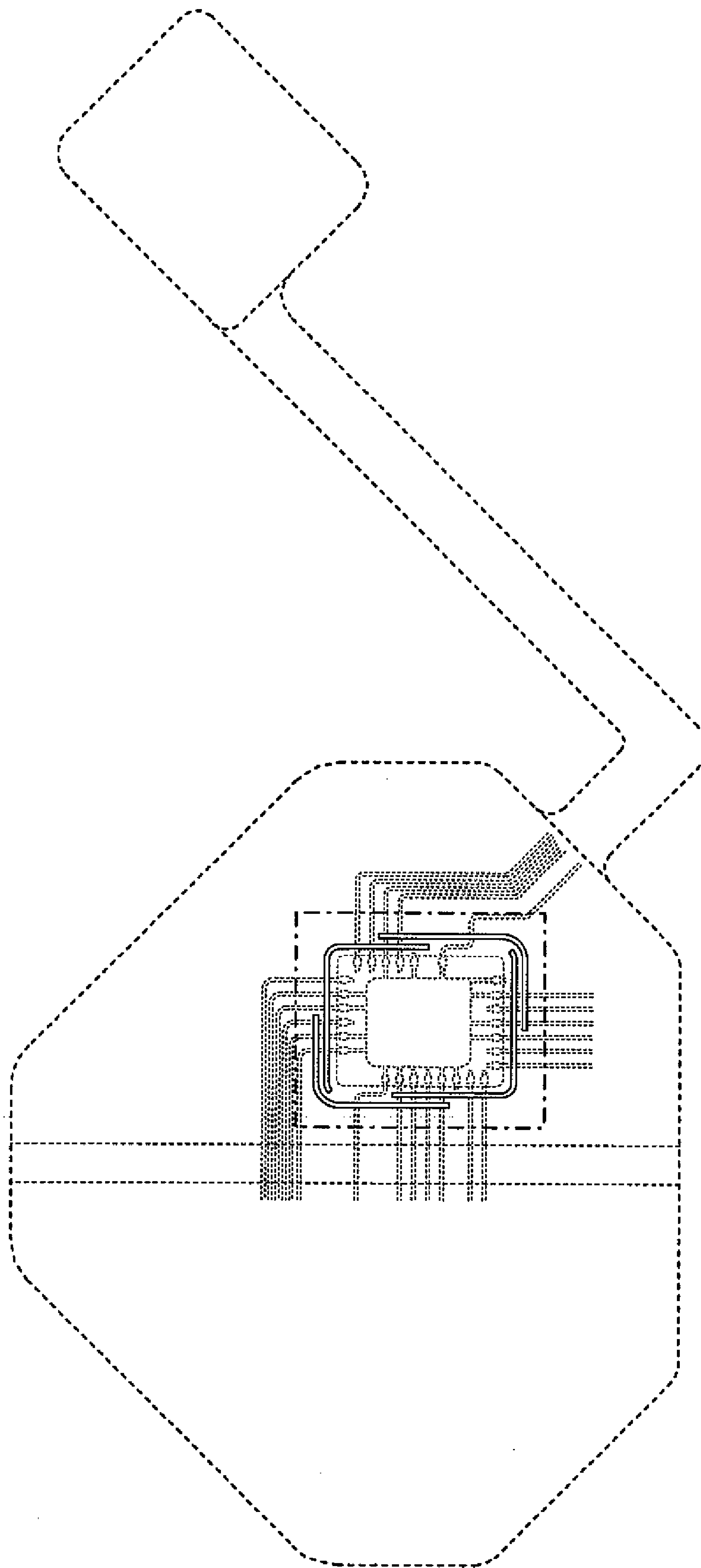


FIG. 5

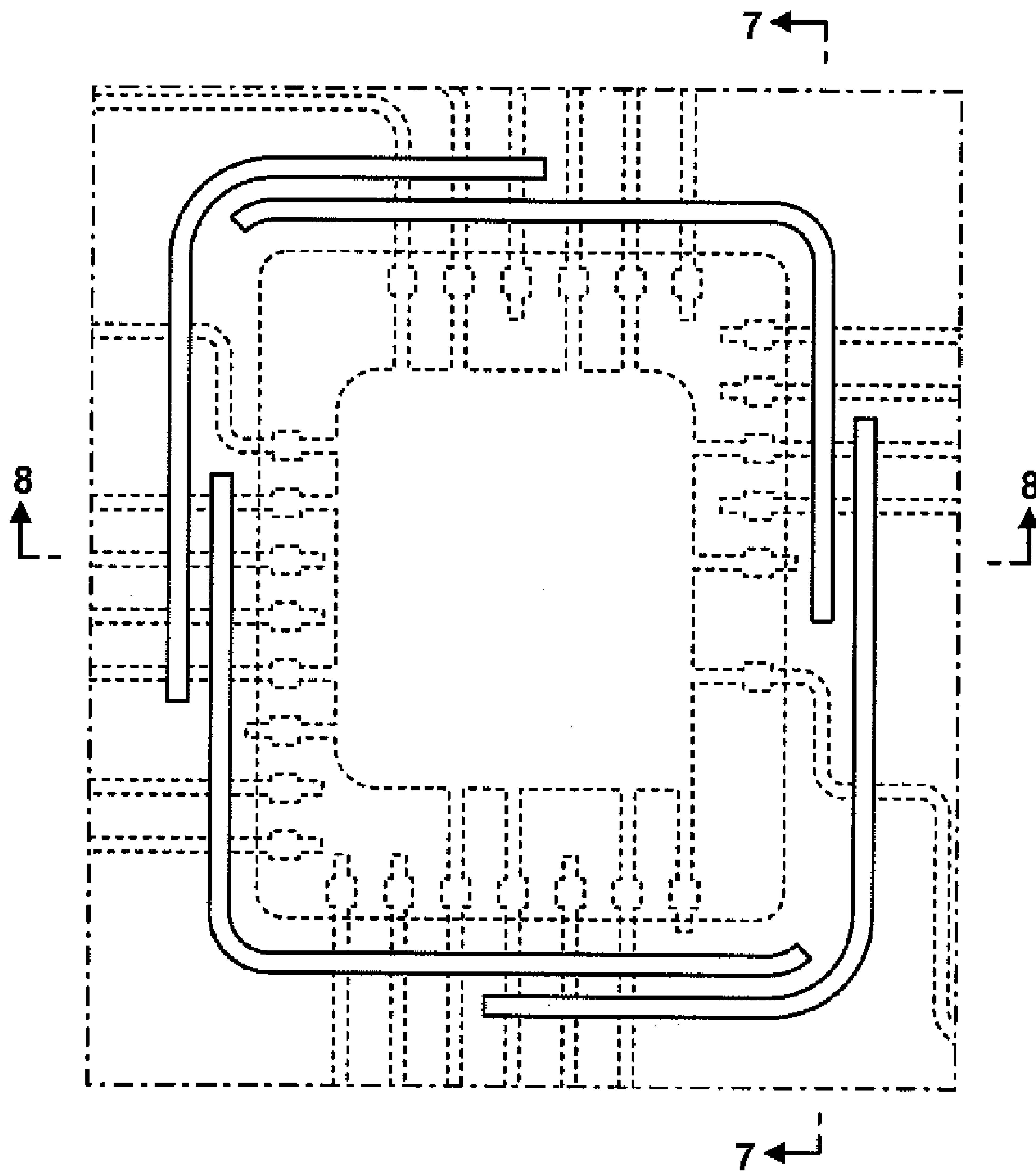


FIG. 6

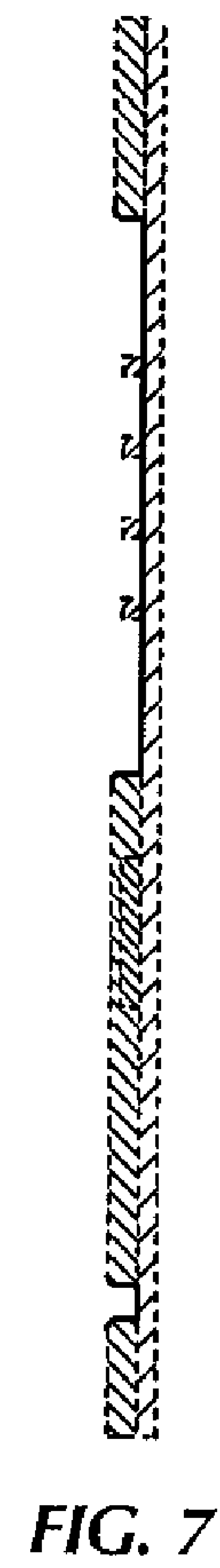


FIG. 7

FIG. 8

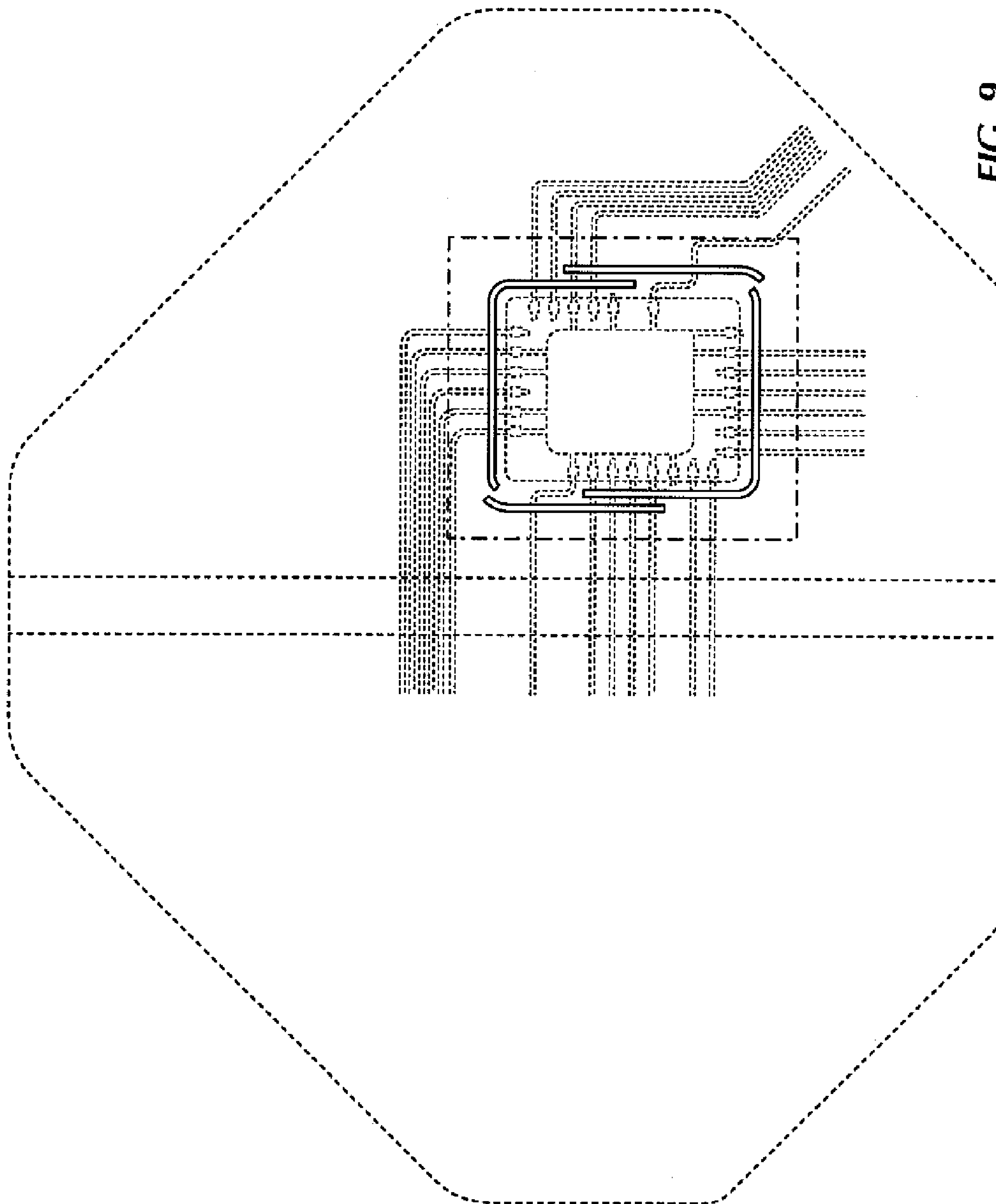


FIG. 9

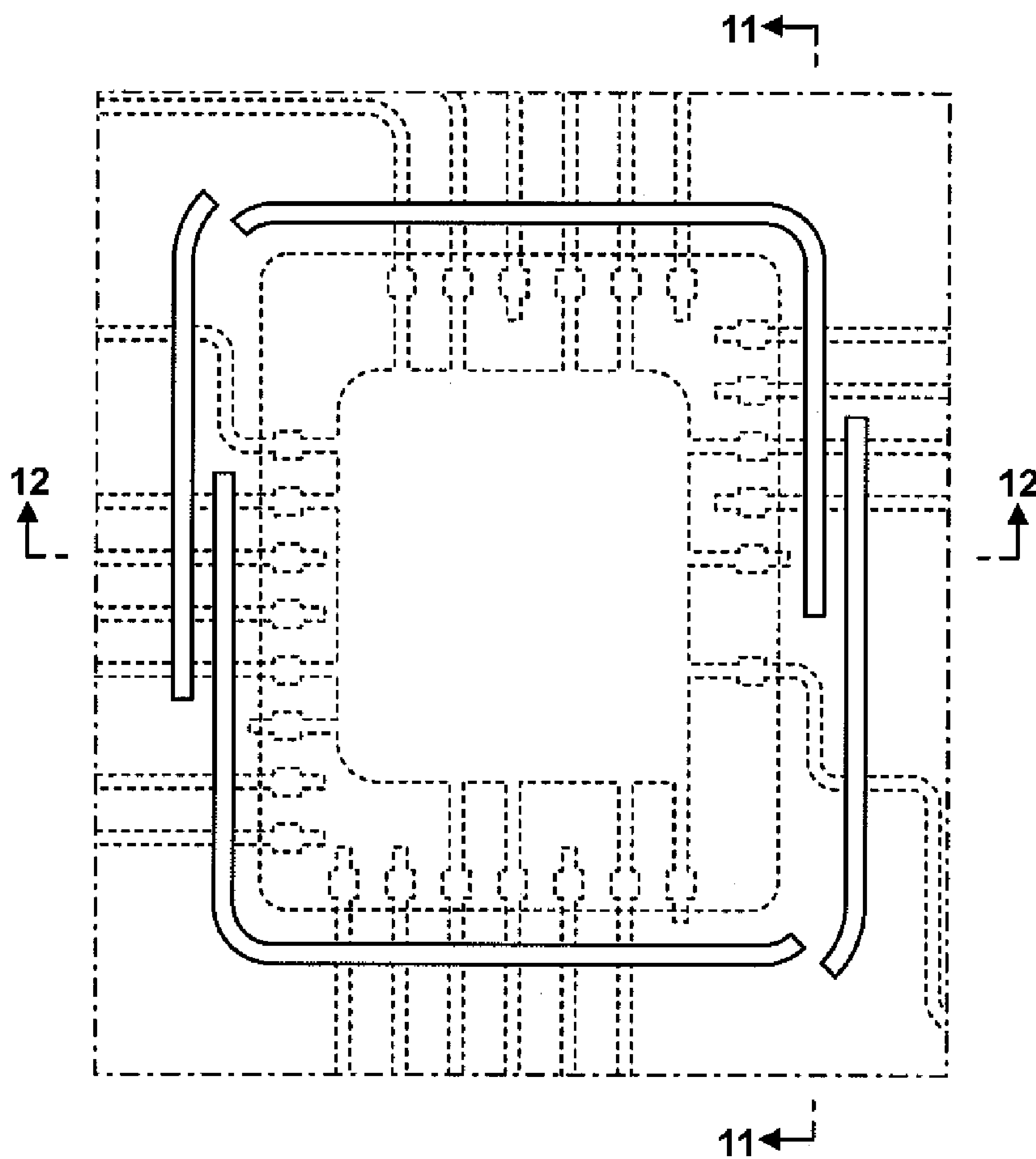


FIG. 10

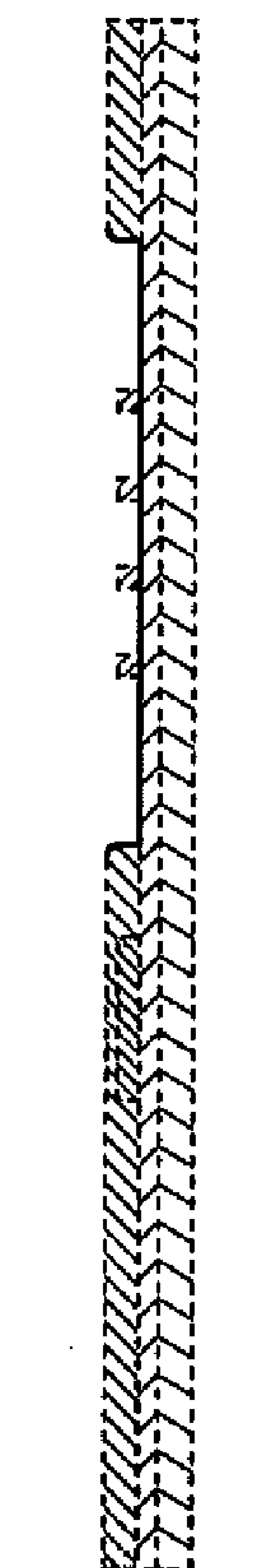


FIG. 11

FIG. 12