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(12) **United States Design Patent** (10) **Patent No.:** **US D566,060 S**  
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(54) **GROOVES FORMED AROUND A SEMICONDUCTOR DEVICE ON A CIRCUIT BOARD**

D510,103 S \* 9/2005 Allard et al. .... D19/10

**FOREIGN PATENT DOCUMENTS**

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JP 11-8275 1/1999

**OTHER PUBLICATIONS**

(73) Assignee: **Nitto Denko Corporation**, Osaka (JP)

Office Action dated Nov. 4, 2005 for Japanese Application No. 2005-010995 (2 pages).

(\*\*) Term: **14 Years**

English Translation of Japanese Publication No. 11-8275 dated Jan. 12, 1999 (16 pages).

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English translation of Office Action dated Nov. 4, 2005 for Japanese Patent Application No. 2005-010995 (1 page).

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\* cited by examiner

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(51) **LOC (8) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Classification Search** ..... D13/182,  
D13/158-177; 336/200; 324/754; D1/106;  
D19/10; 361/813

See application file for complete search history.

(57) **CLAIM**

The ornamental design for grooves formed around a semiconductor device on a circuit board, as shown and described.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

3,676,748 A \* 7/1972 Kobayashi et al. .... 361/813  
D279,670 S \* 7/1985 Lukits ..... D13/182  
D288,556 S \* 3/1987 Wallgren ..... D13/182  
D295,401 S \* 4/1988 Klees ..... D13/182  
5,008,614 A \* 4/1991 Shreeve et al. .... 324/754  
D318,271 S \* 7/1991 Hasegawa et al. .... D13/182  
D319,629 S \* 9/1991 Hasegawa et al. .... D13/182  
D374,541 S \* 10/1996 Garza ..... D1/106  
5,969,590 A \* 10/1999 Gutierrez ..... 336/200  
6,114,937 A \* 9/2000 Burghartz et al. .... 336/200  
D487,430 S \* 3/2004 Asaka et al. .... D13/182

**DESCRIPTION**

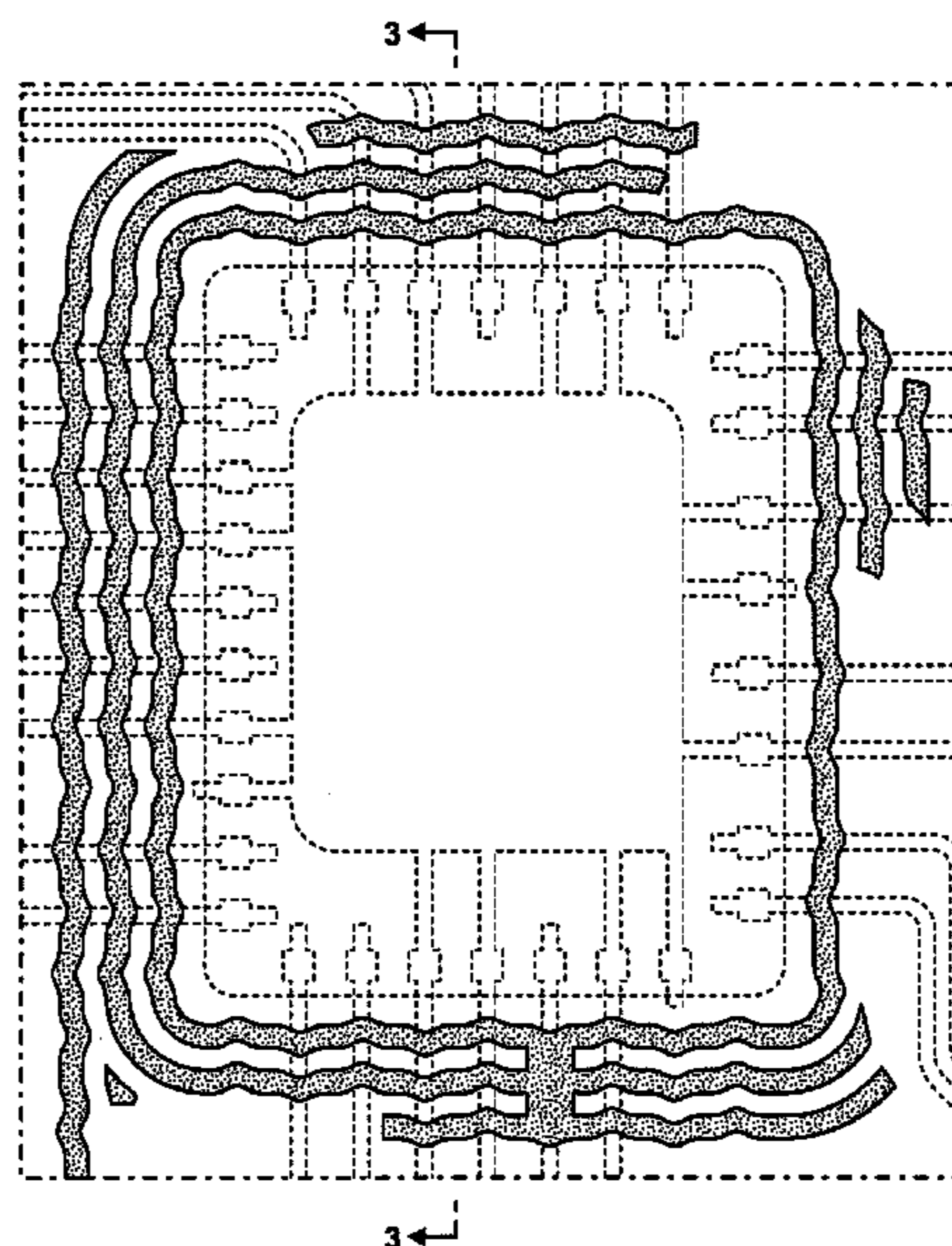
FIG. 1 shows a plan view of grooves formed around a semiconductor device on a circuit board showing our new design.

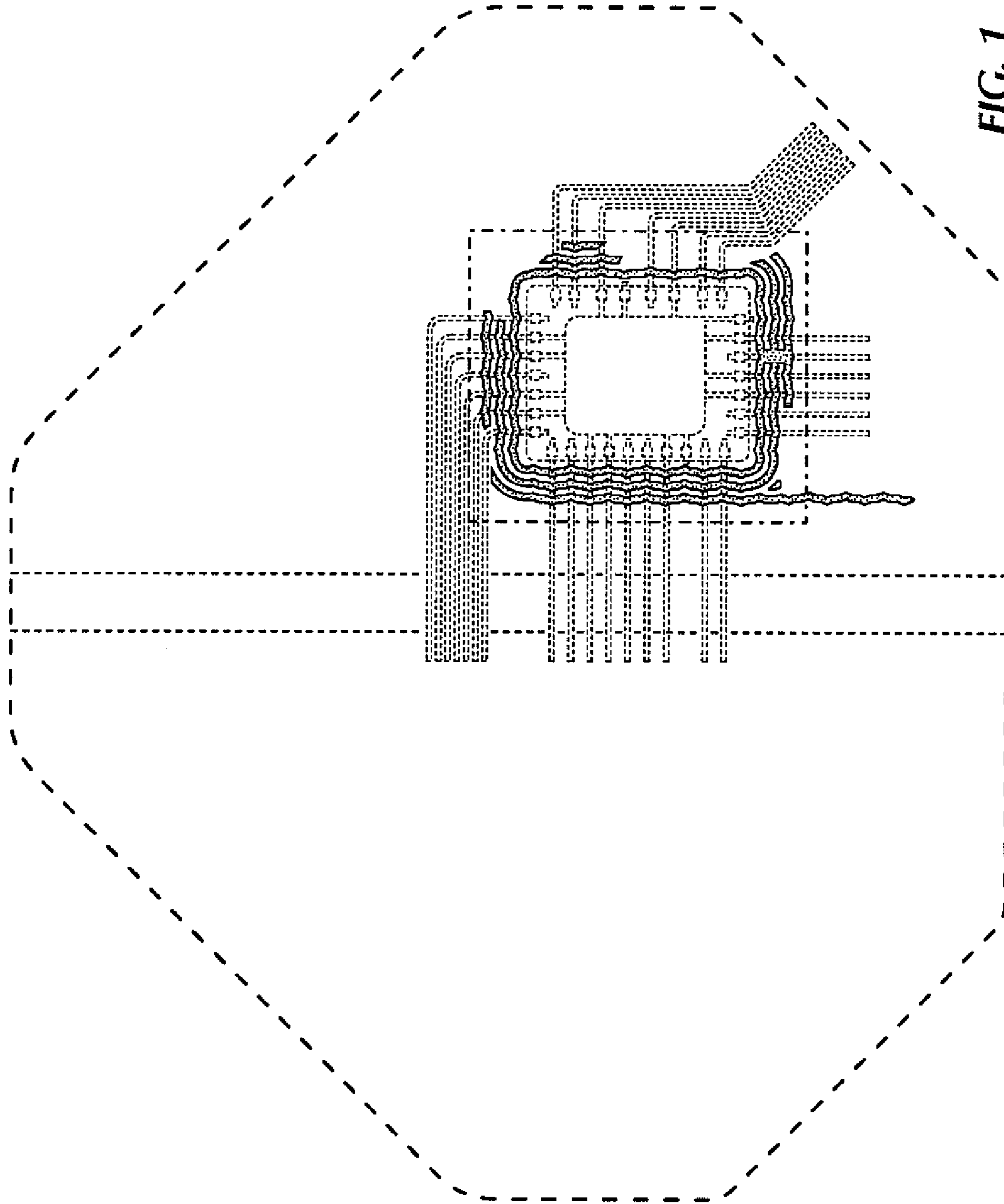
FIG. 2 shows an enlarged view of the claimed portion identified by the dot-dash line in FIG. 1; and,

FIG. 3 shows an enlarged sectional view along the line 3—3 in FIG. 2.

The special dot-dash broken line defines the boundary of the claimed design; the gray stippling indicates the surface of the groove bed; the broken lines show environmental detail for illustrative purposes only and form no part of the claimed design.

**1 Claim, 3 Drawing Sheets**





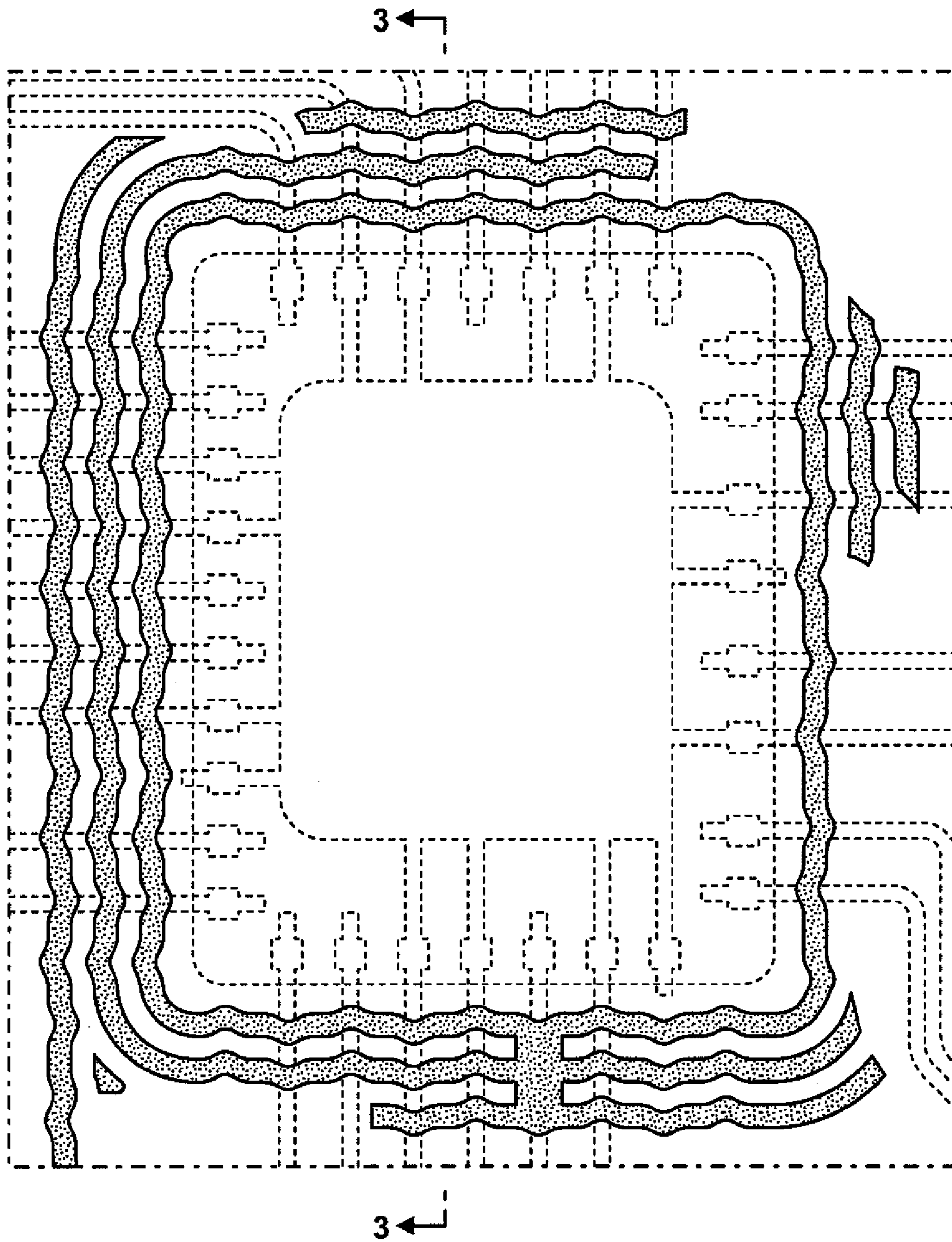


FIG. 2



**FIG. 3**