



US00D552552S

(12) **United States Design Patent**
Chan

(10) **Patent No.:** **US D552,552 S**

(45) **Date of Patent:** **** Oct. 9, 2007**

(54) **SERIAL TO PARALLEL ELECTRICAL
TRANSCEIVER**

D527,709 S * 9/2006 Kuo D13/147
2005/0124227 A1* 6/2005 Liu et al. 439/680

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(US)

* cited by examiner

Primary Examiner—Daniel Bui

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(57) **CLAIM**

(**) Term: **14 Years**

The ornamental design for a serial to parallel electrical transceiver, as shown and described.

(21) Appl. No.: **29/242,351**

DESCRIPTION

(22) Filed: **Nov. 9, 2005**

FIG. 1 is a top, front and right side perspective view of a serial to parallel electrical transceiver, showing my new design;

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/147**

(58) **Field of Classification Search** D13/123,
D13/133, 146–147, 154, 184, 199; D14/356,
D14/432, 433, 435, 438; 439/350, 352, 357–358,
439/606–610, 660, 677, 680–682, 686, 936
See application file for complete search history.

FIG. 2 is a top plan view thereof;

FIG. 3 is a bottom plan view thereof;

FIG. 4 is a right side elevational view thereof;

FIG. 5 is a left side elevational view thereof;

FIG. 6 is a front elevational view thereof; and,

FIG. 7 is a rear elevational view thereof.

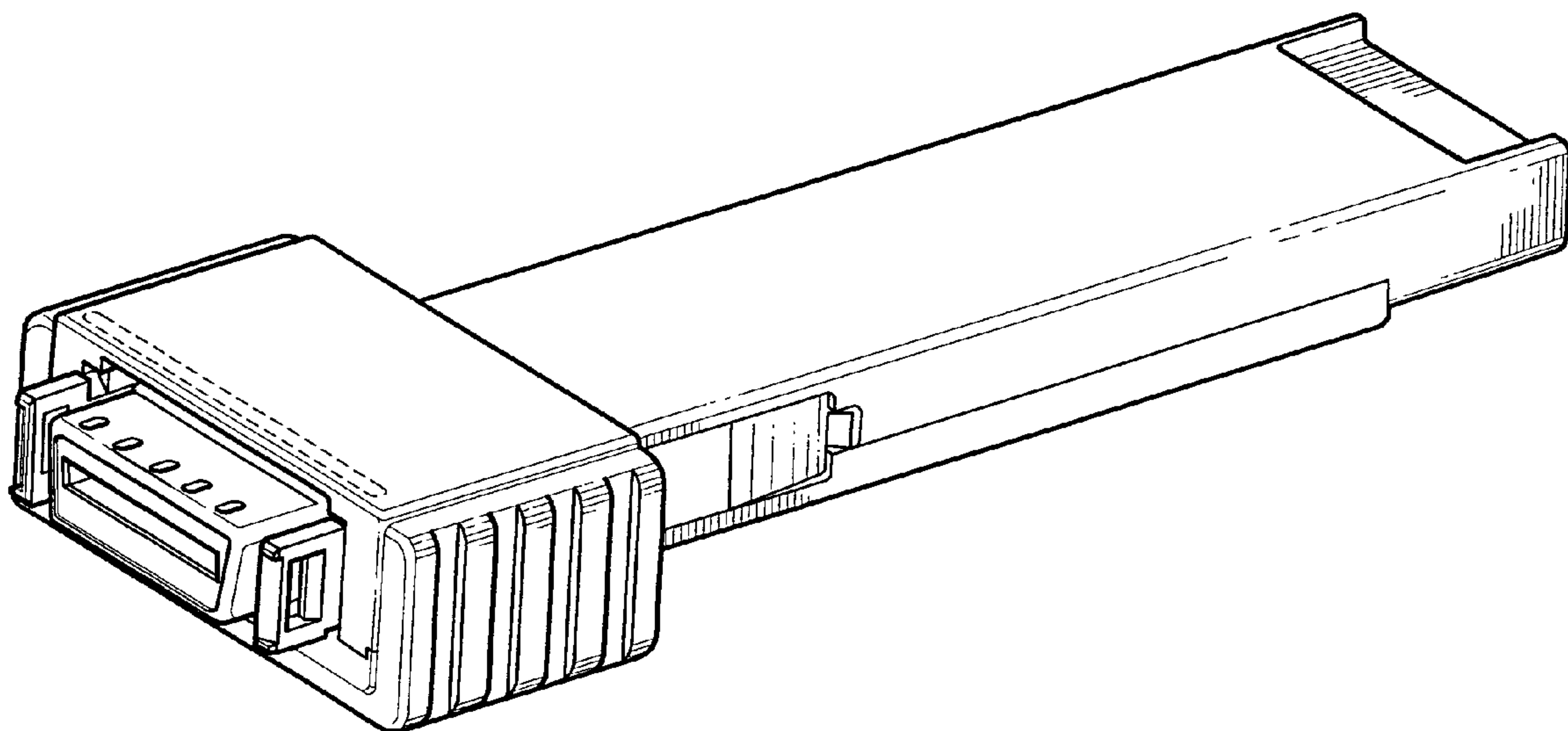
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5,934,942 A * 8/1999 Patel et al. 439/610
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The broken line showing of the environment is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 4 Drawing Sheets



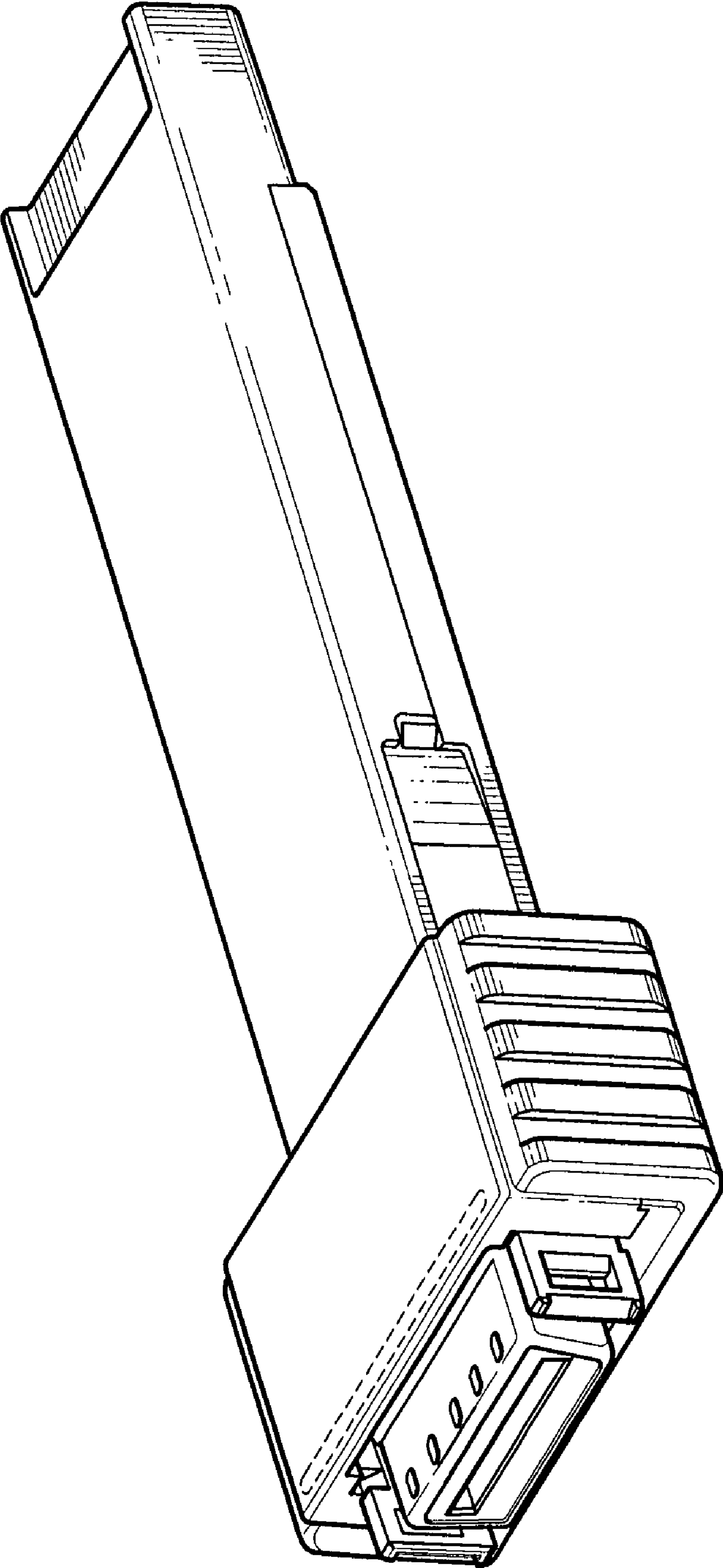


FIG. 1

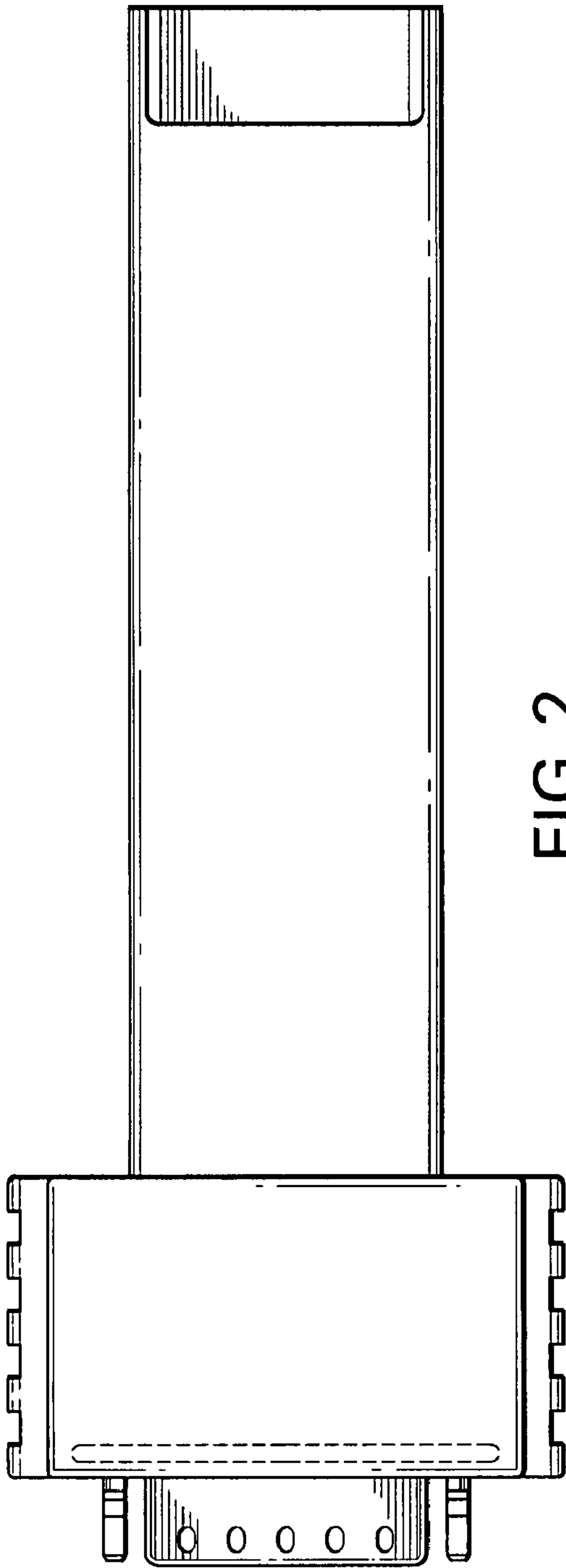


FIG. 2

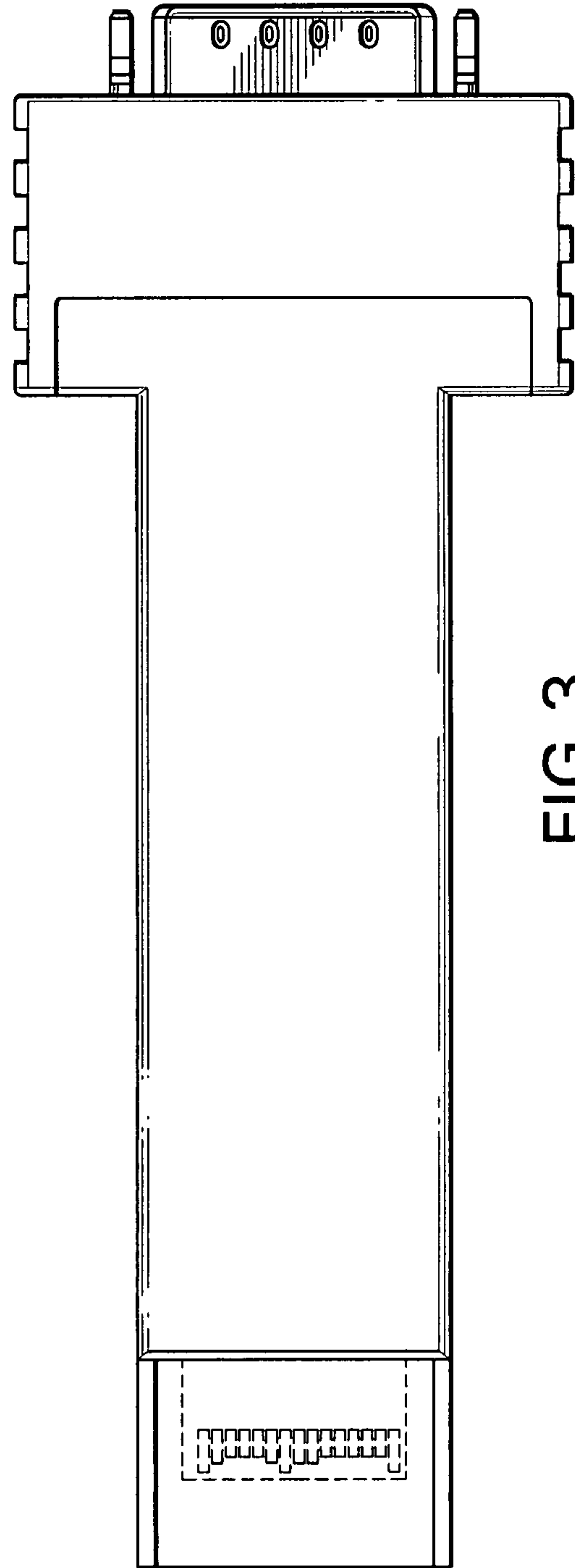


FIG. 3

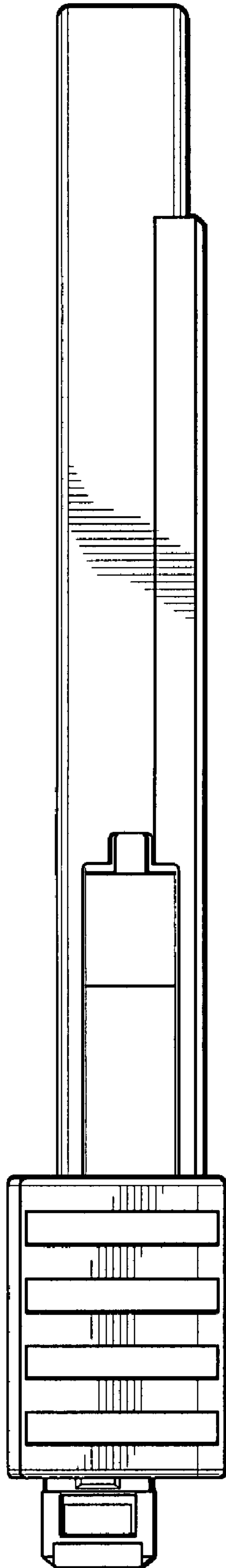


FIG. 4

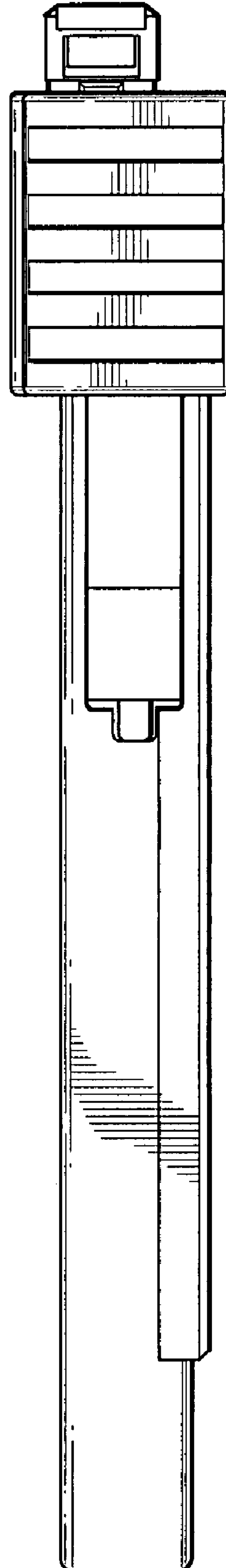


FIG. 5

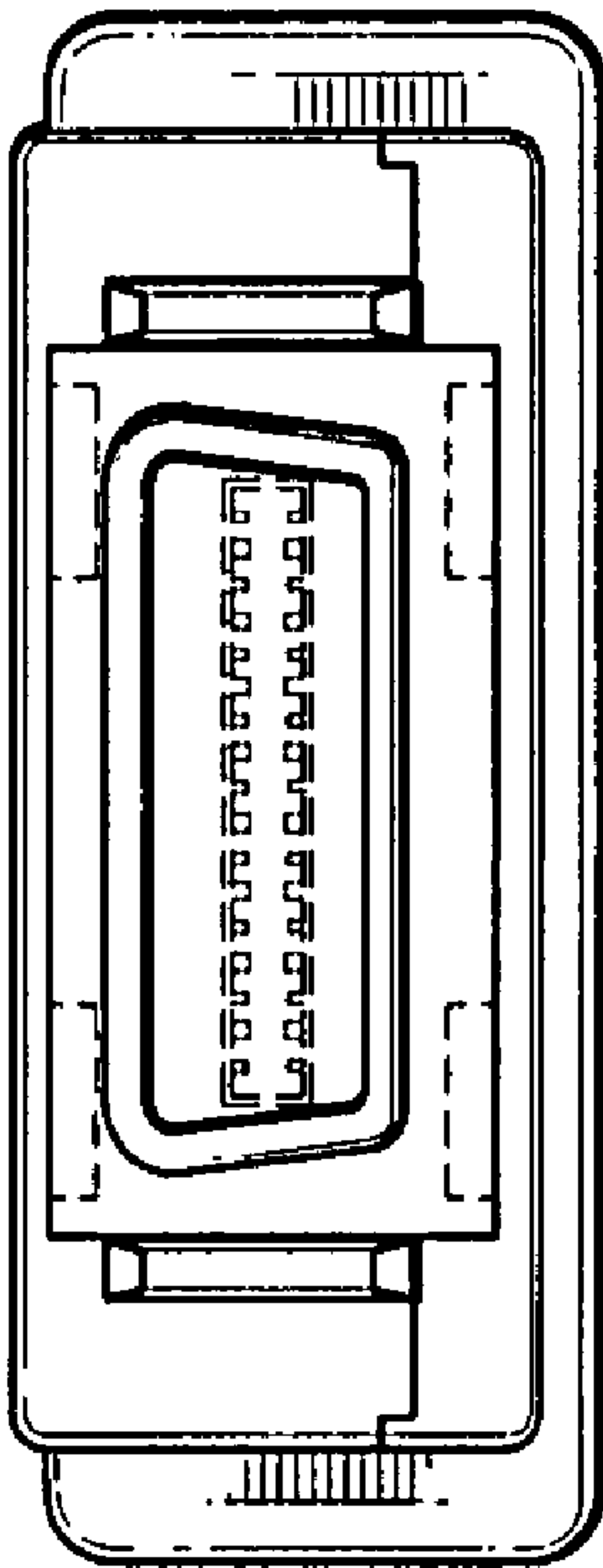


FIG. 6

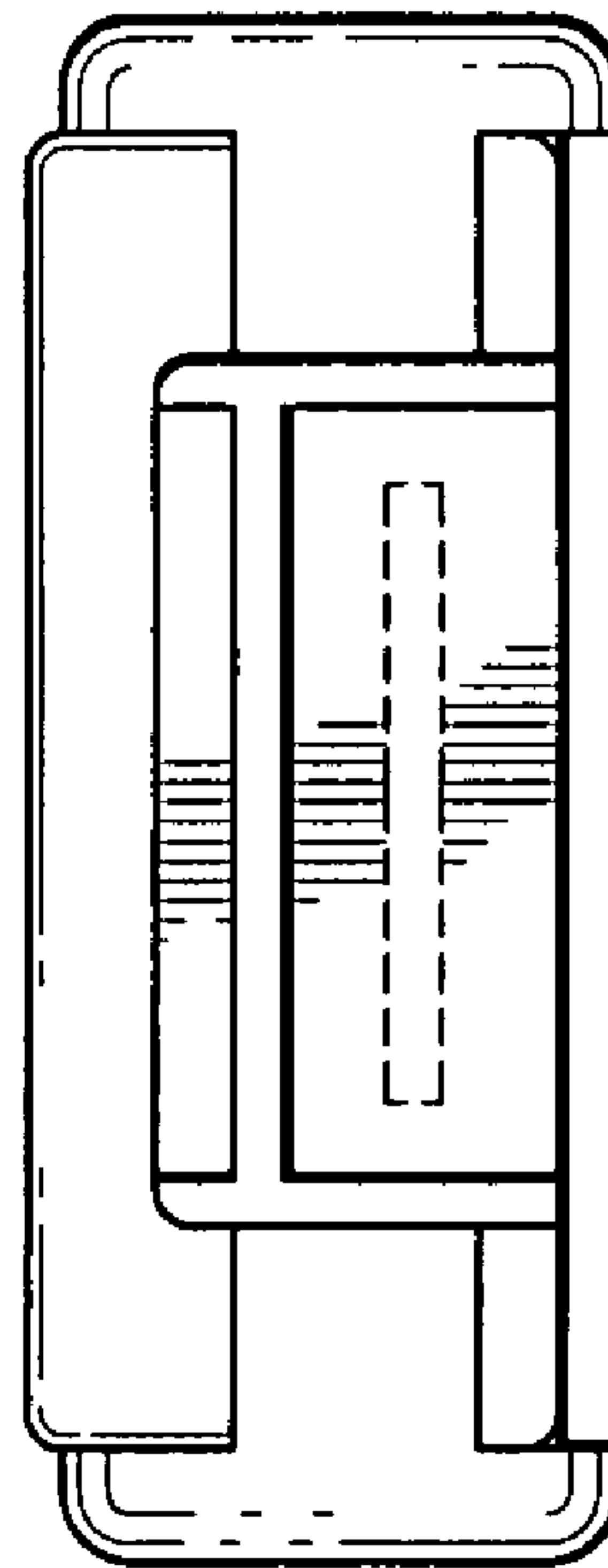


FIG. 7