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(12) **United States Design Patent**
Sugawara

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(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

Feb. 28, 2005 (JP) 2005-005770

(51) **LOC (8) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; D7/600.2, 701; D23/266; 83/35, 39; 118/715; 138/92, 118, 118.1, 121, 178; 206/454, 711; 211/41.18; 414/935; 432/253
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a process tube for manufacturing semiconductor wafers, as shown and described.

DESCRIPTION

FIG. **1** is a reference perspective view of the process tube for manufacturing semiconductor wafers;

FIG. **2** is a reference perspective view of the process tube as seen from another direction;

FIG. **3** is a front view of the process tube;

FIG. **4** is a back view thereof;

FIG. **5** is a left side view thereof. A right side view thereof is a mirror image thereto;

FIG. **6** is a top view thereof;

FIG. **7** is a bottom view thereof;

FIG. **8** is a sectional view taken along line **8**—**8** in FIG. **6**; and,

FIG. **9** is a sectional view taken along line **9**—**9** in FIG. **3**.

1 Claim, 4 Drawing Sheets

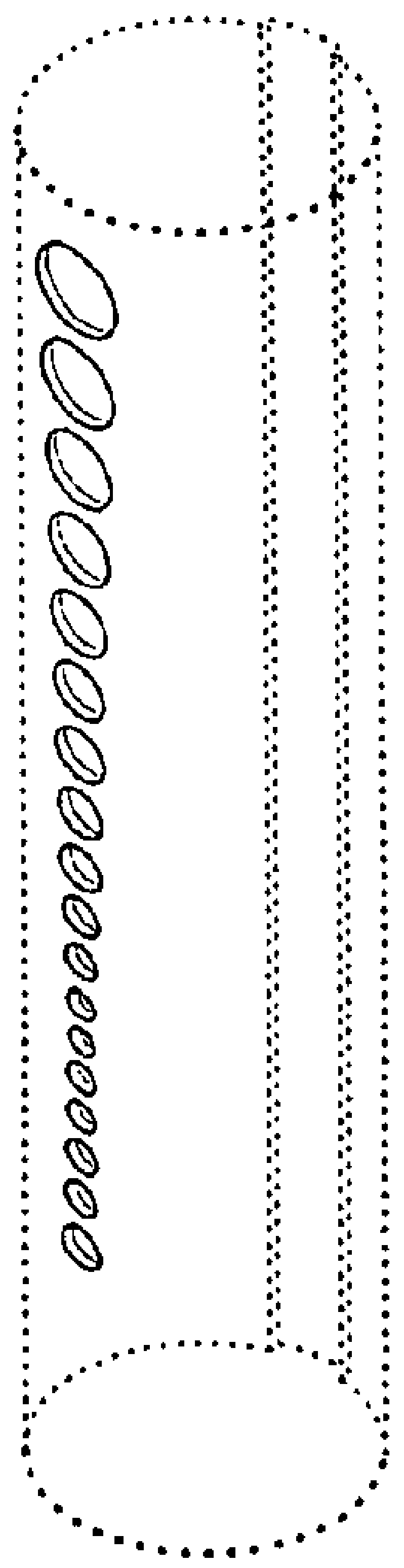

FIG. 1

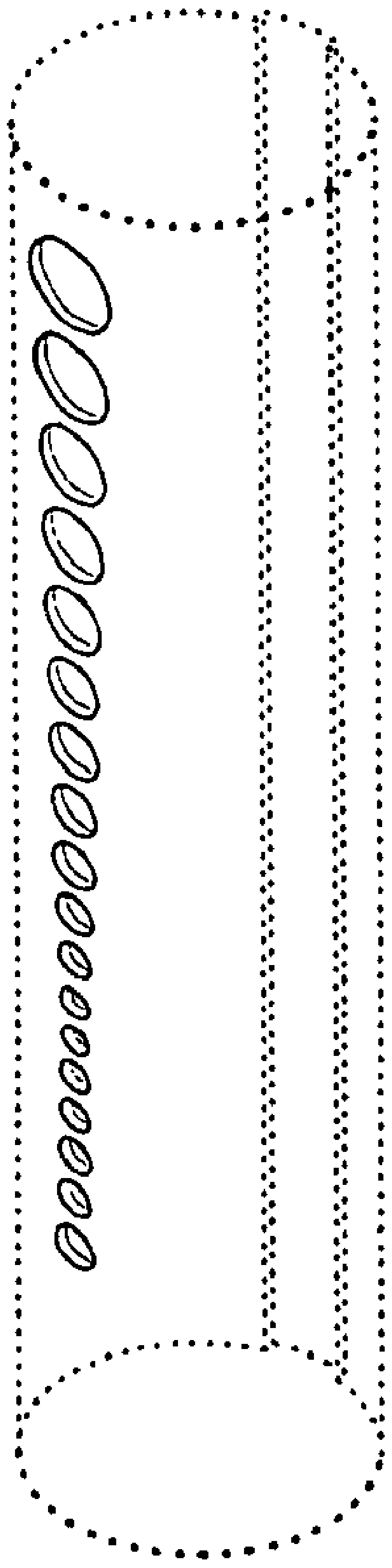

FIG. 2

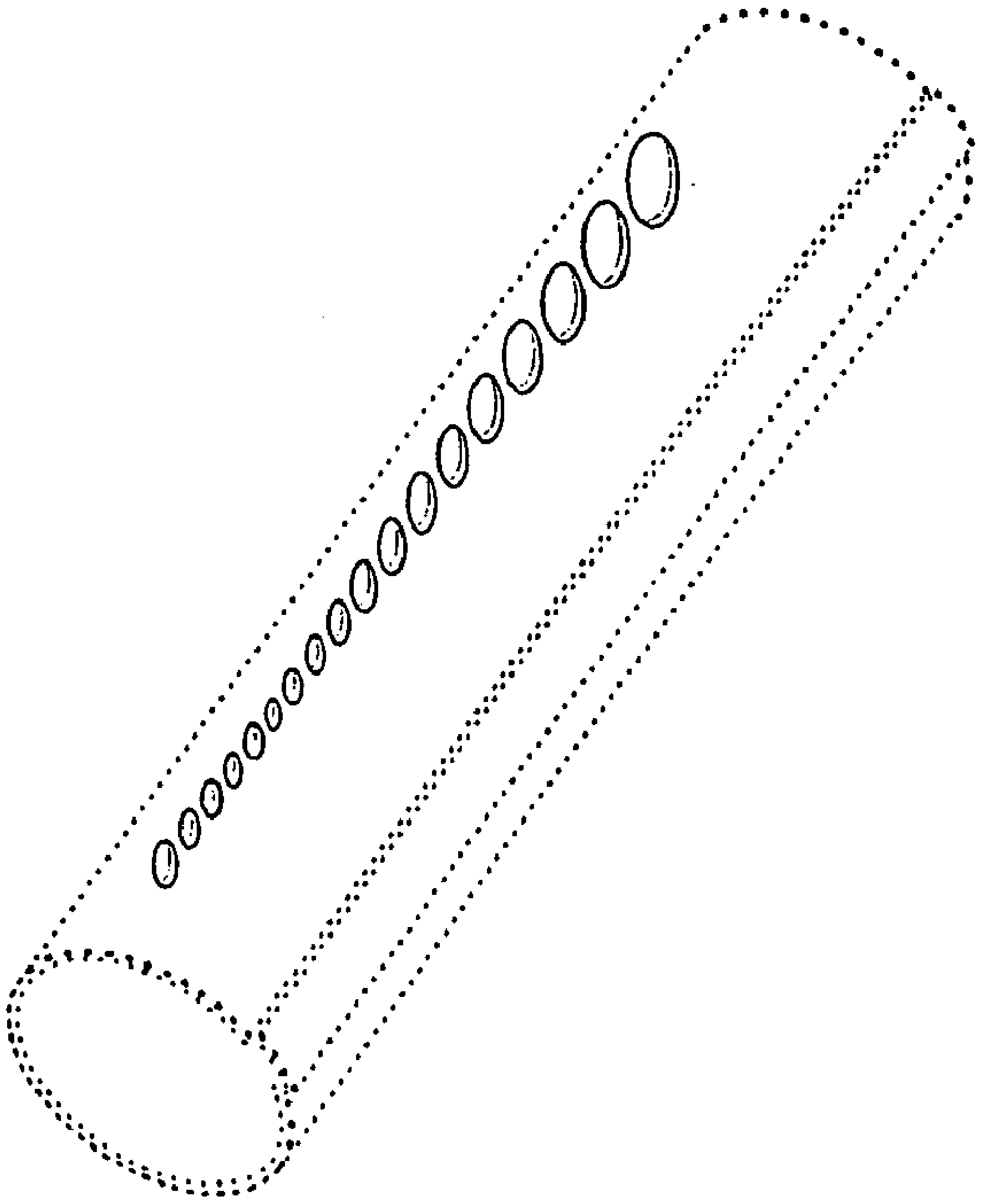

FIG. 3

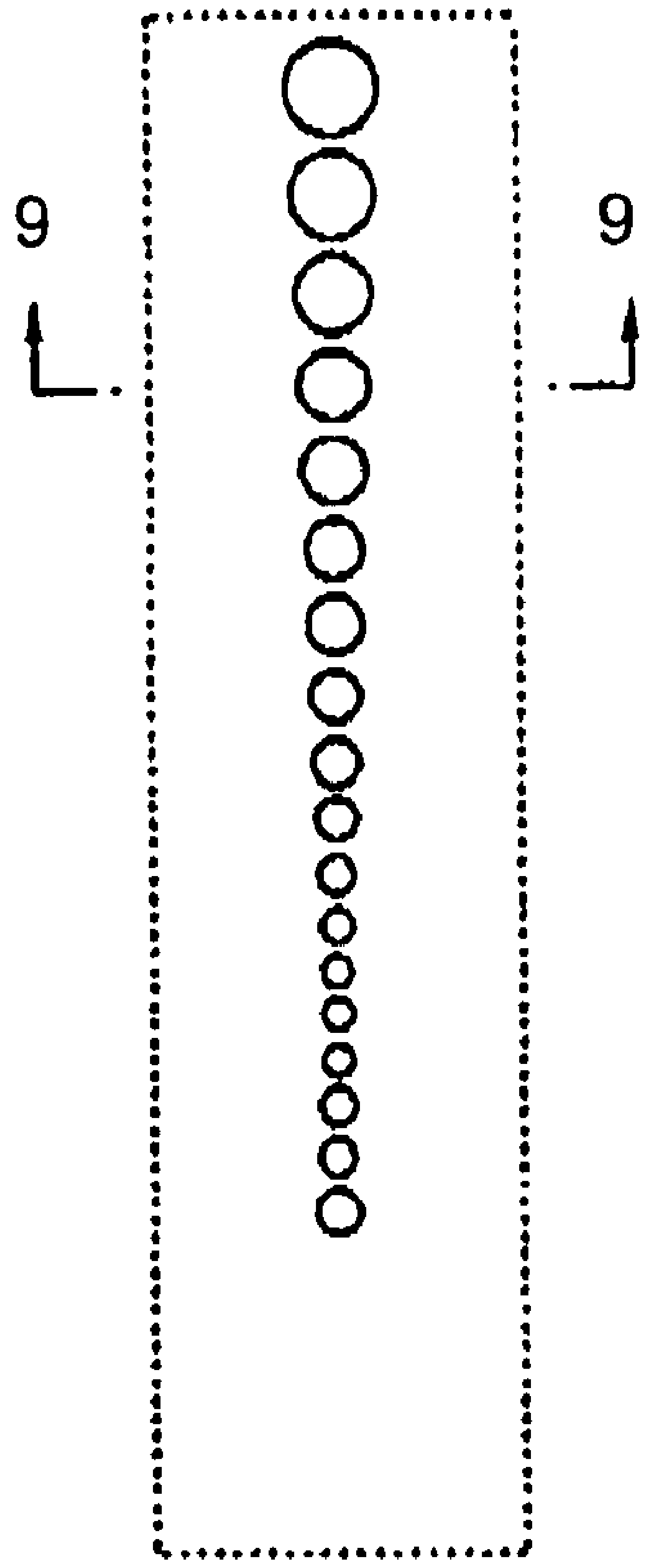

FIG. 4

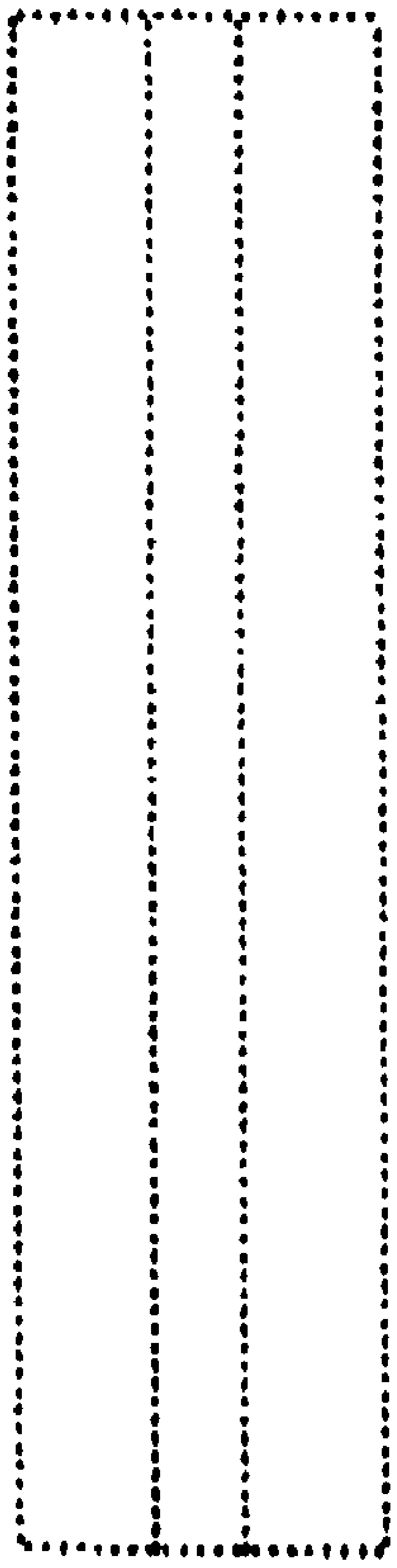

FIG. 5

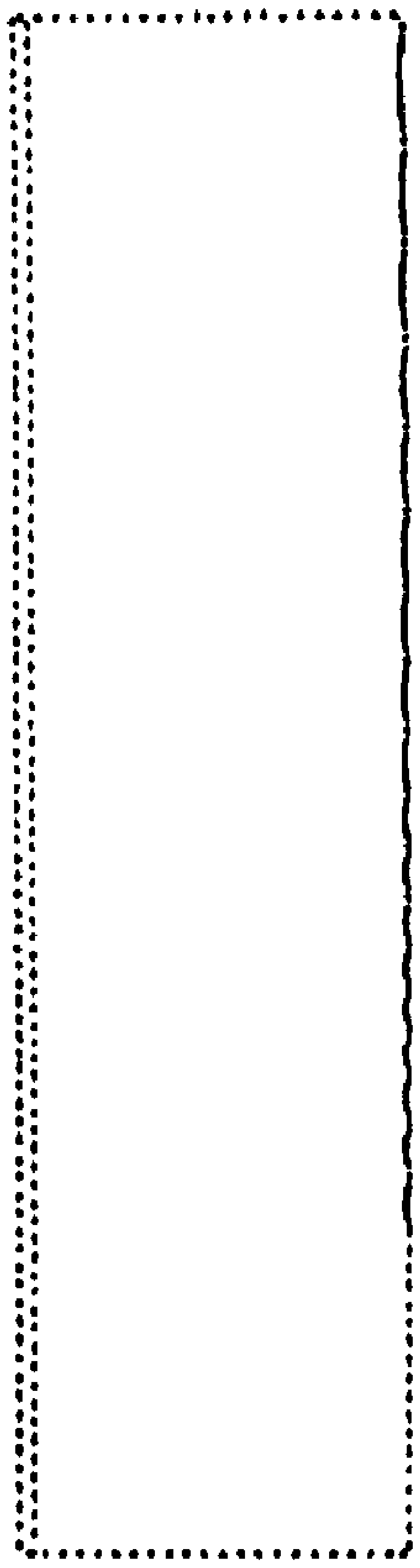

FIG. 6

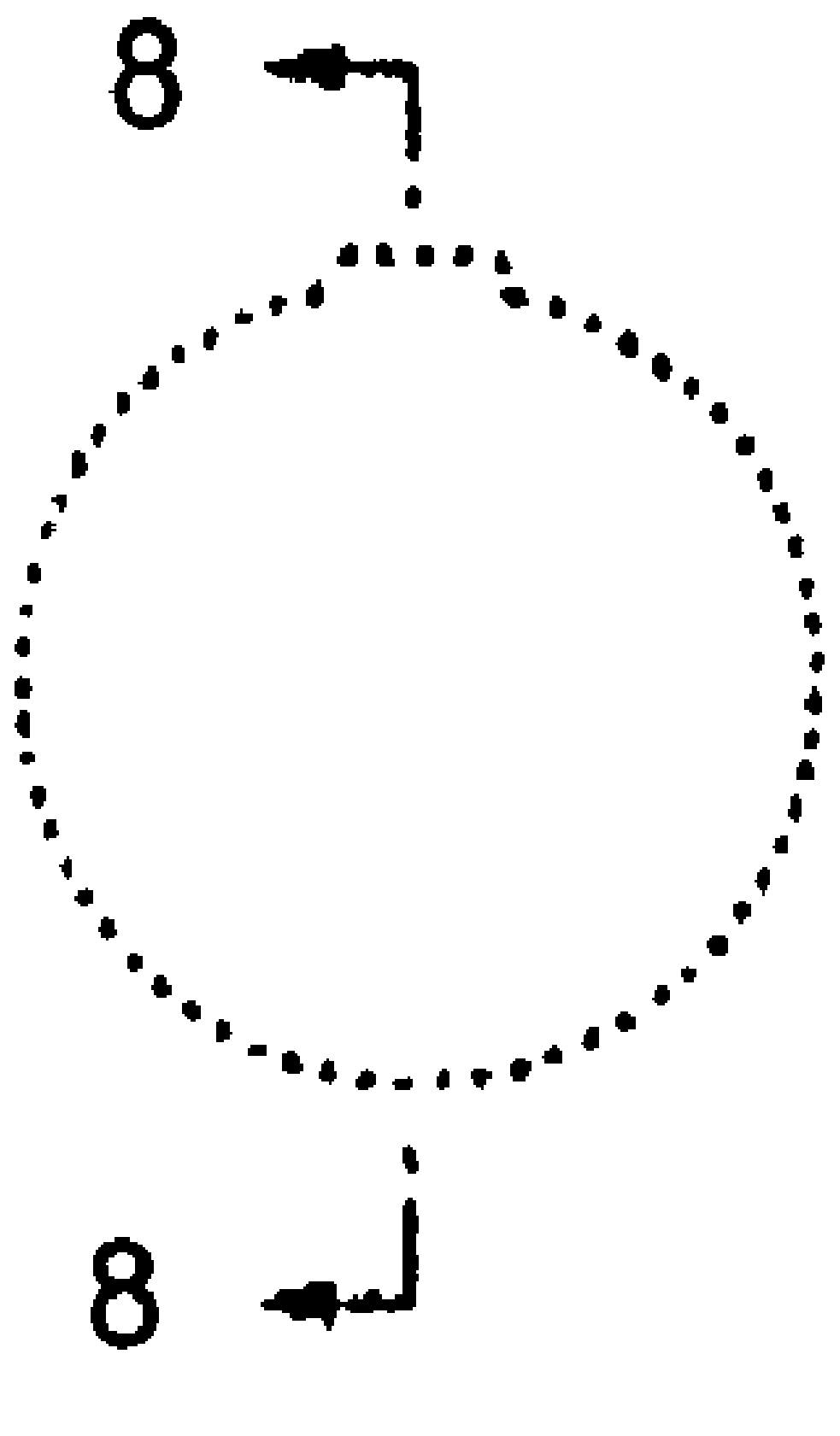

FIG. 7

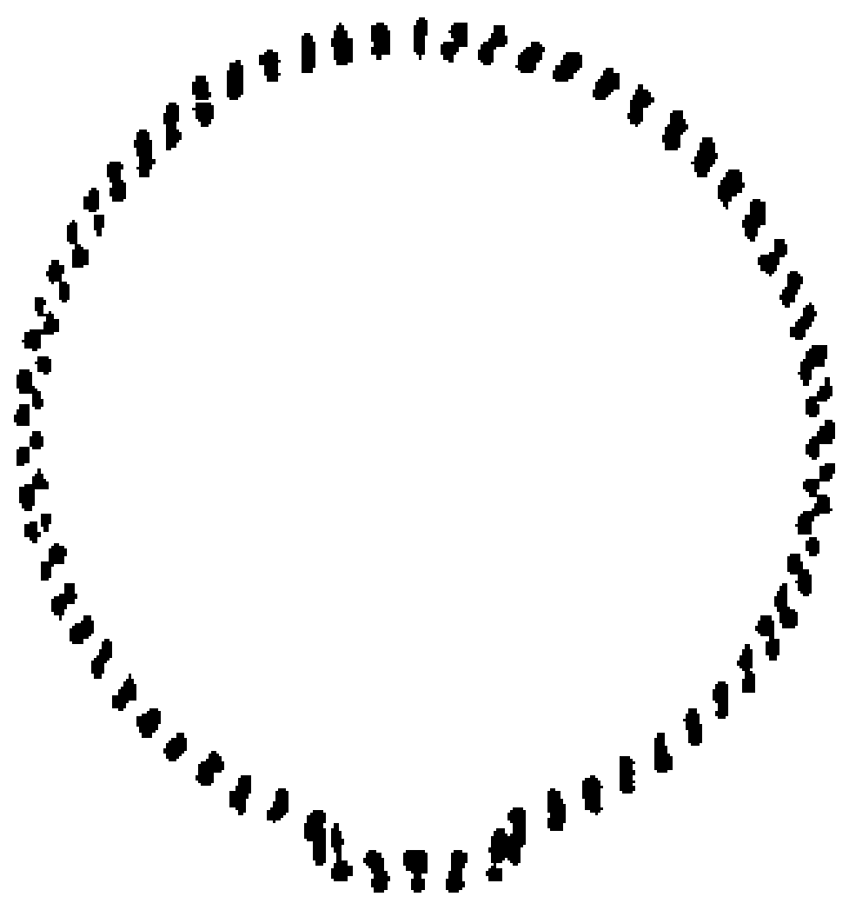

FIG. 8

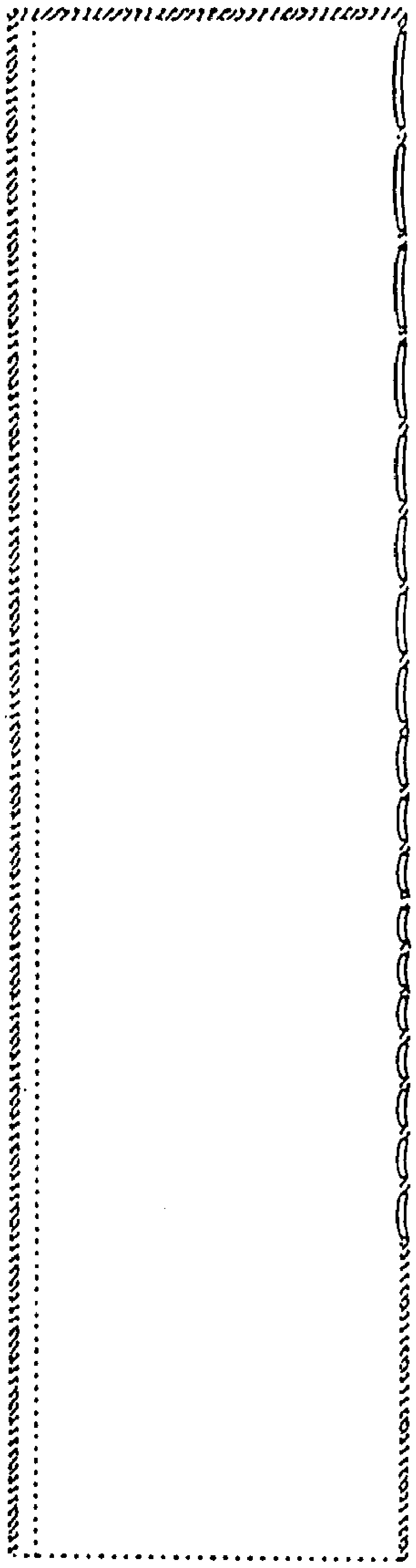

FIG. 9