US00D545703S

(12) **United States Design Patent** (10) **Patent No.: US D545,703 S**
Ikeda (45) **Date of Patent: ** Jul. 3, 2007**

(54) **ELECTRICAL TEST INSTRUMENT**

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(73) Assignee: **Fluke Corporation**, Everett, WA (US)

(**) Term: **14 Years**

(21) Appl. No.: **29/181,322**

(22) Filed: **May 7, 2003**

(51) **LOC (8) Cl.** **10-04**
(52) **U.S. Cl.** **D10/79**; D10/78; D10/75
(58) **Field of Classification Search** ..... D10/78, D10/79, 75; 324/115, 116, 117 R, 117 H, 324/126–130, 142, 143, 149, 156
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D510,044 S	*	9/2005	Ribeiro et al.	D10/78
D518,394 S	*	4/2006	Lipscomb et al.	D10/78

* cited by examiner

Primary Examiner—Antoine D. Davis

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(57) **CLAIM**

The ornamental design for an electrical test instrument, as shown and described.

DESCRIPTION

FIG. **1** is a bottom-front perspective view of a digital electronic test instrument embodying my new design;

FIG. **2** is a top-front perspective view thereof;

FIG. **3** is a front elevation view thereof;

FIG. **4** is a top plan view thereof;

FIG. **5** is a rear elevation view thereof;

FIG. **6** is a bottom plan view thereof;

FIG. **7** is a left side elevation view thereof; and,

FIG. **8** is a right side elevation view thereof.

The broken lines showing instrument controls, display panel and i/o ports in the figures are for illustrative purposes only and form no part of the claimed design.

1 Claim, 3 Drawing Sheets

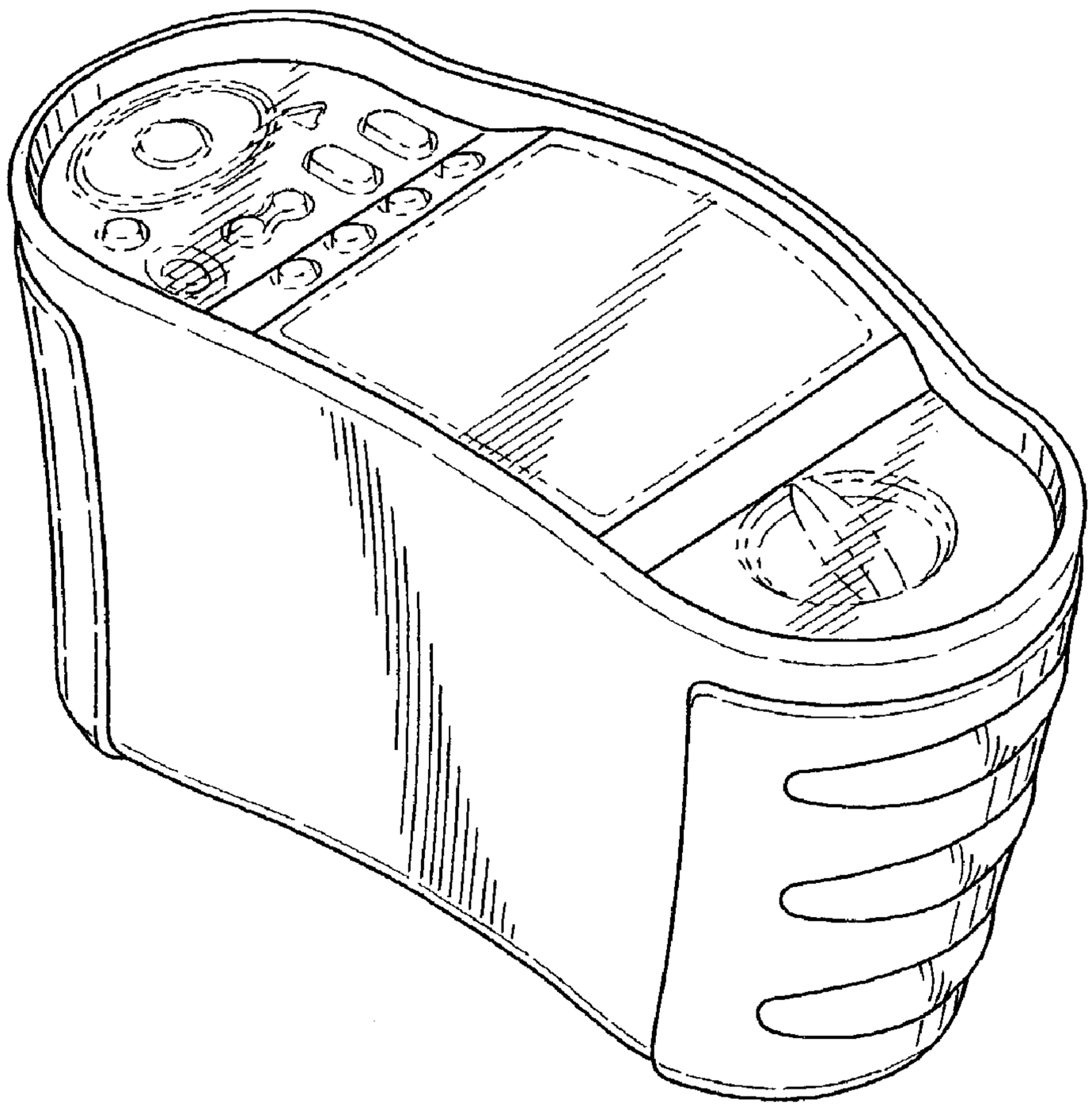

FIG. 1

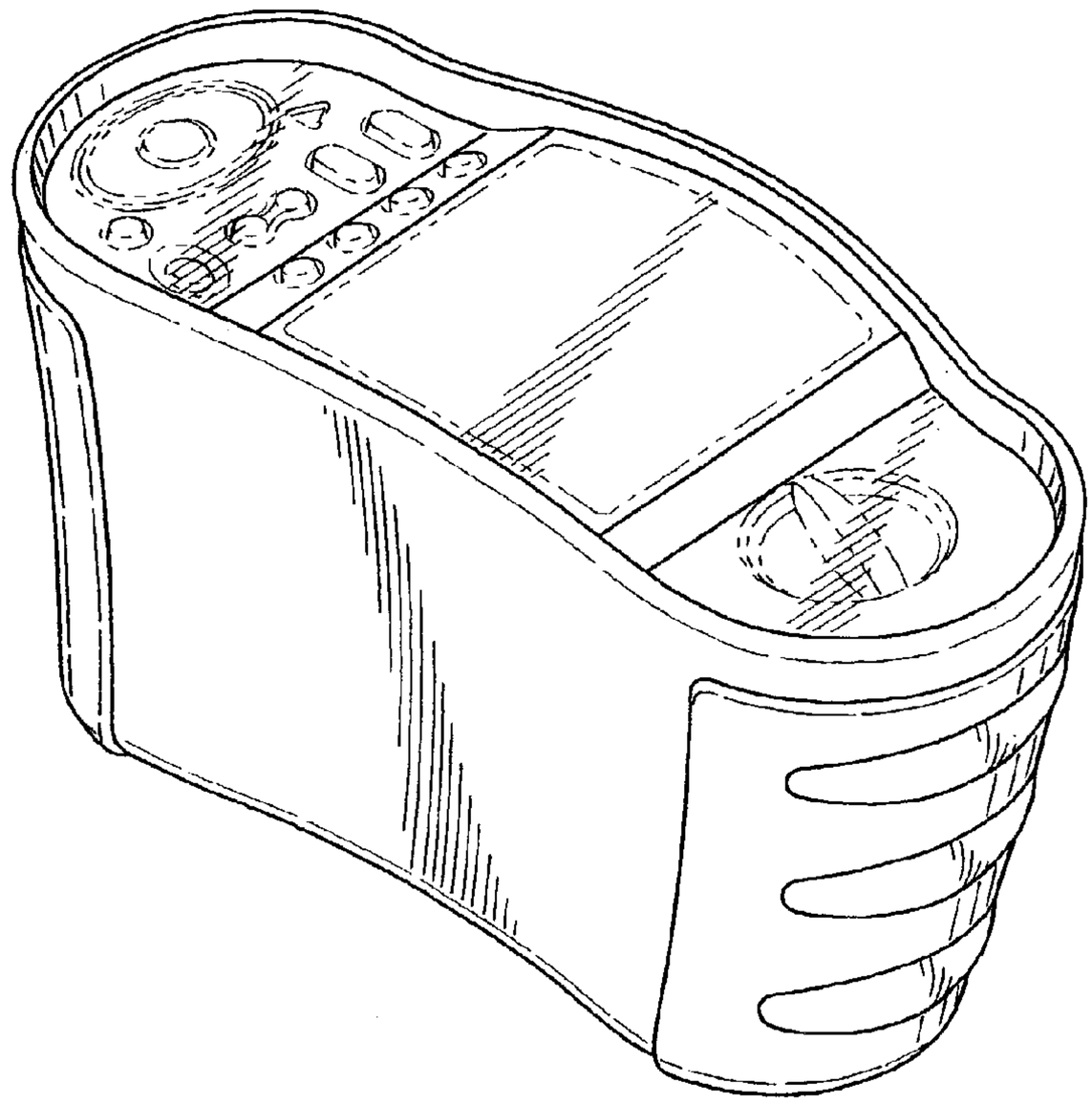

FIG. 2

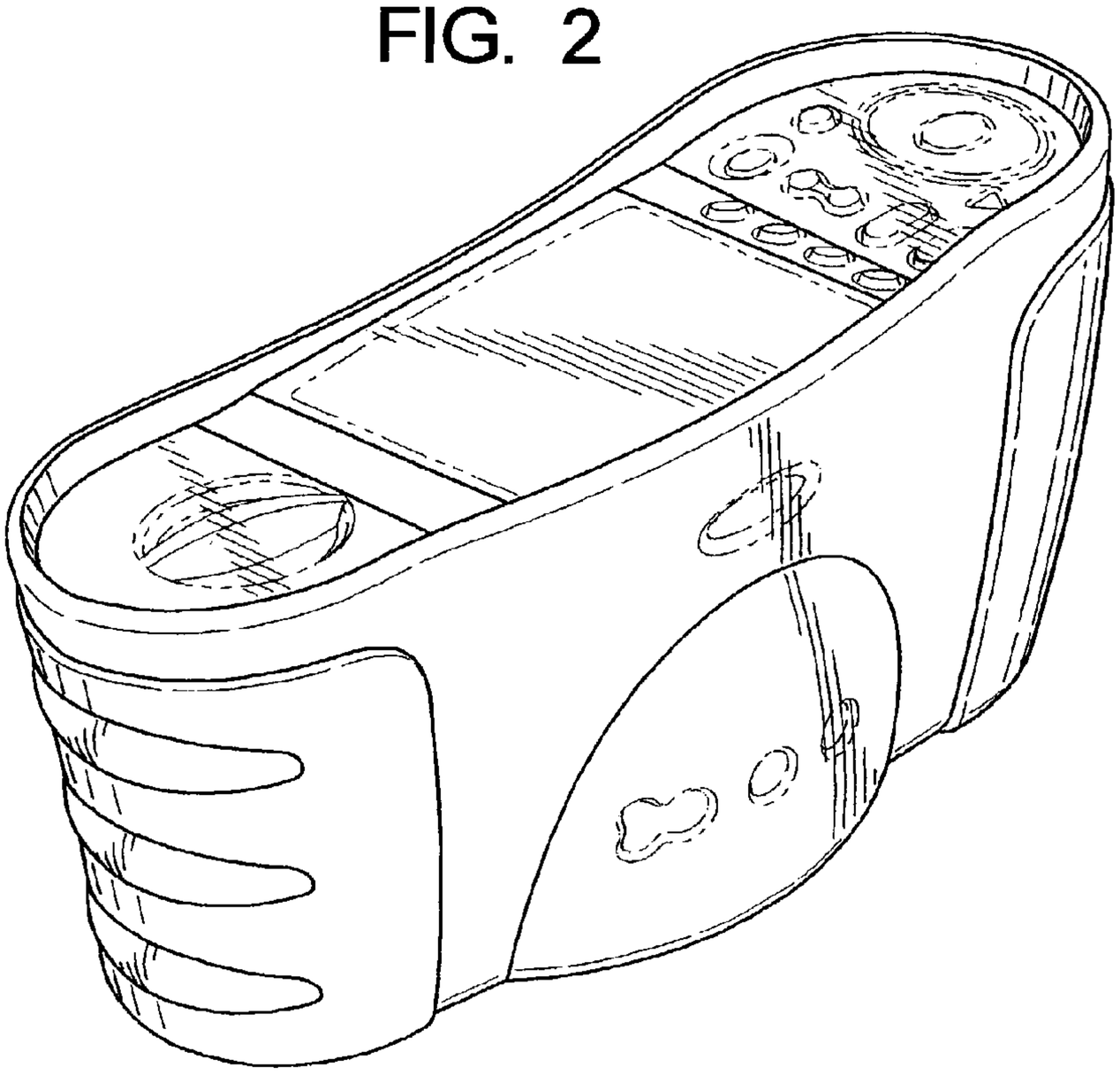

FIG. 3

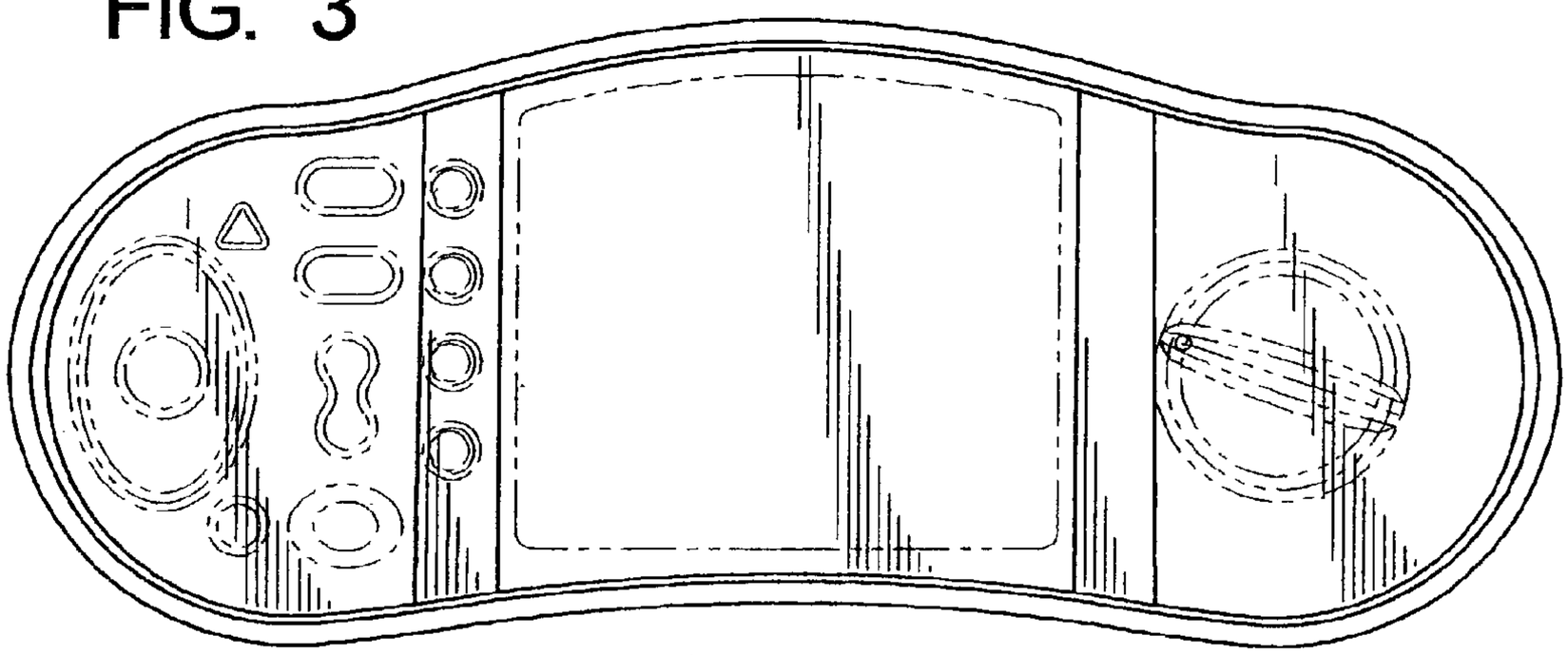

FIG. 4

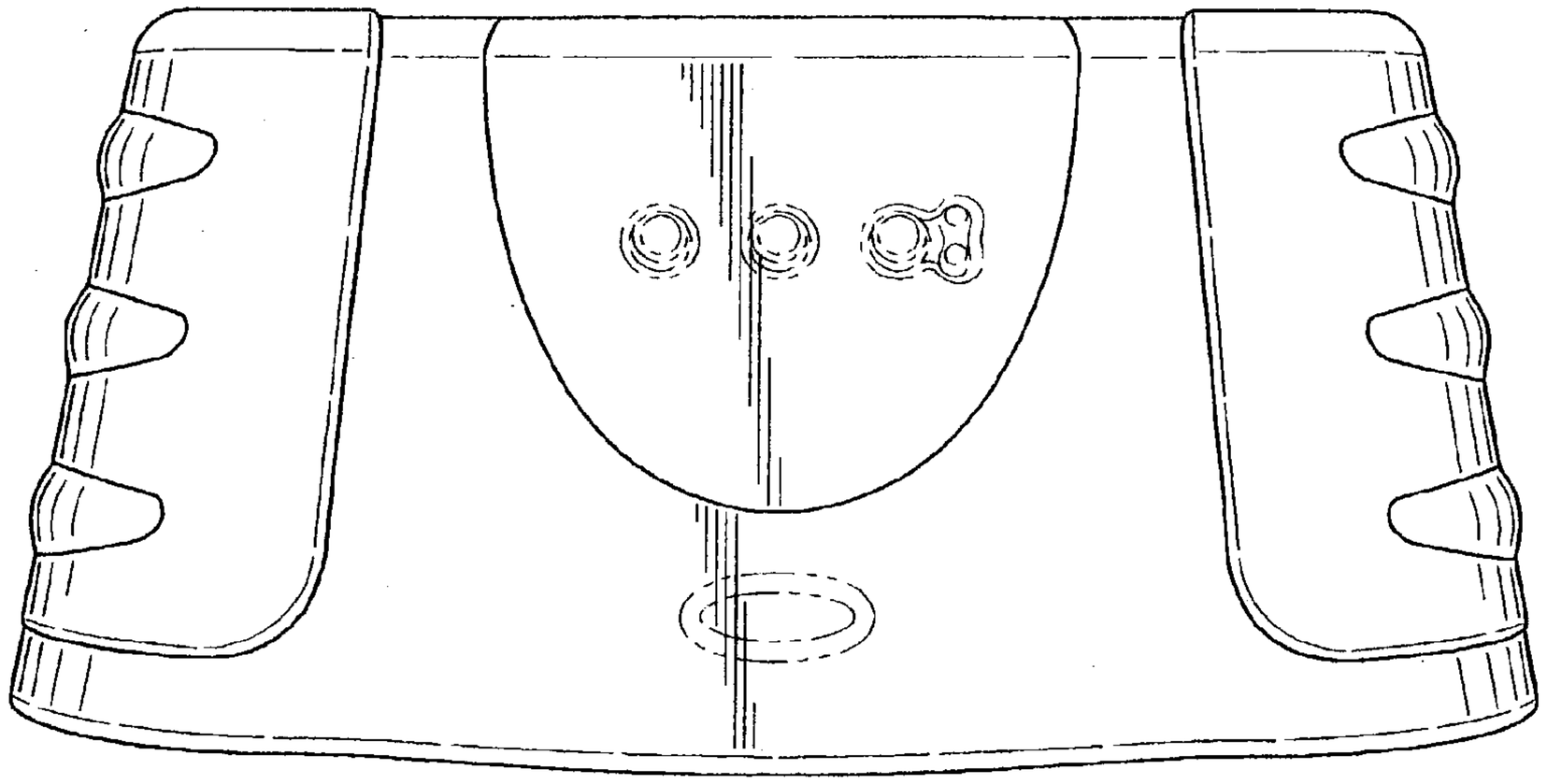

FIG. 5

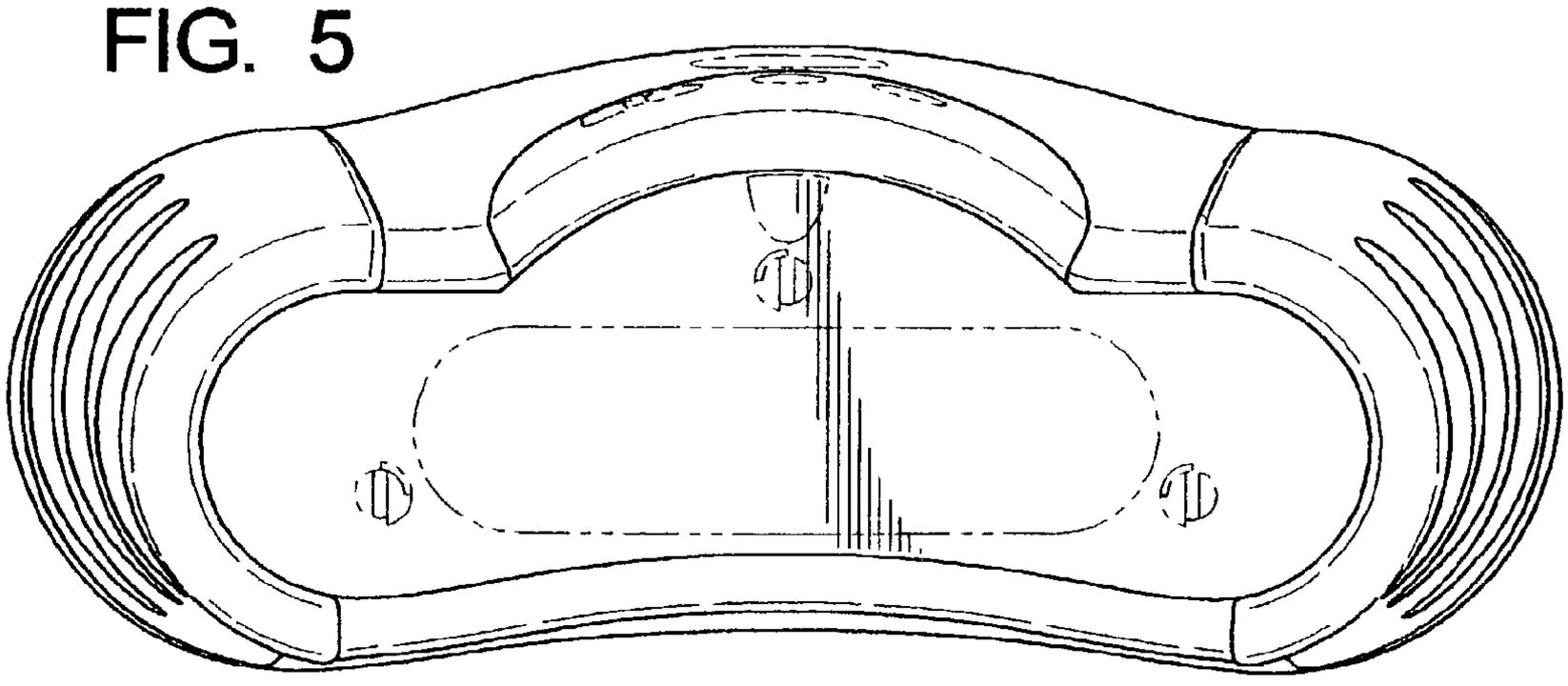

FIG. 6

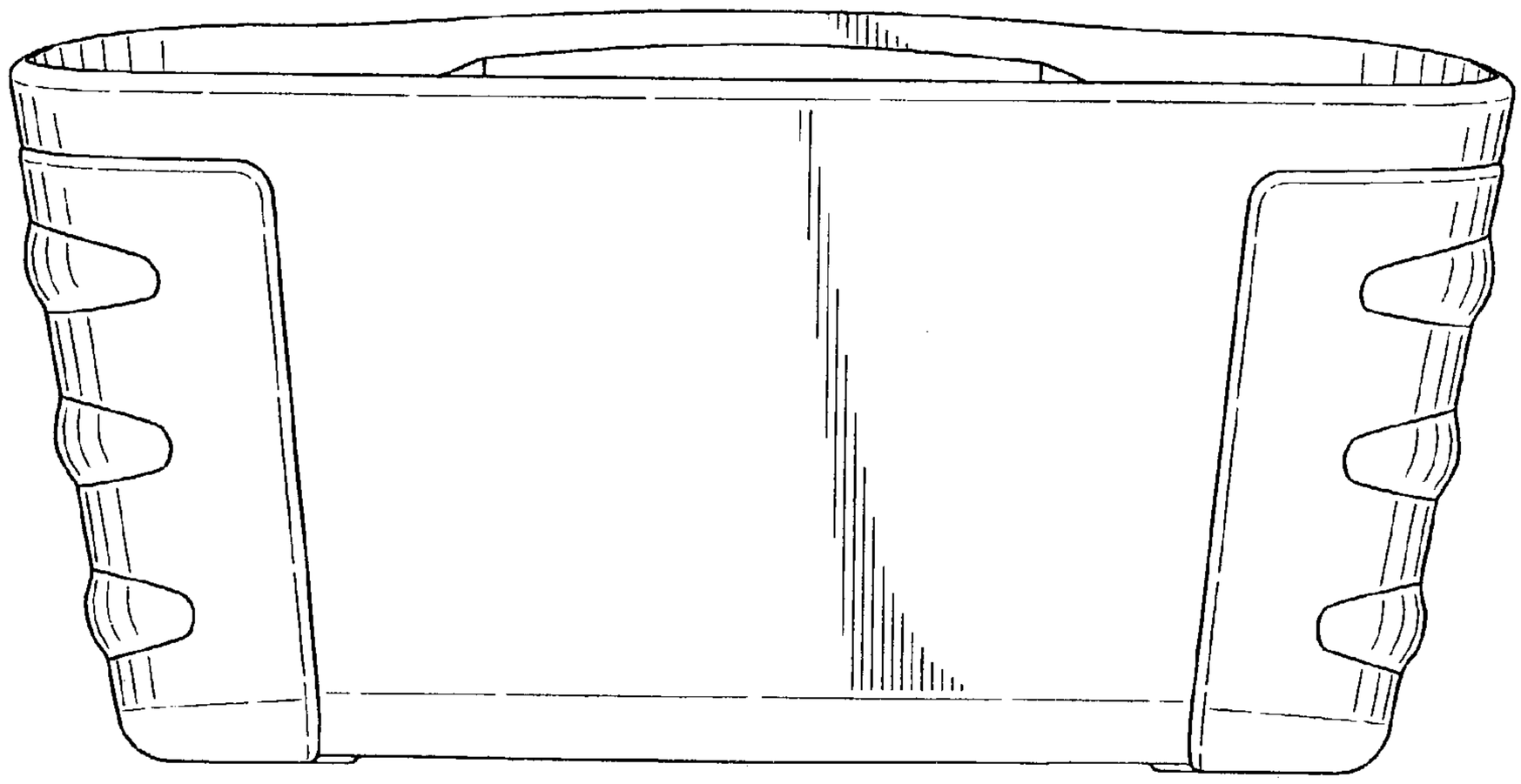

FIG. 7

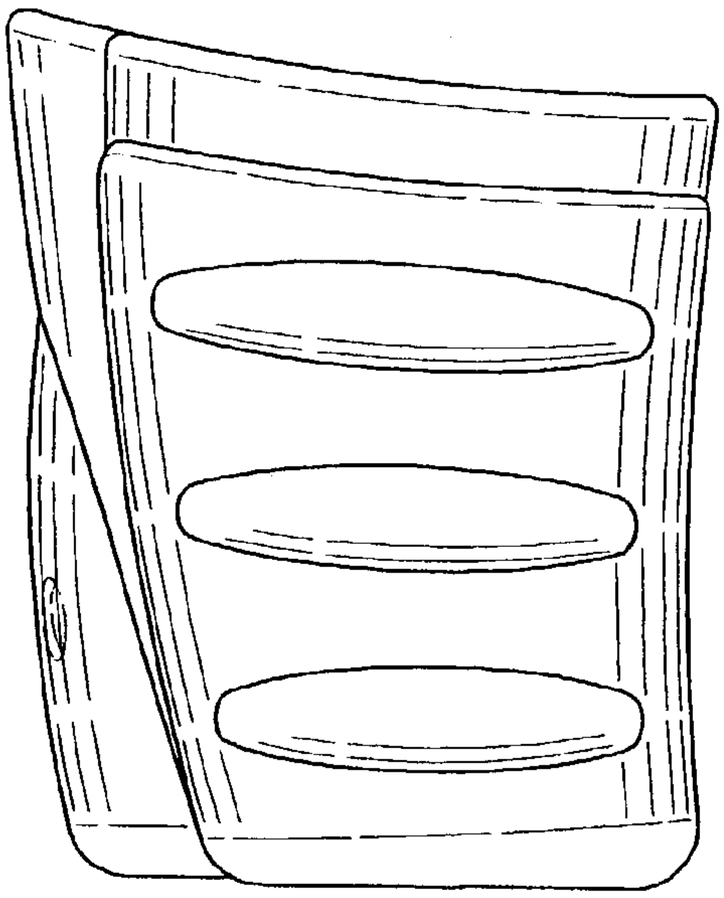

FIG. 8