

US00D540272S

(12) **United States Design Patent** (10) **Patent No.:** **US D540,272 S**
Higashibata (45) **Date of Patent:** **** *Apr. 10, 2007**

- (54) **SEMICONDUCTOR MODULE**
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- (73) Assignee: **Murata Manufacturing Co., Ltd. (JP)**
- (*) Notice: This patent is subject to a terminal disclaimer.
- (**) Term: **14 Years**
- (21) Appl. No.: **29/238,804**
- (22) Filed: **Sep. 22, 2005**
- (30) **Foreign Application Priority Data**
Apr. 18, 2005 (JP) 2005-011529(D)
- (51) **LOC (8) Cl.** **13-03**
- (52) **U.S. Cl.** **D13/182**
- (58) **Field of Classification Search** D13/182;
257/177, 197, 666, 684, 686, 689, 775; 361/820
See application file for complete search history.

- (56) **References Cited**
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(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a semiconductor module showing our new design;
FIG. 2 is a rear view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a left side view thereof; and,
FIG. 6 is a right side view thereof.
The broken lines shown in the drawings are for illustrative purposes only and form no part of the claimed design.

1 Claim, 2 Drawing Sheets

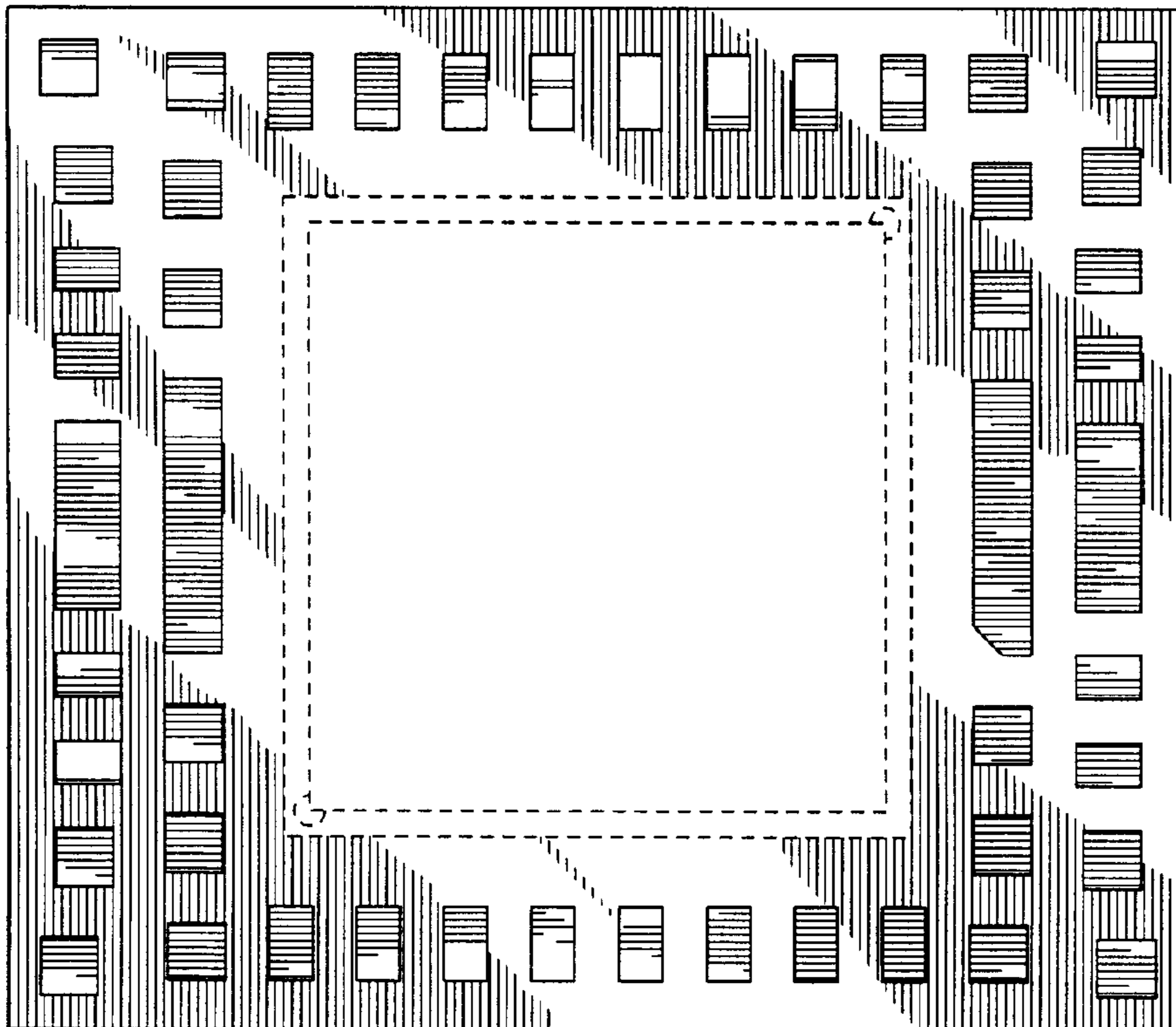


FIG.1

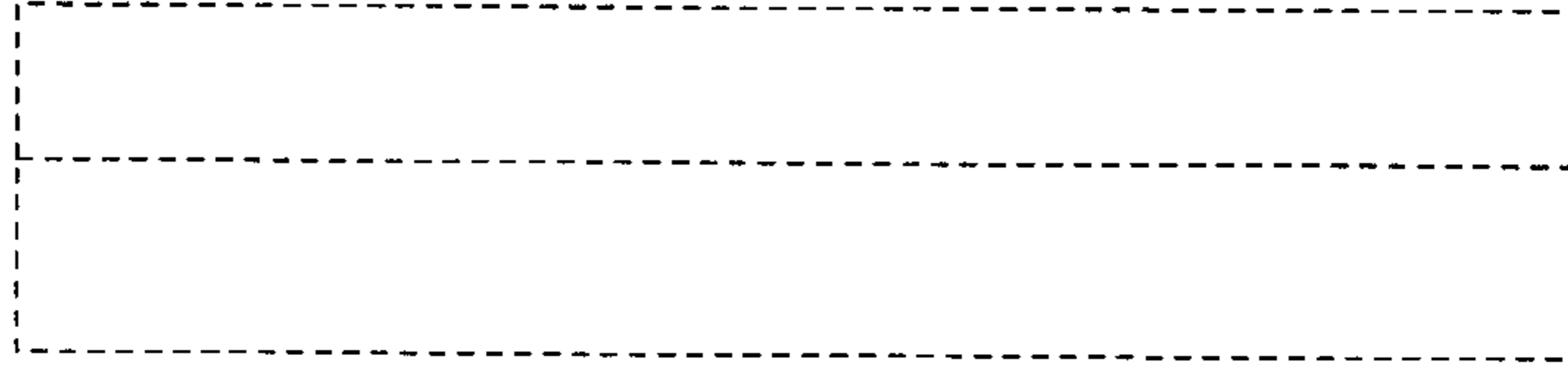


FIG.2

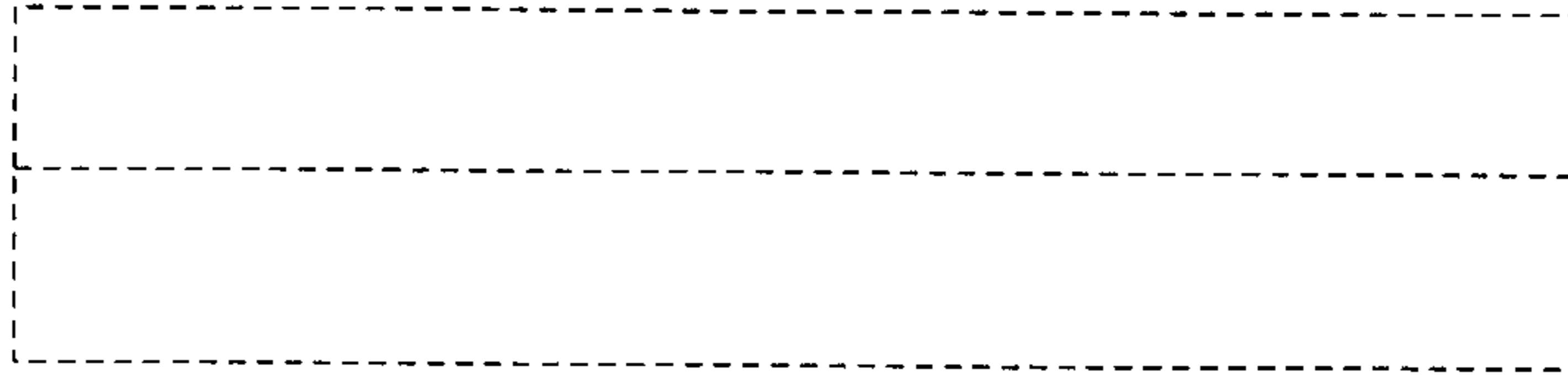


FIG.3

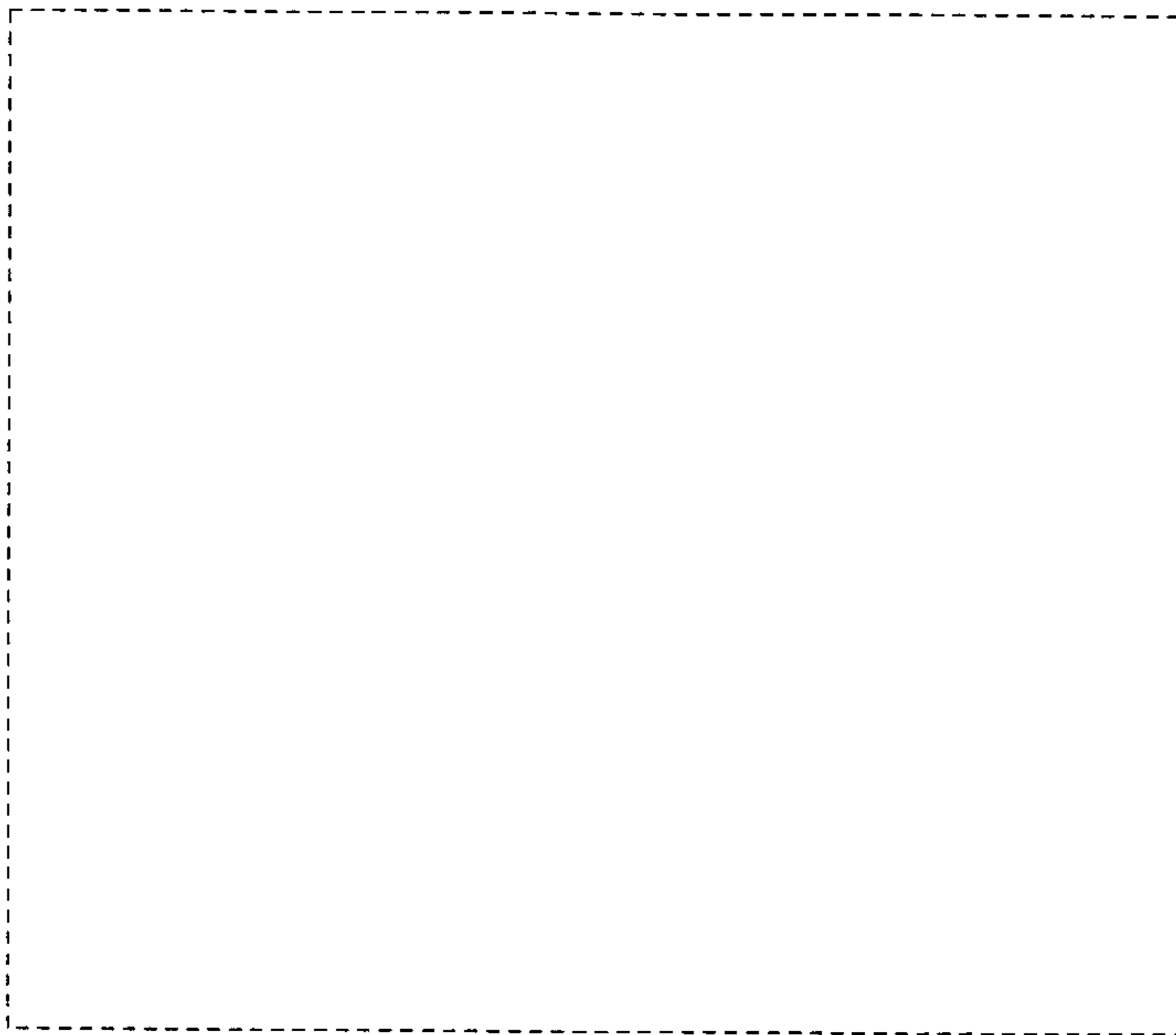


FIG.4

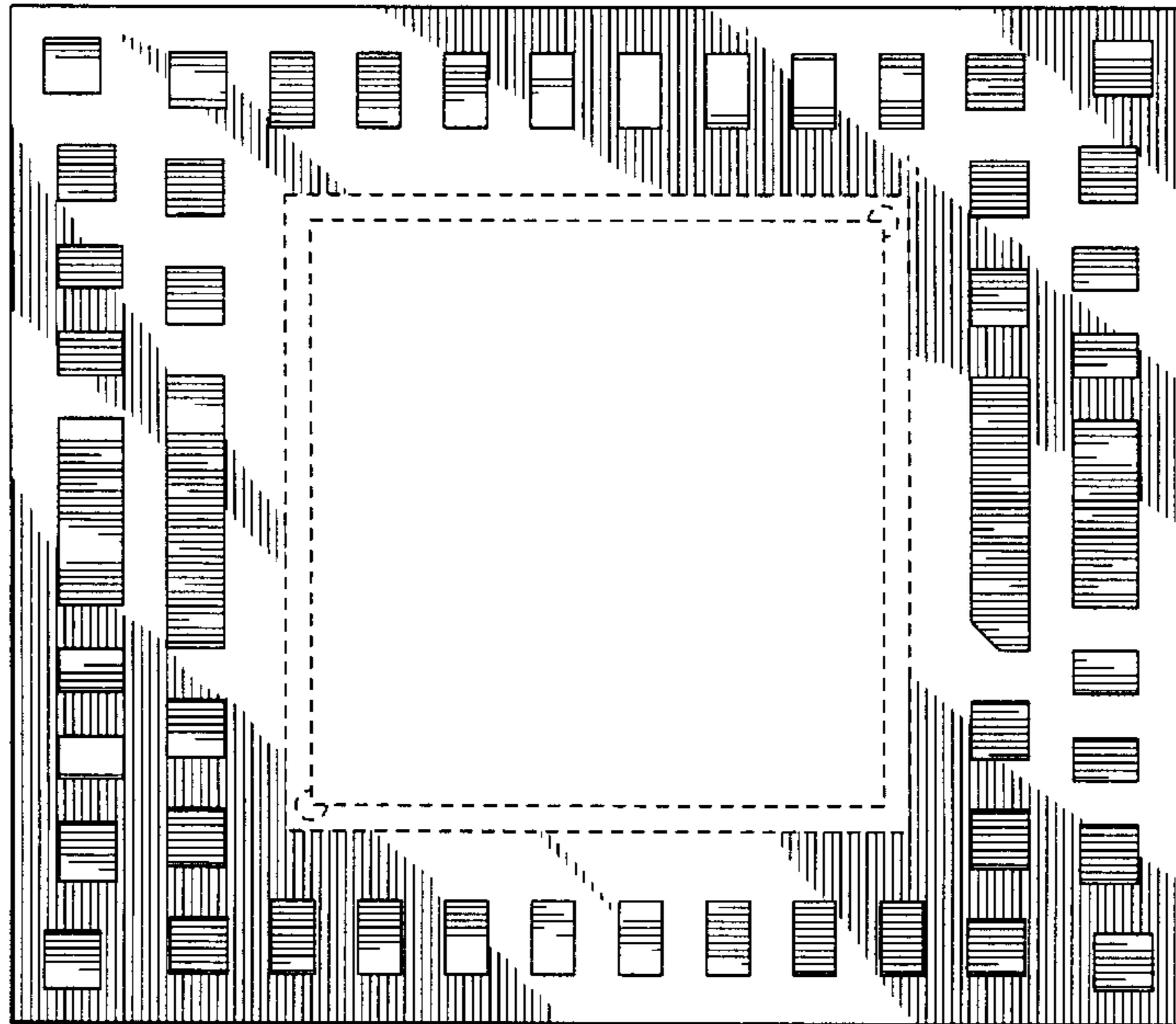


FIG.5

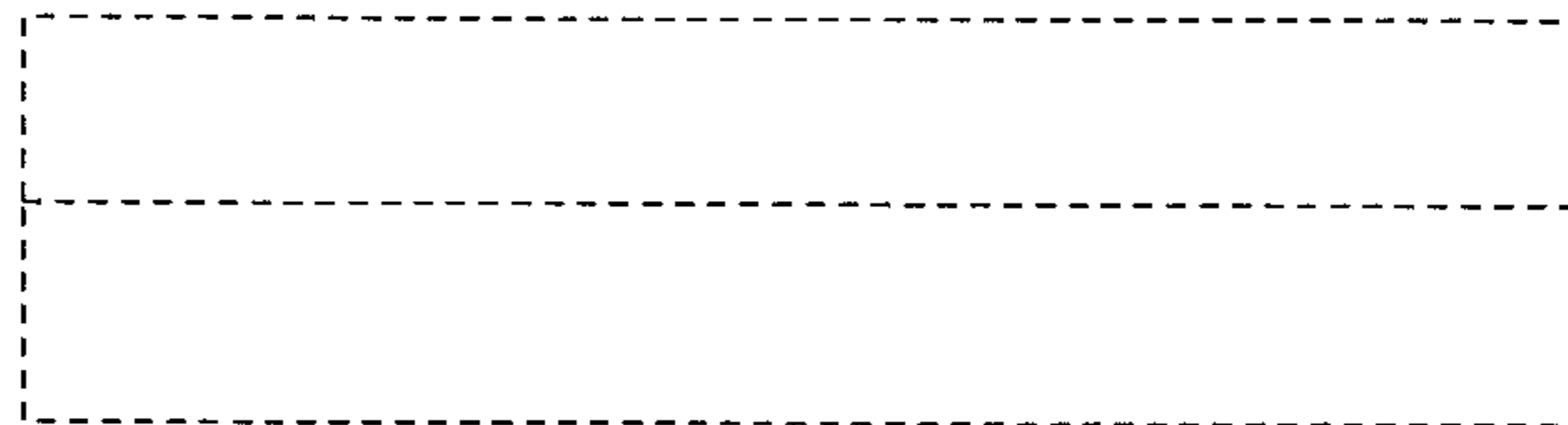


FIG.6

