US00D529000S

(12) United States Design Patent

Ishii

(10) Patent No.: US D529,000 S
(45) Date of Patent: ** Sep. 26, 2006

(54) **INTEGRATED CIRCUIT TAG**

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(73) Assignee: **Riso Kagaku Corporation**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/201,582**

(22) Filed: **Mar. 18, 2004**

(30) **Foreign Application Priority Data**

Sep. 18, 2003 (JP) 2003-027209

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182; 257/E27.114, E27.001; 340/5.91, 572.1, 340/825.49; 361/314, 766, 776, 777; 365/154
See application file for complete search history.

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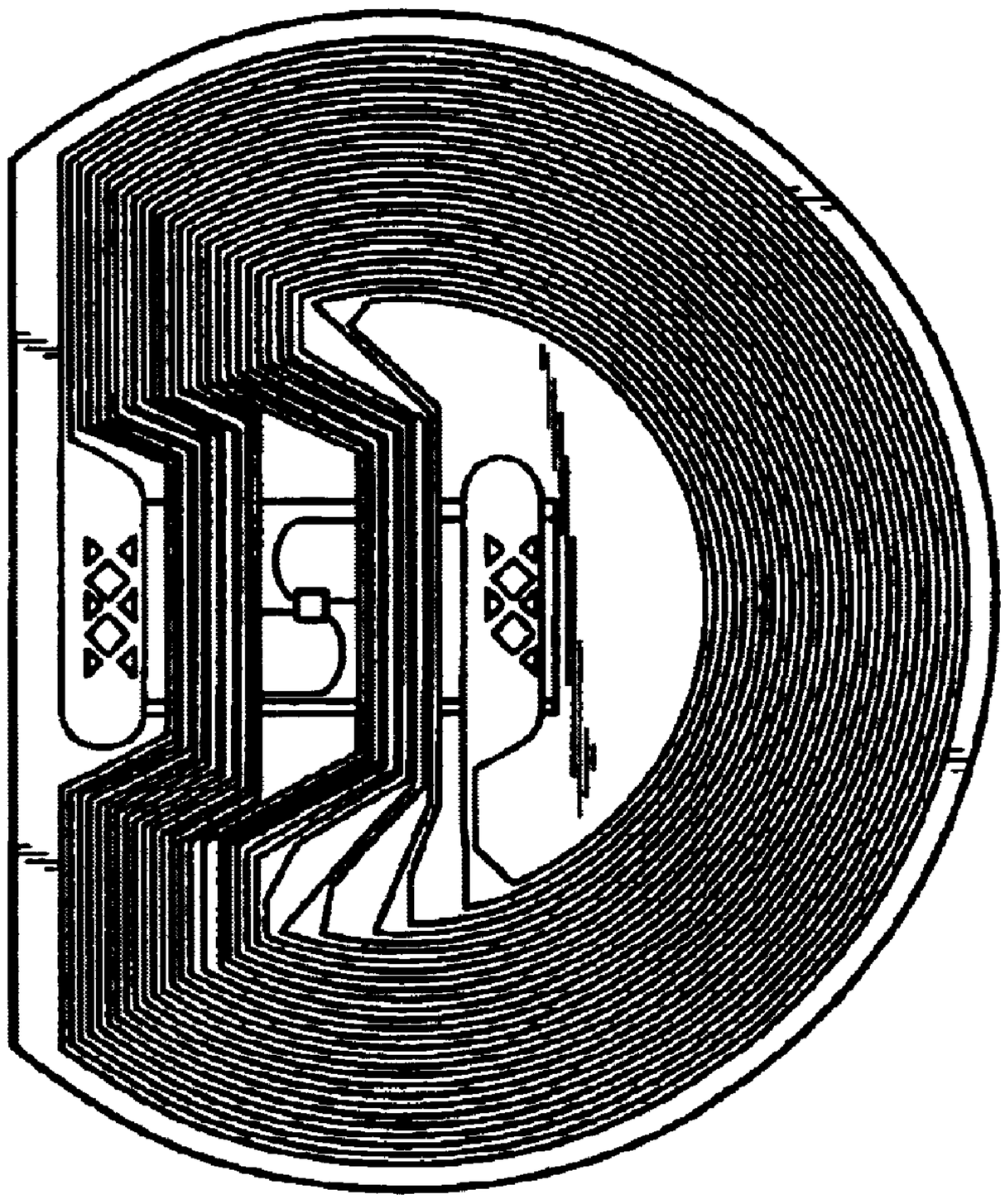
(57) **CLAIM**

The ornamental design for an integrated circuit tag, as shown and described.

DESCRIPTION

FIG. **1** is a front elevational view of and integrated circuit tag showing my new design;
FIG. **2** is a is top plan view thereof;
FIG. **3** is a left side elevational view thereof;
FIG. **4** is a right side elevational view thereof;
FIG. **5** is a rear elevational view thereof; and,
FIG. **6** is a bottom plan view thereof;

1 Claim, 3 Drawing Sheets



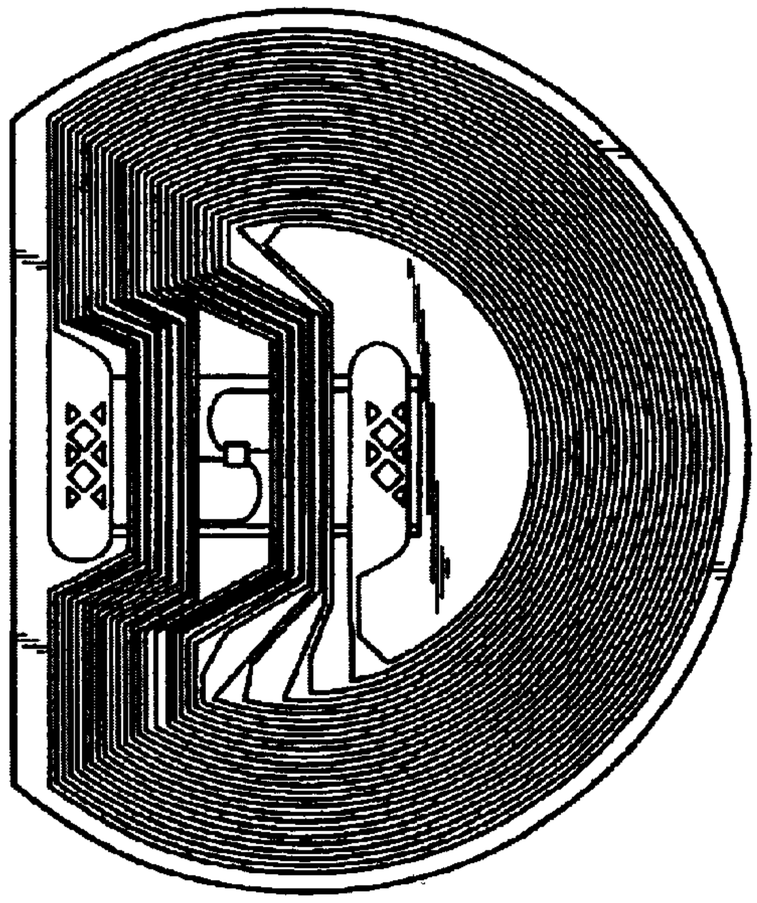


Fig. 1

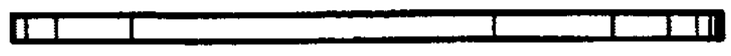


Fig. 2

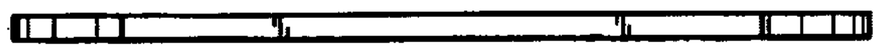


Fig. 3

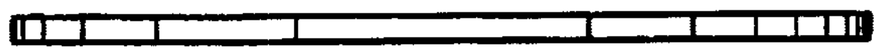


Fig. 4

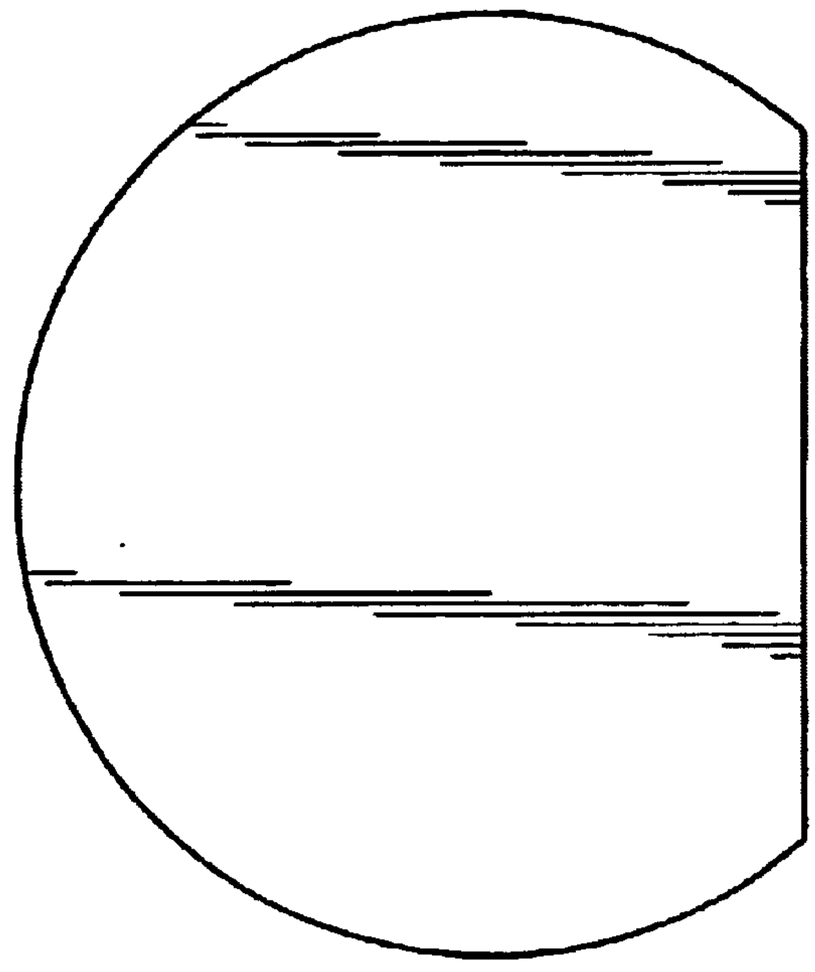


Fig. 5

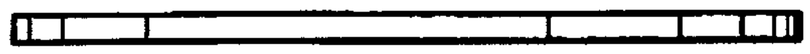


Fig. 6