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(12) United States Design Patent

Nesenoff

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(54) **ELECTRICAL CIRCUITS LAB**

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(**) Term: **14 Years**

(21) Appl. No.: **29/236,810**

(22) Filed: **Aug. 24, 2005**

(51) **LOC (8) Cl.** **19-07**

(52) **U.S. Cl.** **D19/62**

(58) **Field of Classification Search** D19/59–64; D13/184; 434/224, 301, 379–380
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

1,271,641 A * 7/1918 Werwath 434/224
D176,574 S * 1/1956 Brerdan et al. D19/62
3,277,589 A * 10/1966 Berdan et al. 434/224
D264,351 S * 5/1982 Dresens D19/62
4,332,568 A * 6/1982 Hyink 434/224
D304,957 S * 12/1989 Melone D19/62
D508,265 S * 8/2005 Nesenoff D19/59

* cited by examiner

Primary Examiner—Robert A. Delehanty
Assistant Examiner—Mark Cavanna

(57) **CLAIM**

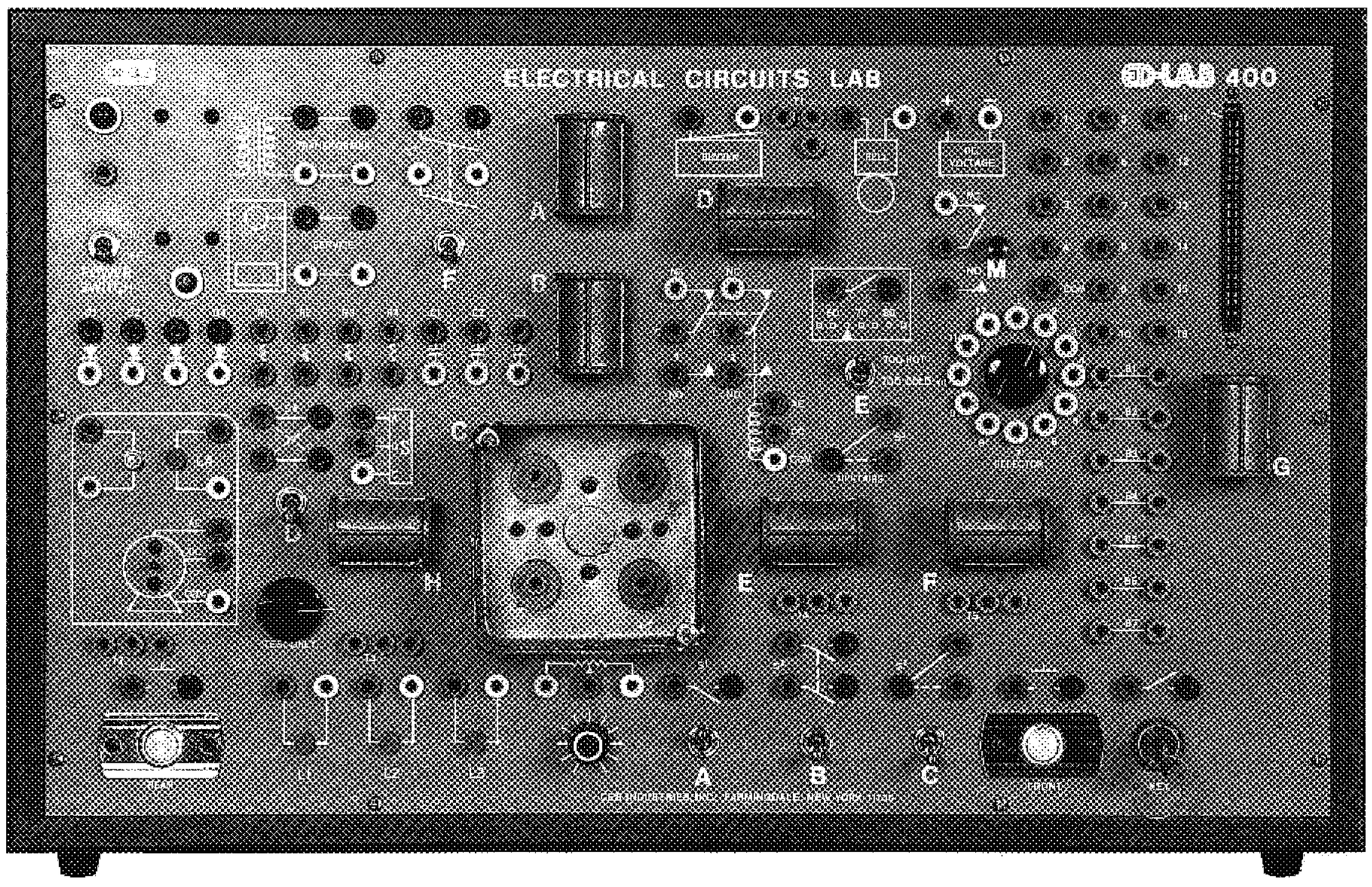
The ornamental design for a electrical circuits lab, as shown.

DESCRIPTION

FIG. **1** is a front elevation view of the electrical circuits lab showing my new design; and,

FIG. **2** is a right front perspective view thereof.

1 Claim, 2 Drawing Sheets



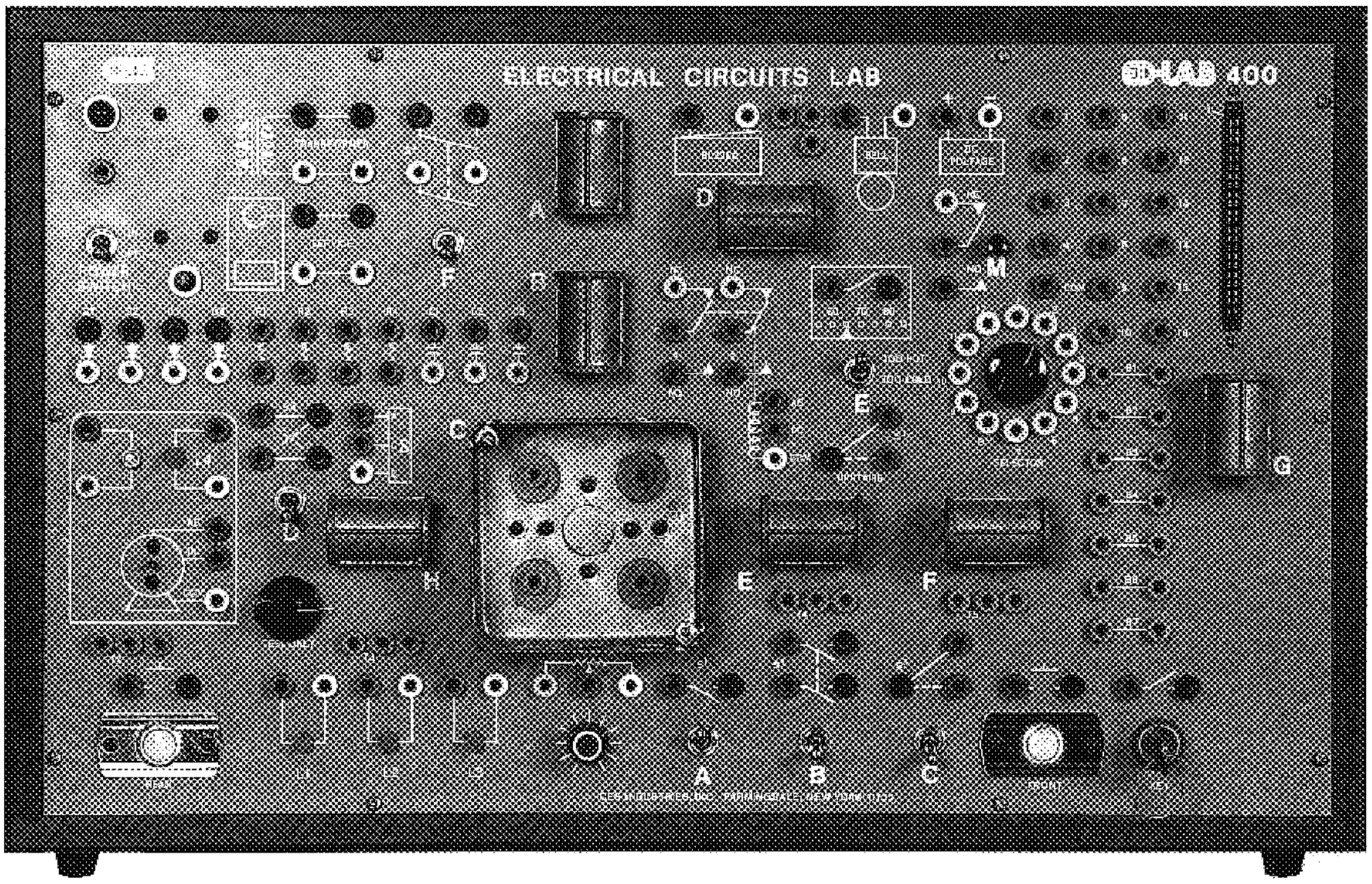


FIG. 1

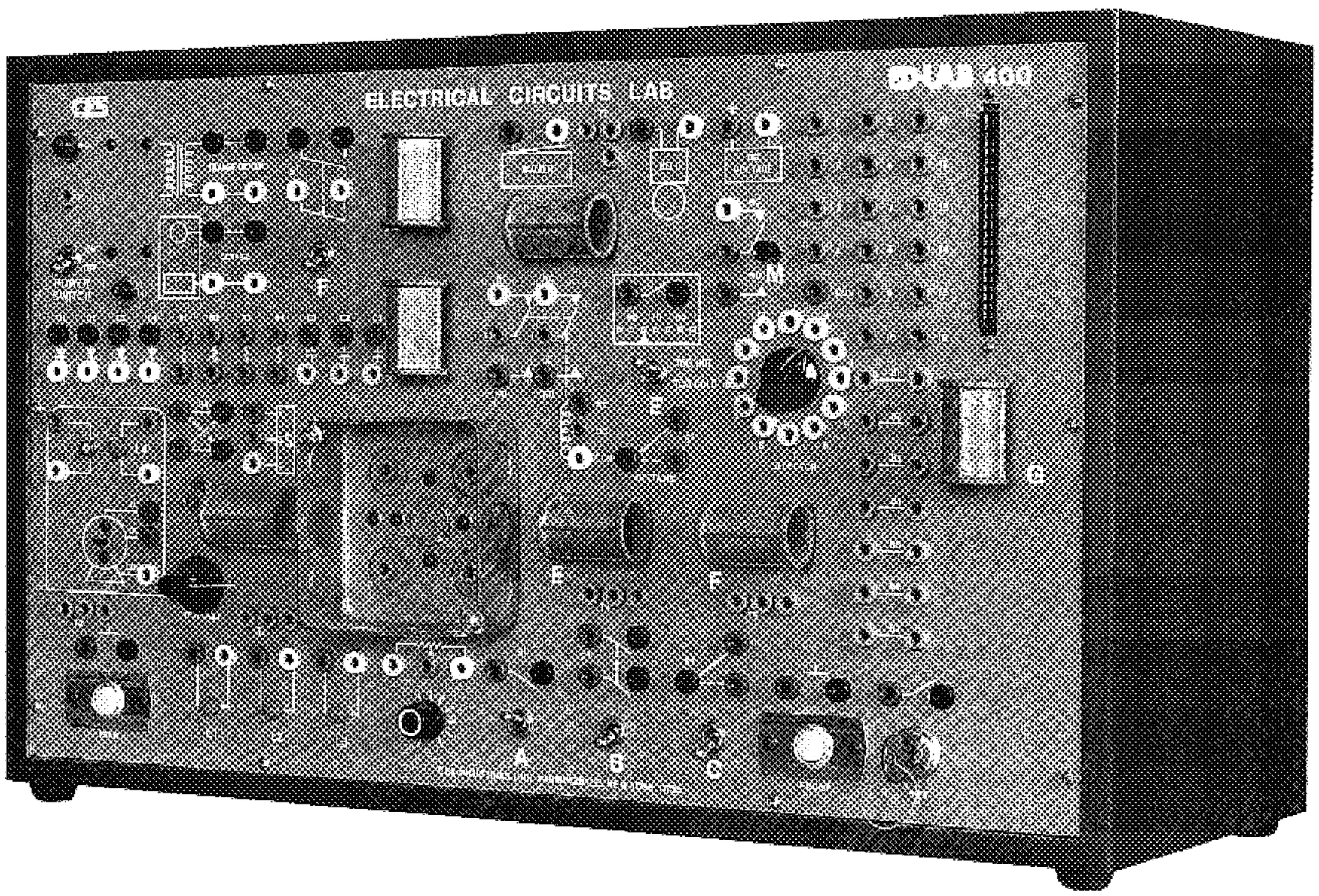


FIG. 2