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(12) **United States Design Patent**
Mizukoshi

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(45) **Date of Patent:** **** Jun. 13, 2006**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **Kabushiki Kaisha Toshiba** (JP)

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JP D1166594 3/2003
JP D1166916 3/2003

(**) Term: **14 Years**

* cited by examiner

(21) Appl. No.: **29/217,555**

Primary Examiner—Stella Reid
Assistant Examiner—Selina Sikder

(22) Filed: **Nov. 19, 2004**

(74) *Attorney, Agent, or Firm*—Banner & Witocoff, Ltd.

(30) **Foreign Application Priority Data**

Sep. 9, 2004 (JP) 2004-027498

(57) **CLAIM**

(51) **LOC (8) Cl.** **13-03**

The ornamental design for a semiconductor device, as shown and described.

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
174/52.1, 255, 256; 257/676, 678, 691; 361/760
See application file for complete search history.

DESCRIPTION

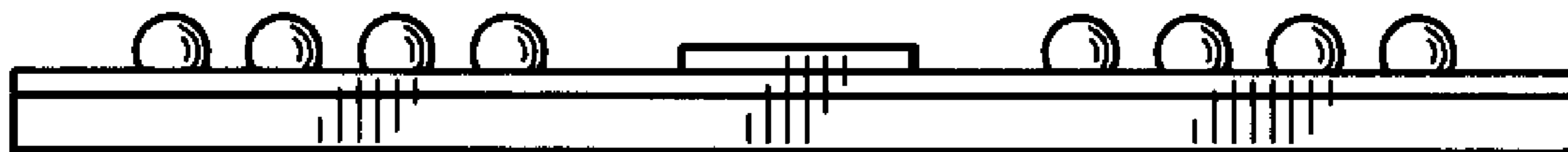
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FIG. 1 is a top plan view of a semiconductor device, showing my new design; the opposite side being a mirror image thereof;
FIG. 2 is a front elevational view thereof;
FIG. 3 is a right side elevational view thereof; the opposite side being a mirror image thereof;
FIG. 4 is a rear elevational view thereof; and,
FIG. 5 is an enlarged fragmented rear elevational view thereof, taken along the line 5—5 in FIG. 2.

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1 Claim, 3 Drawing Sheets



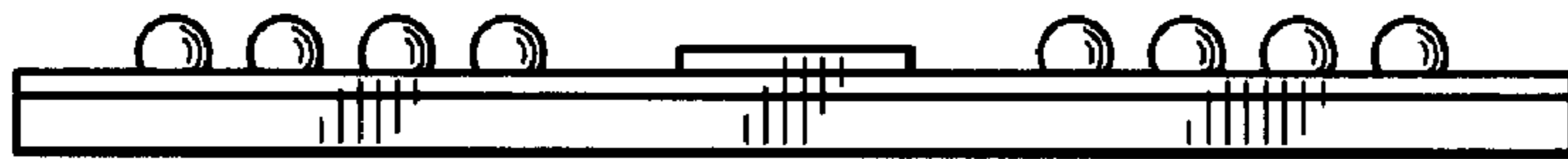


Fig. 1

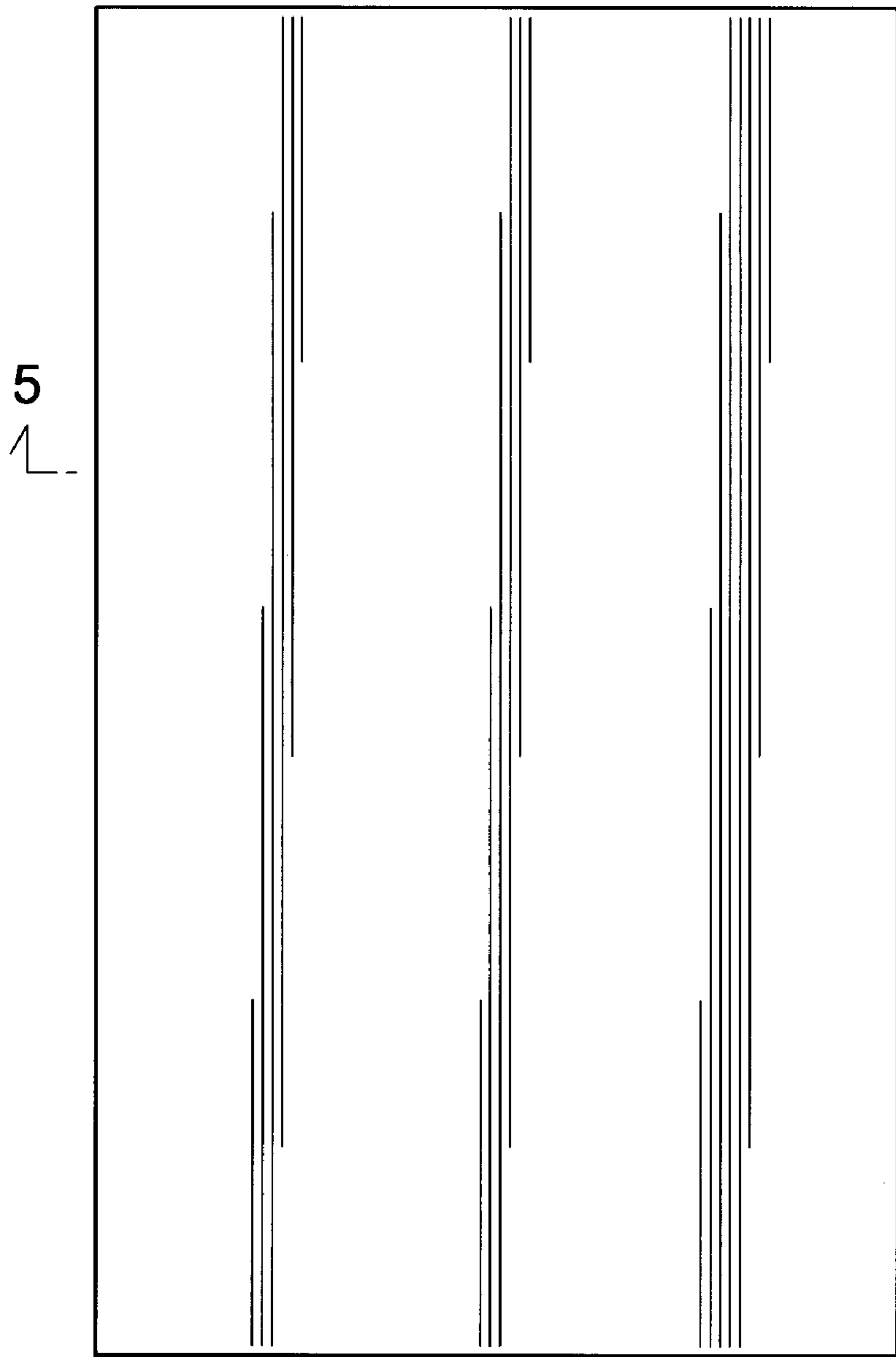


Fig. 2

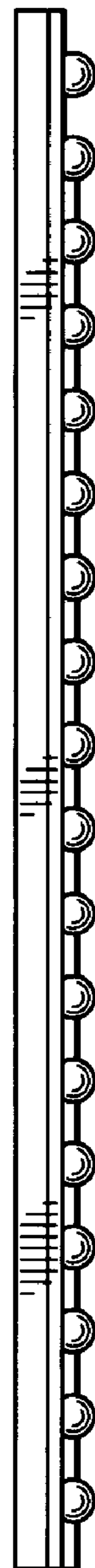


Fig. 3

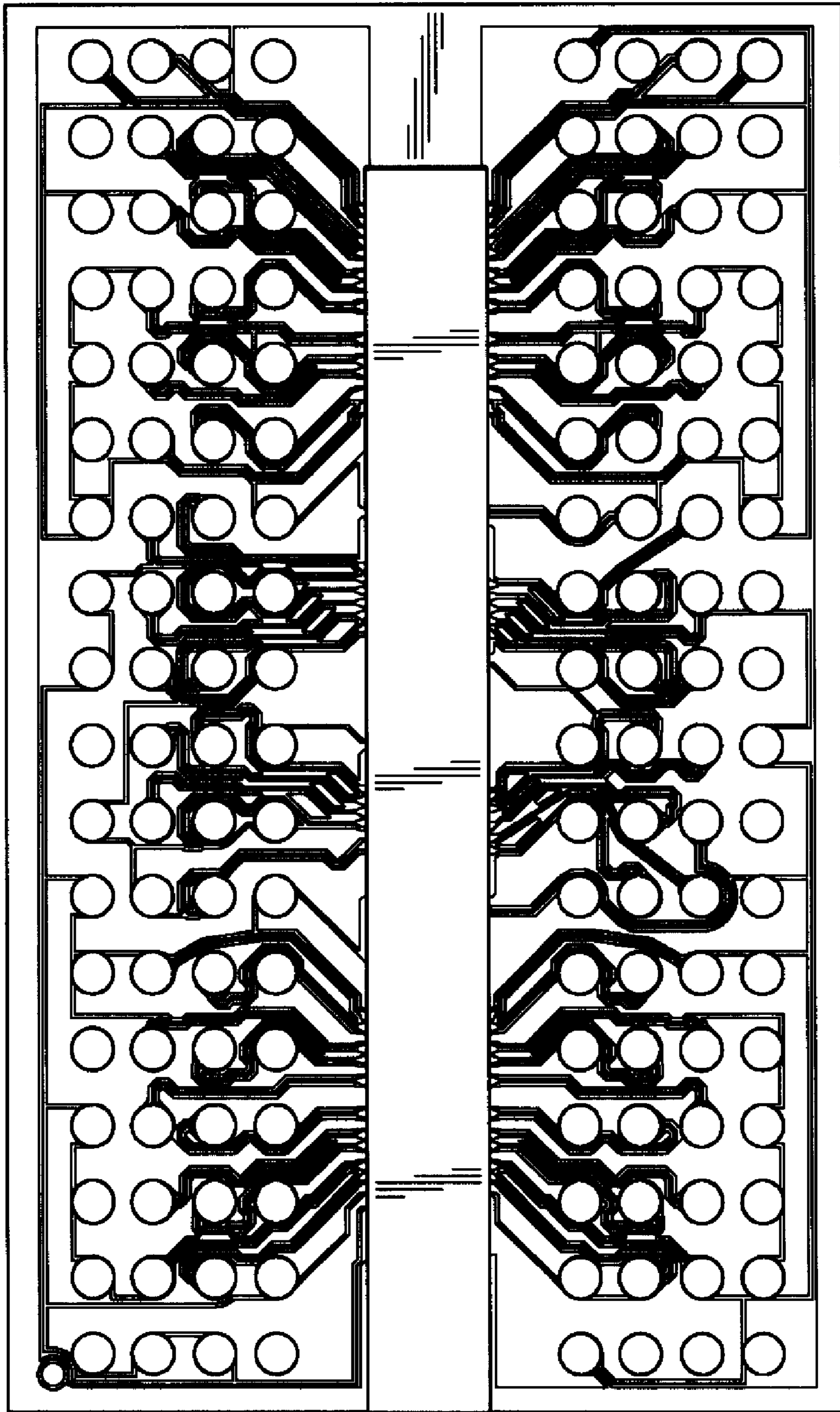


Fig.4

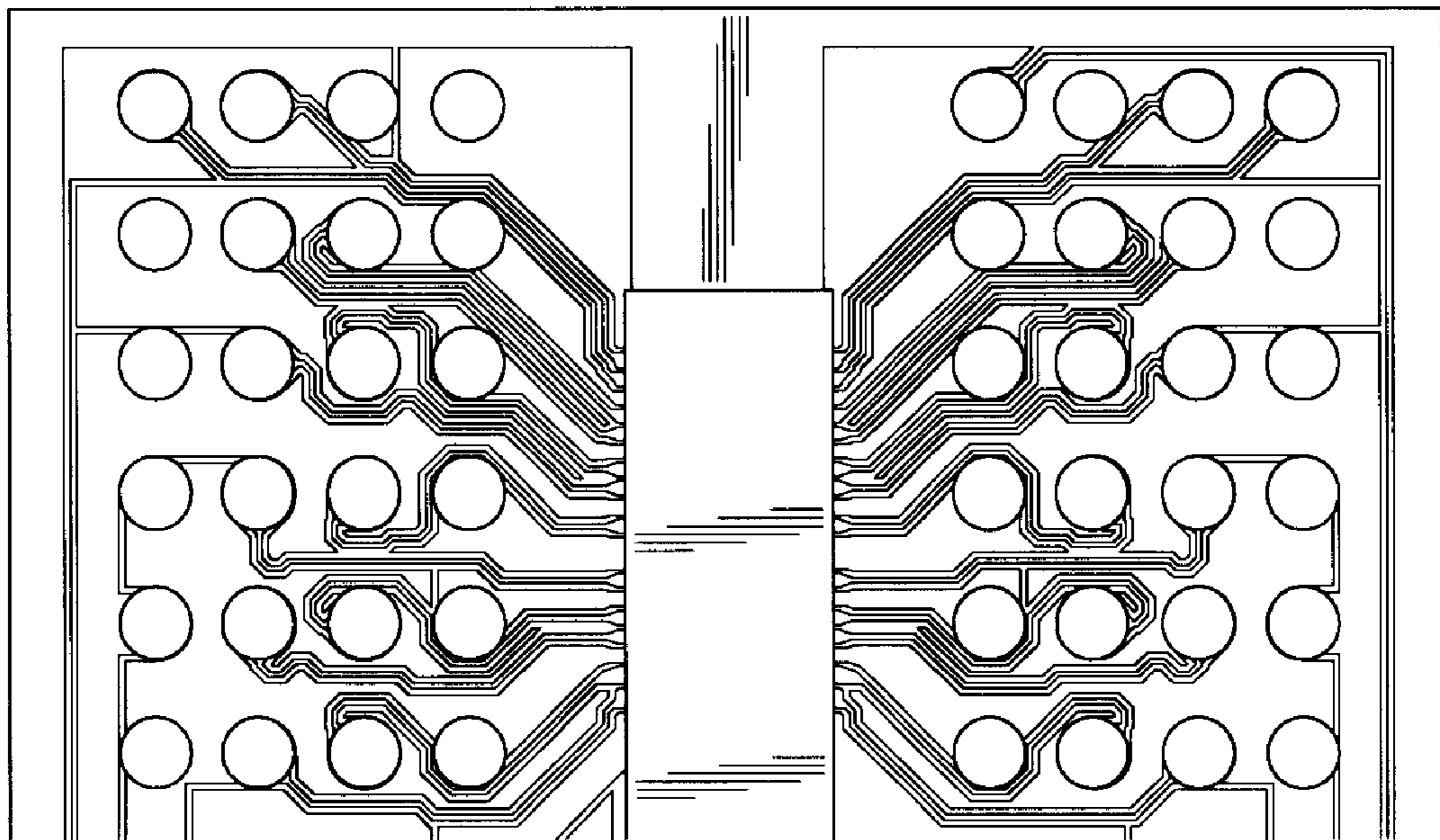


Fig.5