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(12) **United States Design Patent**
Ishii et al.

(10) **Patent No.:** **US D520,467 S**

(45) **Date of Patent:** **** May 9, 2006**

(54) **PROCESS TUBE FOR SEMICONDUCTOR
DEVICE MANUFACTURING APPARATUS**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

Nov. 4, 2003 (JP) 2003-032507

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
117/102; 118/715, 725; 414/935-941
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a process tube for semiconductor device manufacturing apparatus, as shown and described.

DESCRIPTION

FIG. 1 is an isometric view of a process tube for semiconductor device manufacturing apparatus of the present invention;
 FIG. 2 is a front view thereof;
 FIG. 3 is a rear view thereof;
 FIG. 4 is a left side view thereof;
 FIG. 5 is a right side view thereof;
 FIG. 6 is a top view thereof;
 FIG. 7 is a bottom view thereof;
 FIG. 8 is a sectional view along line 8—8 shown in FIG. 6;
 FIG. 9 is a sectional view along line 9—9 shown in FIG. 6;
 FIG. 10 is a sectional view along line 10—10 shown in FIG. 6; and,
 FIG. 11 is a sectional view along line 11—11 shown in FIG. 2.

1 Claim, 9 Drawing Sheets

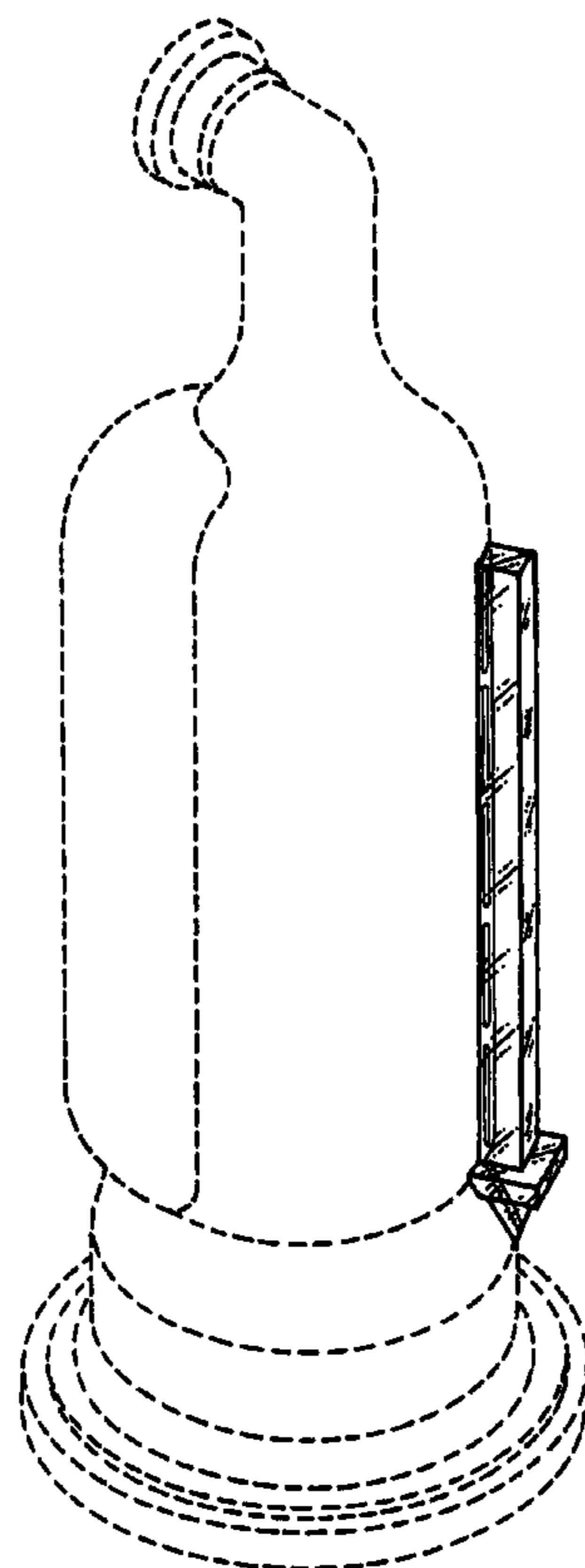


FIG. 1

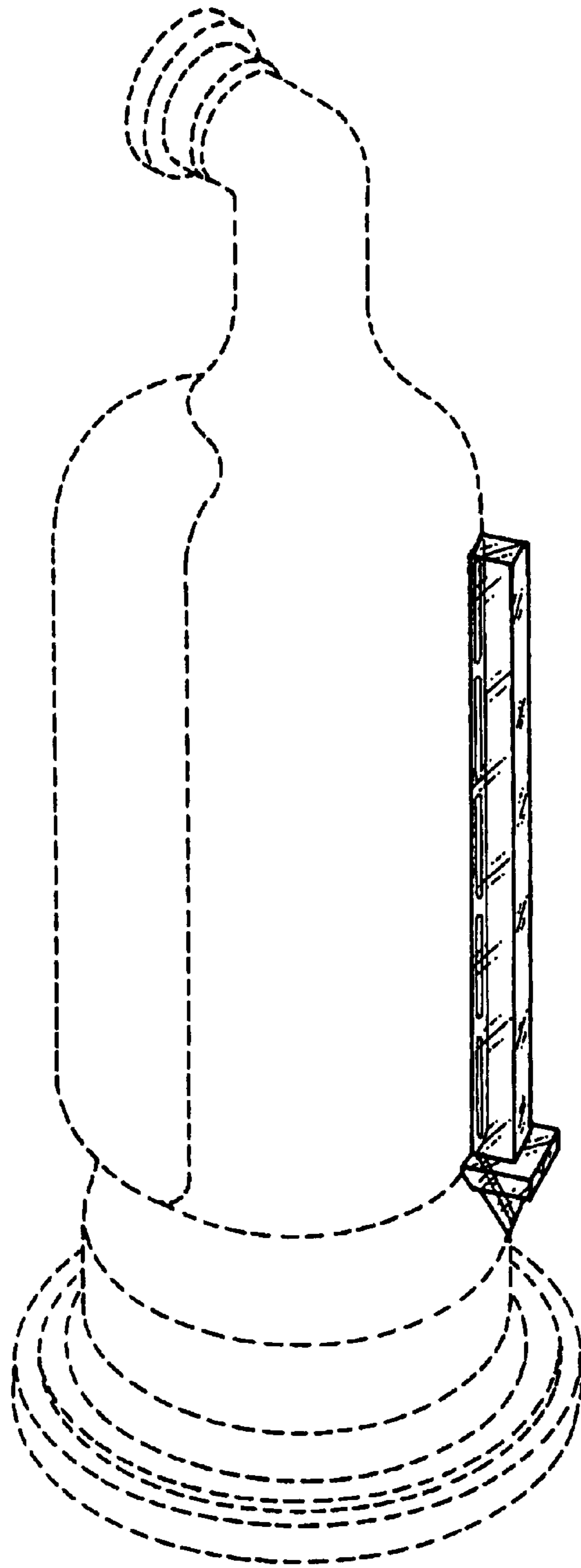


FIG. 2

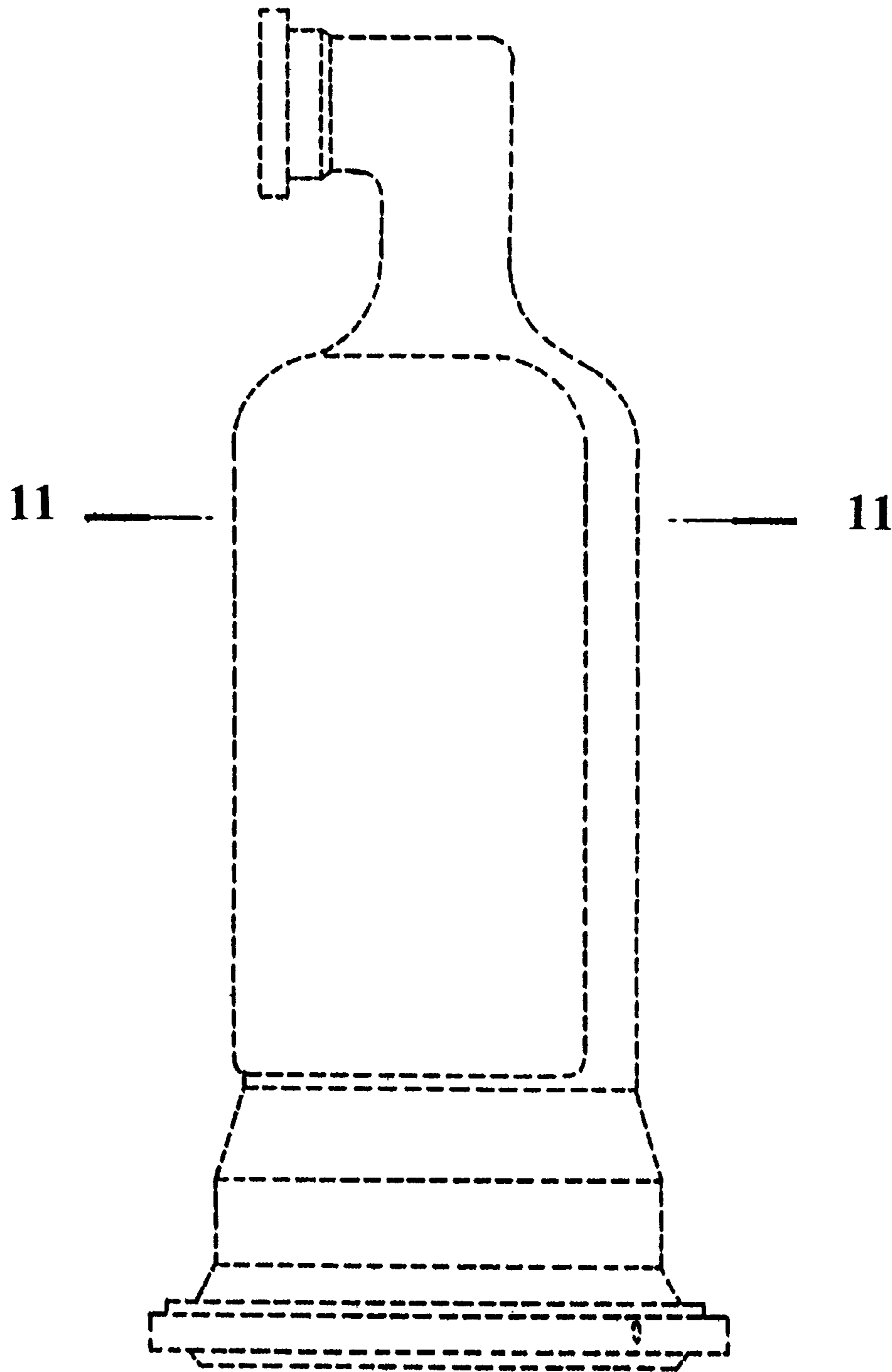


FIG. 3

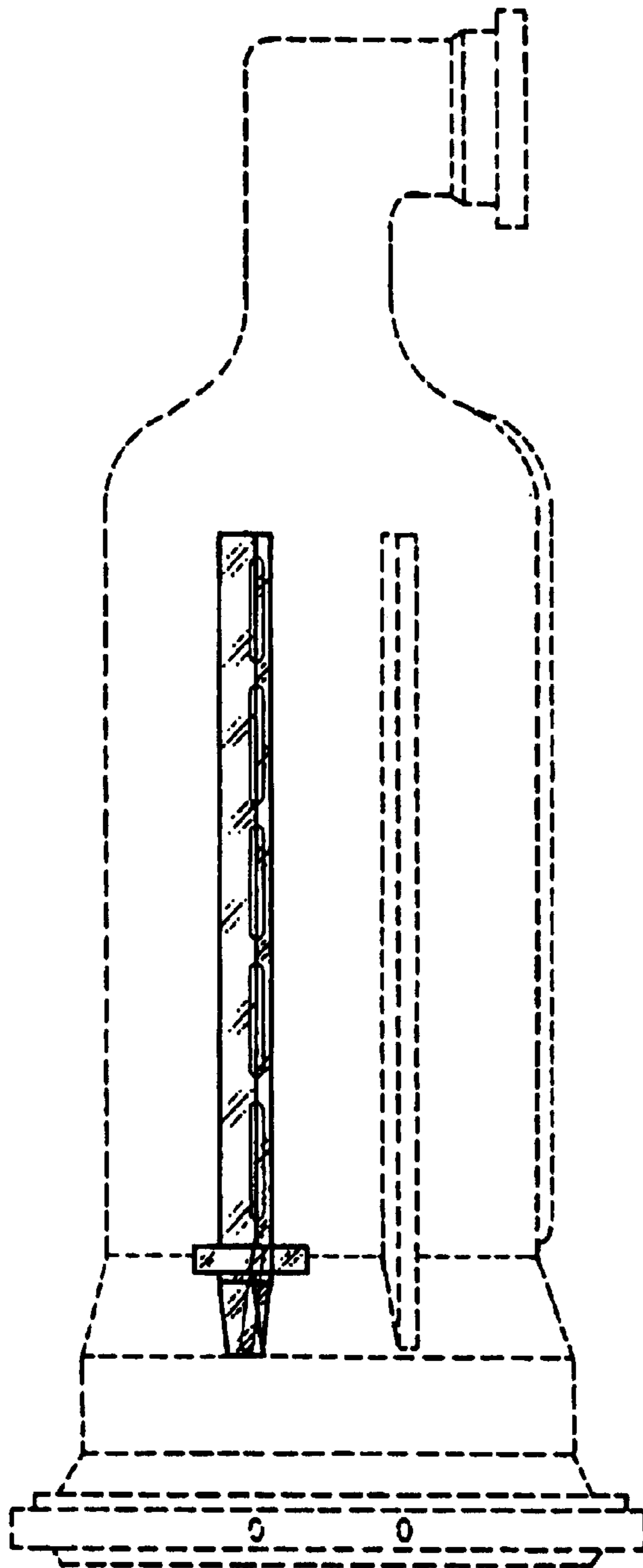


FIG. 4

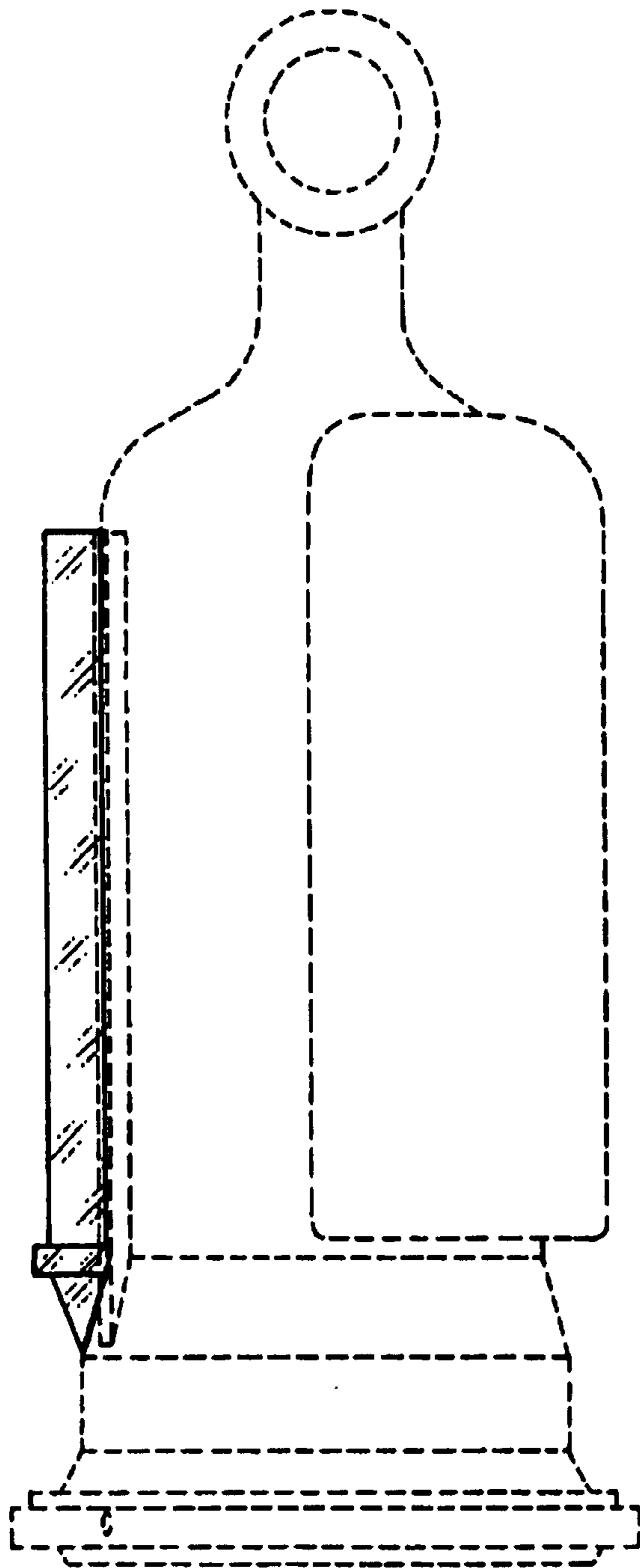


FIG. 5

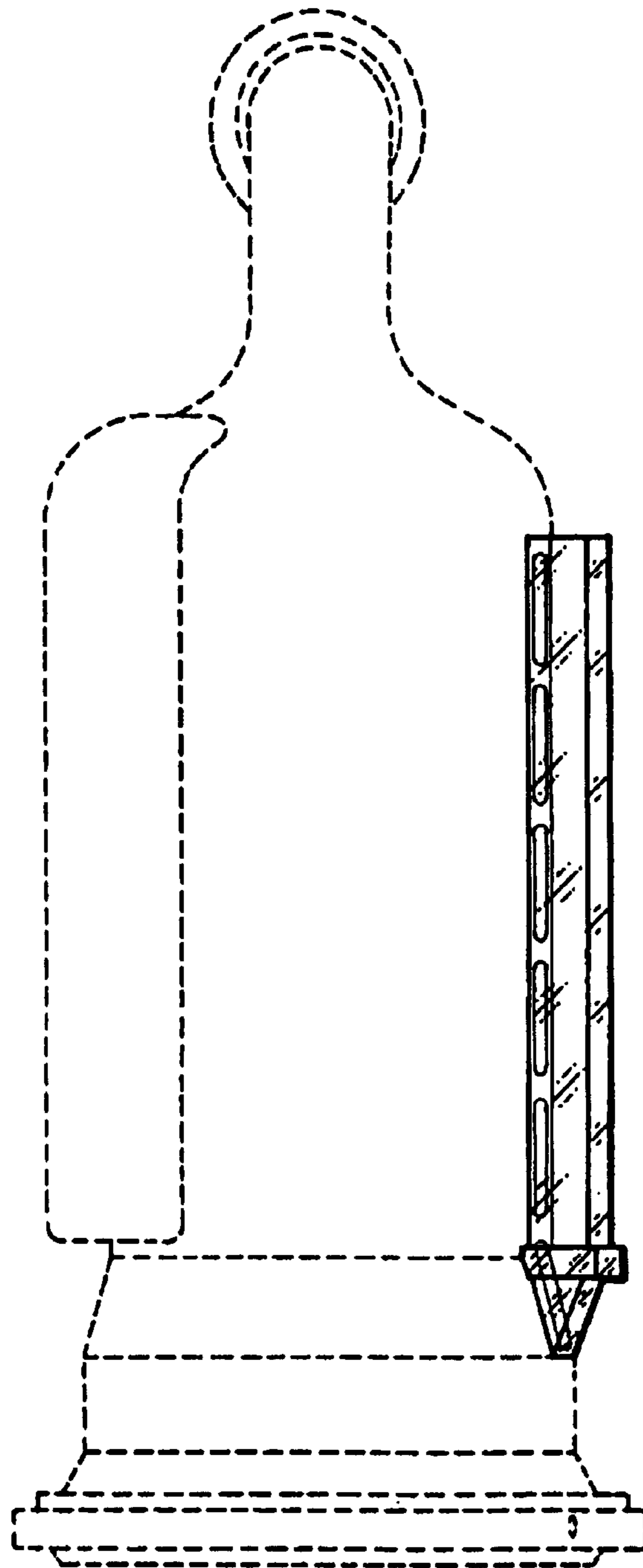


FIG. 6

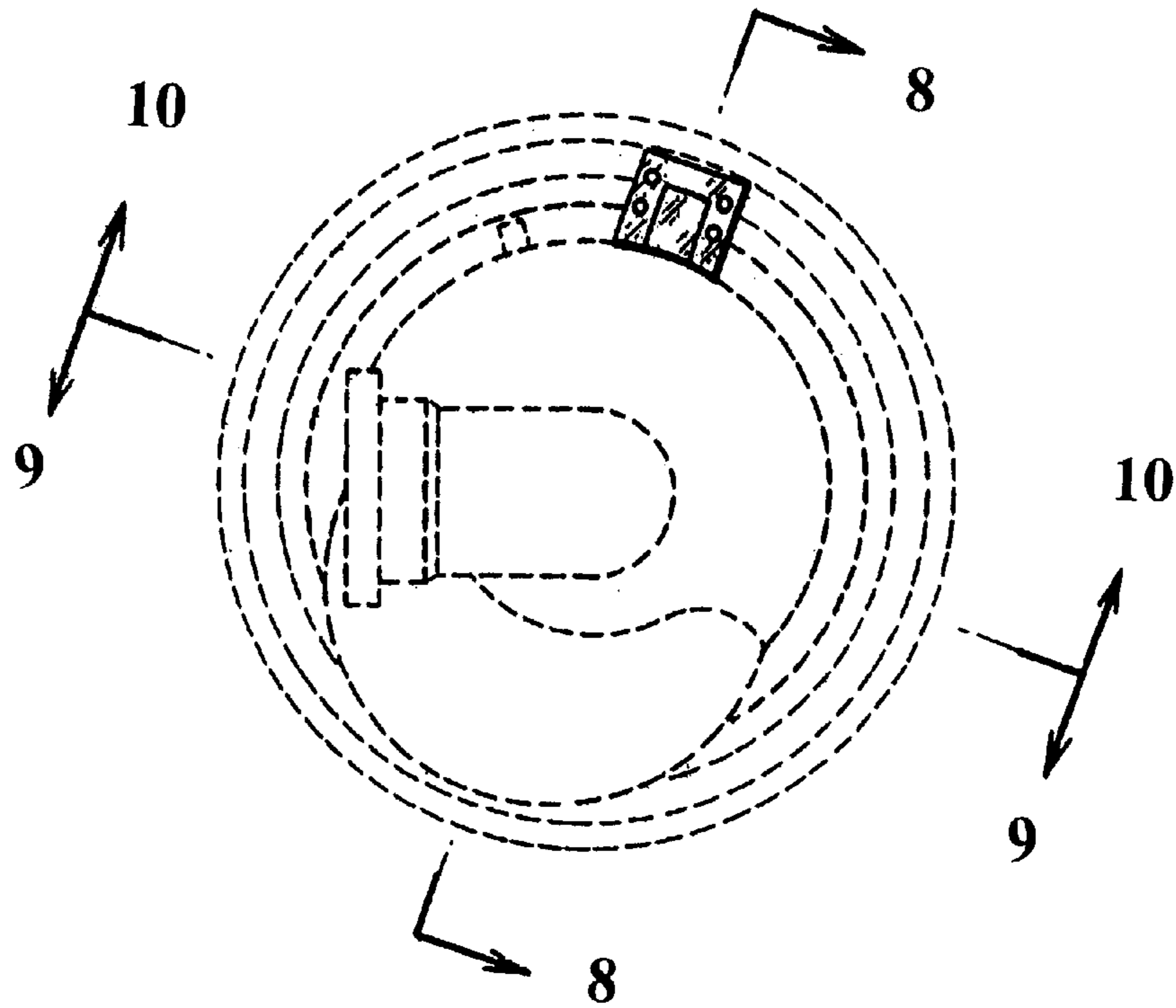


FIG. 7

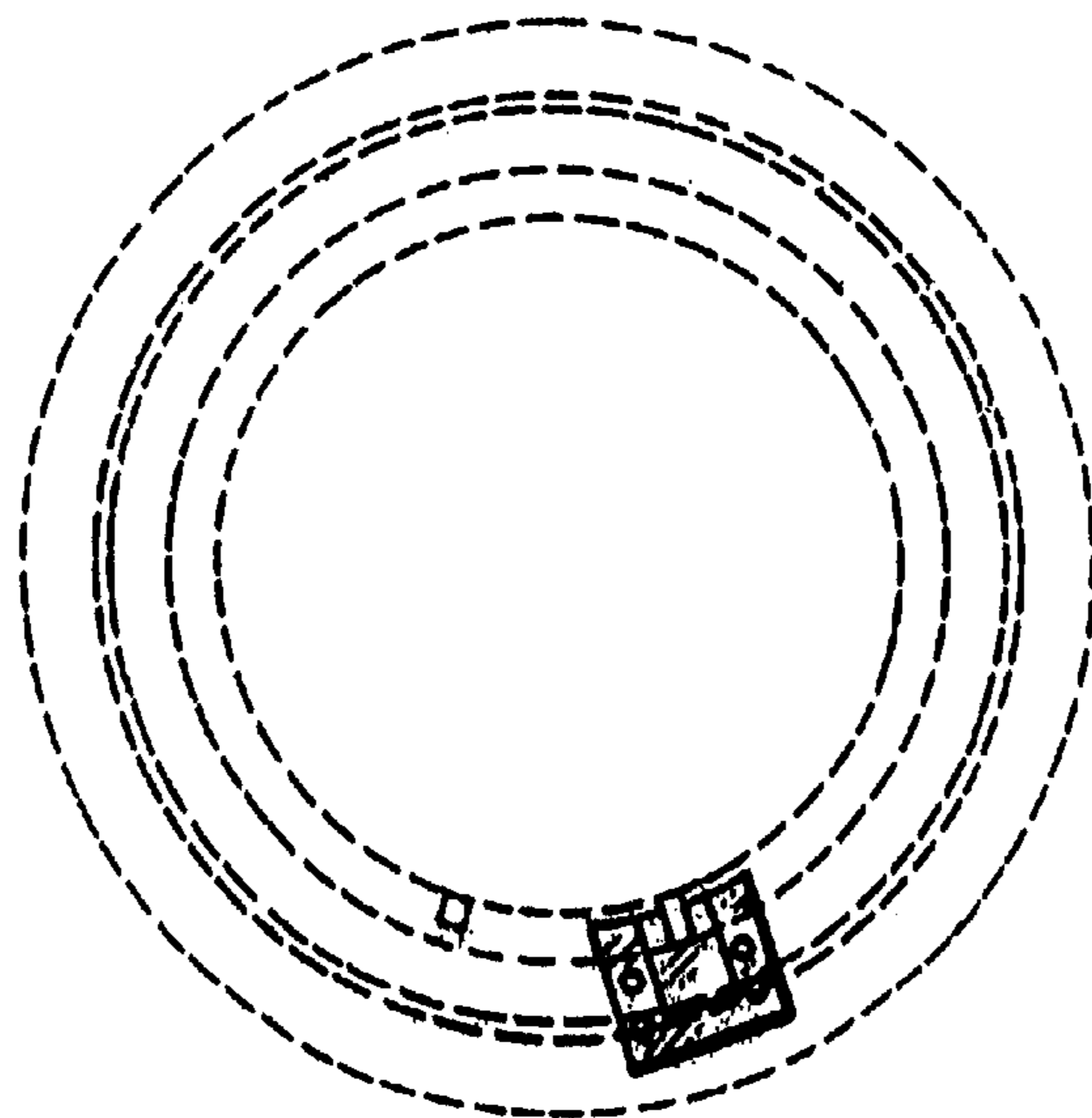


FIG. 8

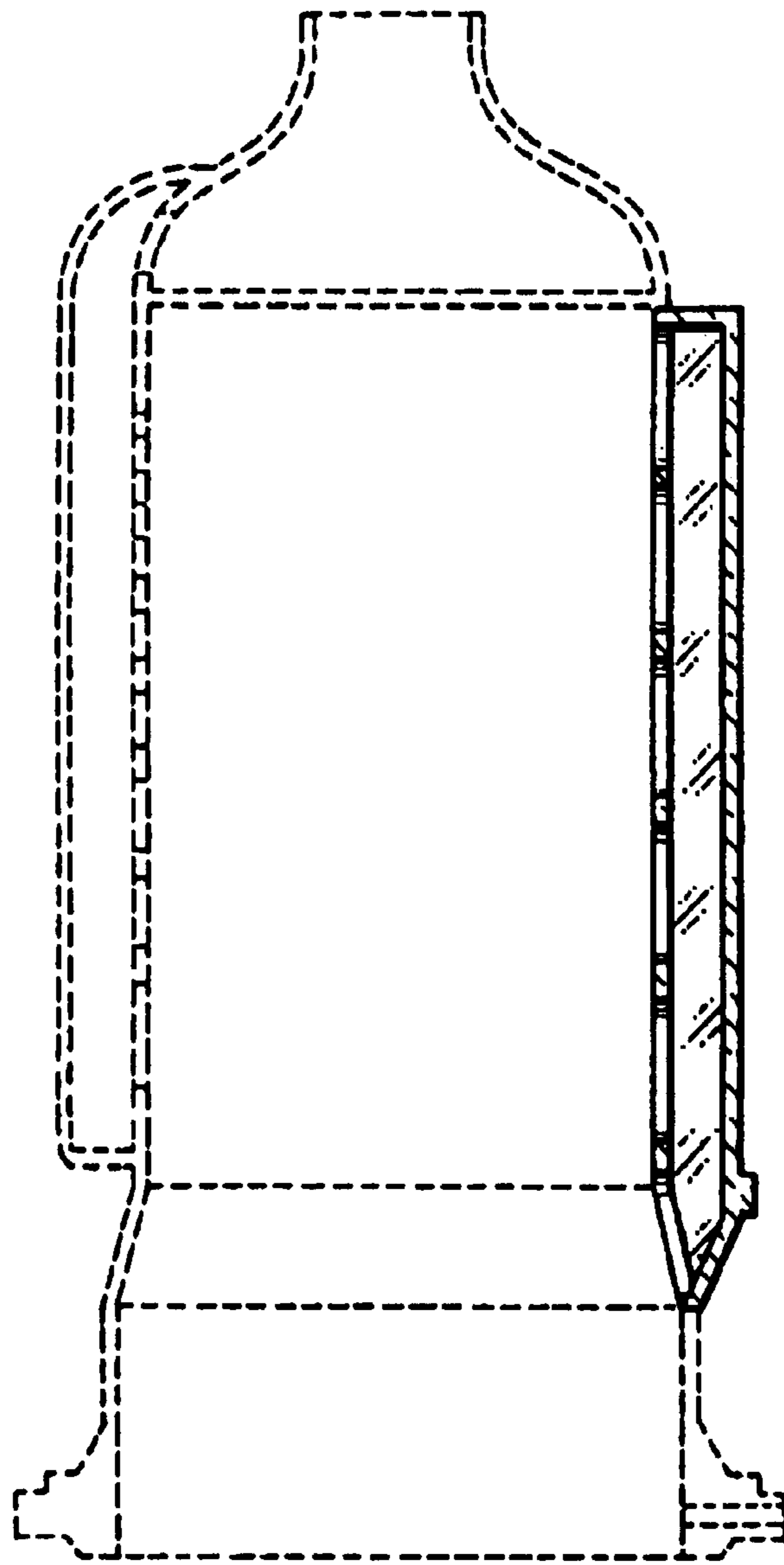


FIG. 9

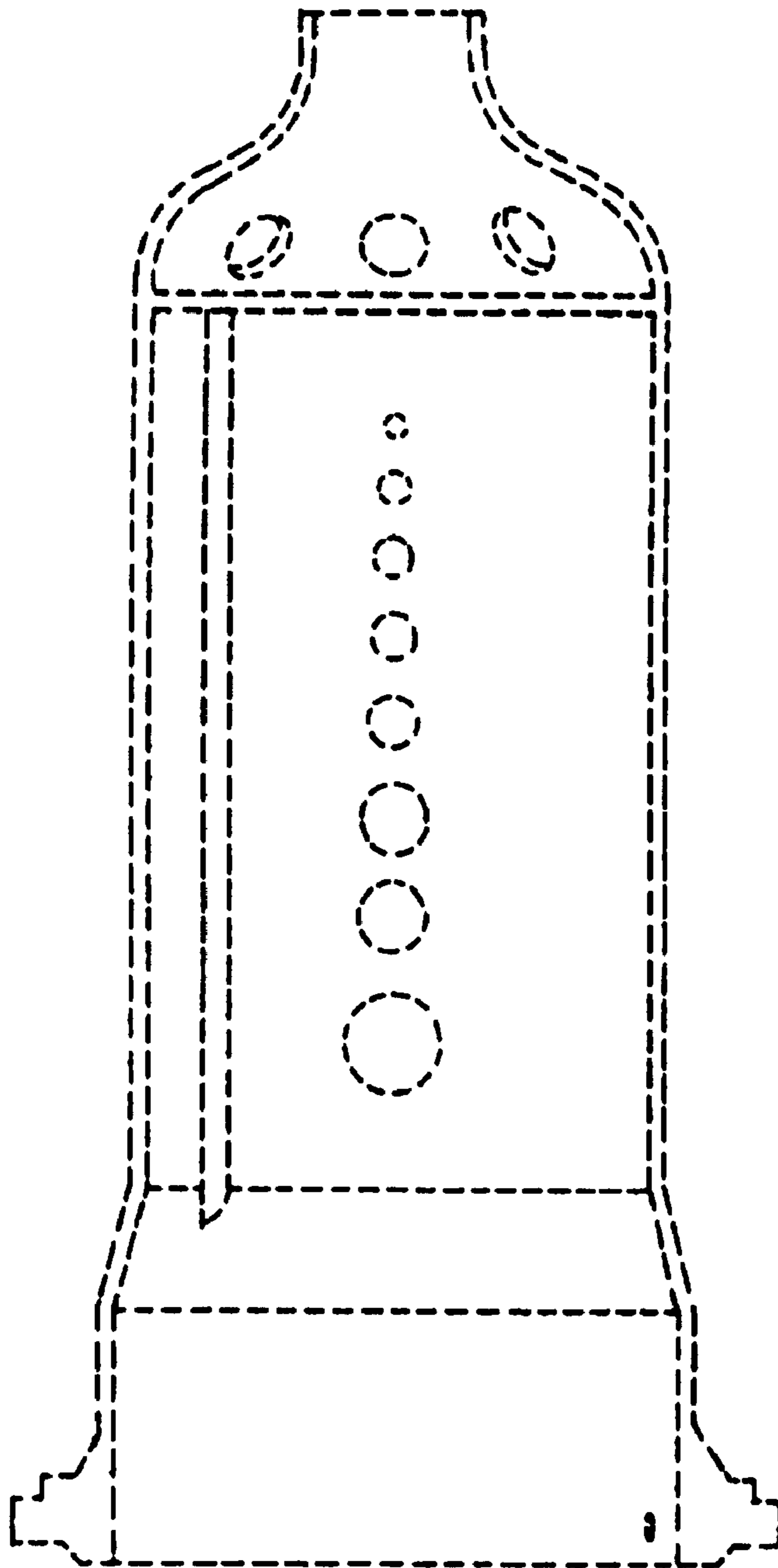


FIG. 10

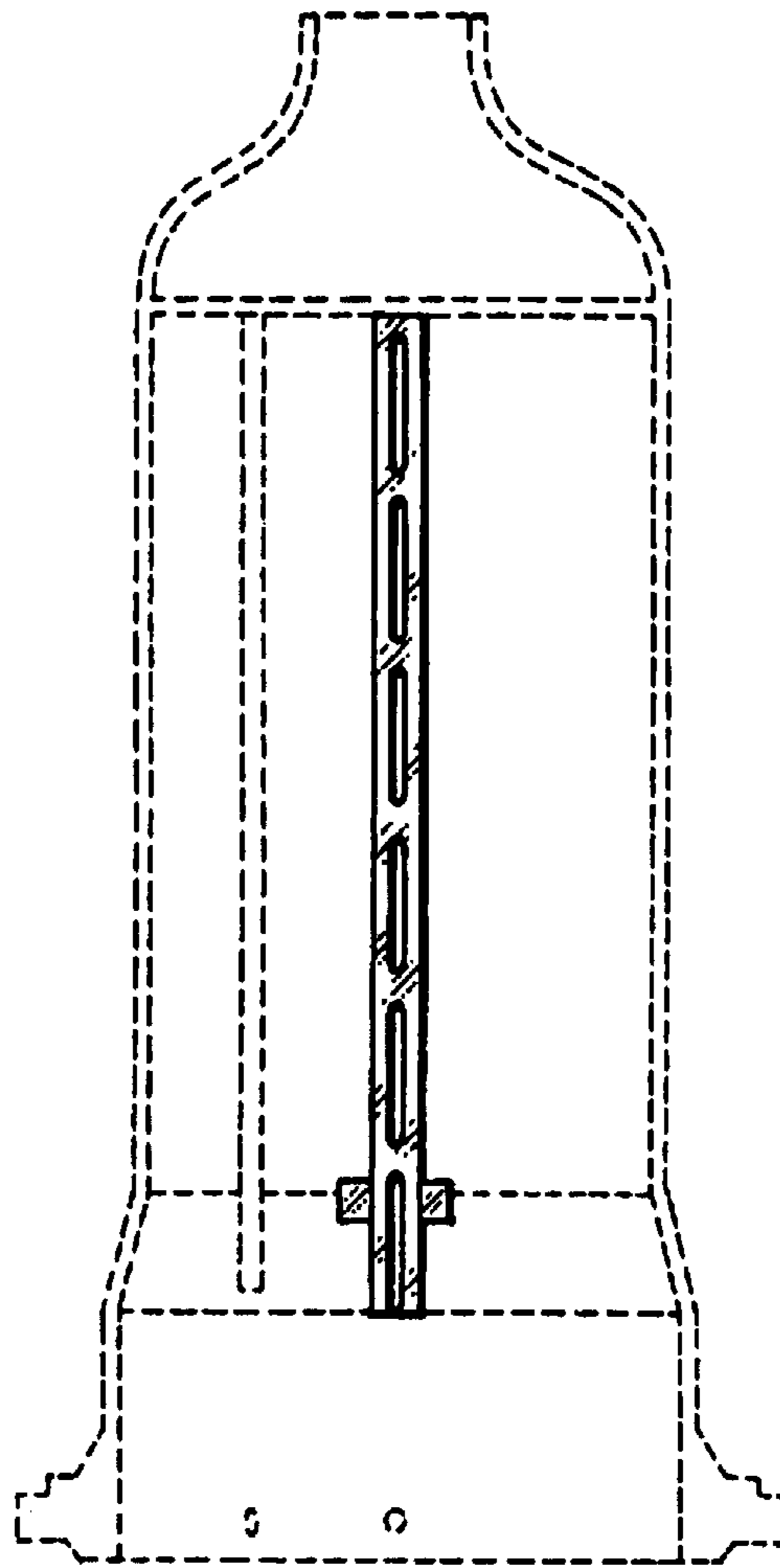


FIG. 11

