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(12) **United States Design Patent**
Peddle

(10) **Patent No.:** **US D520,015 S**

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(54) **COVER FOR MEMORY CHIPS ON A
CIRCUIT BOARD**

(75) Inventor: **Charles I. Peddle**, Las Vegas, NV (US)

(73) Assignee: **Celetronix, Inc.**, Simi Valley, CA (US)

(**) Term: **14 Years**

(21) Appl. No.: **29/168,585**

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(51) **LOC (8) Cl.** **14-02**

(52) **U.S. Cl.** **D14/435**

(58) **Field of Classification Search** D14/432-438;
D13/182; 361/816, 748, 800
See application file for complete search history.

(56) **References Cited**

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Primary Examiner—M. H. Tung

(74) *Attorney, Agent, or Firm*—Steven L. Nichols; Paul W. Fish; Rader, Fishman & Grauer PLLC

(57) **CLAIM**

The ornamental design for a cover for memory chips on a circuit board, as shown and described.

DESCRIPTION

FIG. 1 is a top plan view of a cover for memory chips on a circuit board showing my new design;

FIG. 2 is an inside view of the top portion, of the cover for memory chips on a circuit board;

FIG. 3 is a top plan view thereof;

FIG. 4 is a bottom plan view thereof;

FIG. 5 is a cross-sectional view thereof, taken along 5—5 of FIG. 1;

FIG. 6 is a front elevational view thereof;

FIG. 7 is a rear elevational view thereof;

FIG. 8 is an end elevational view thereof, the top portion is shown separately for clarity of illustration, the opposite end is a mirror image;

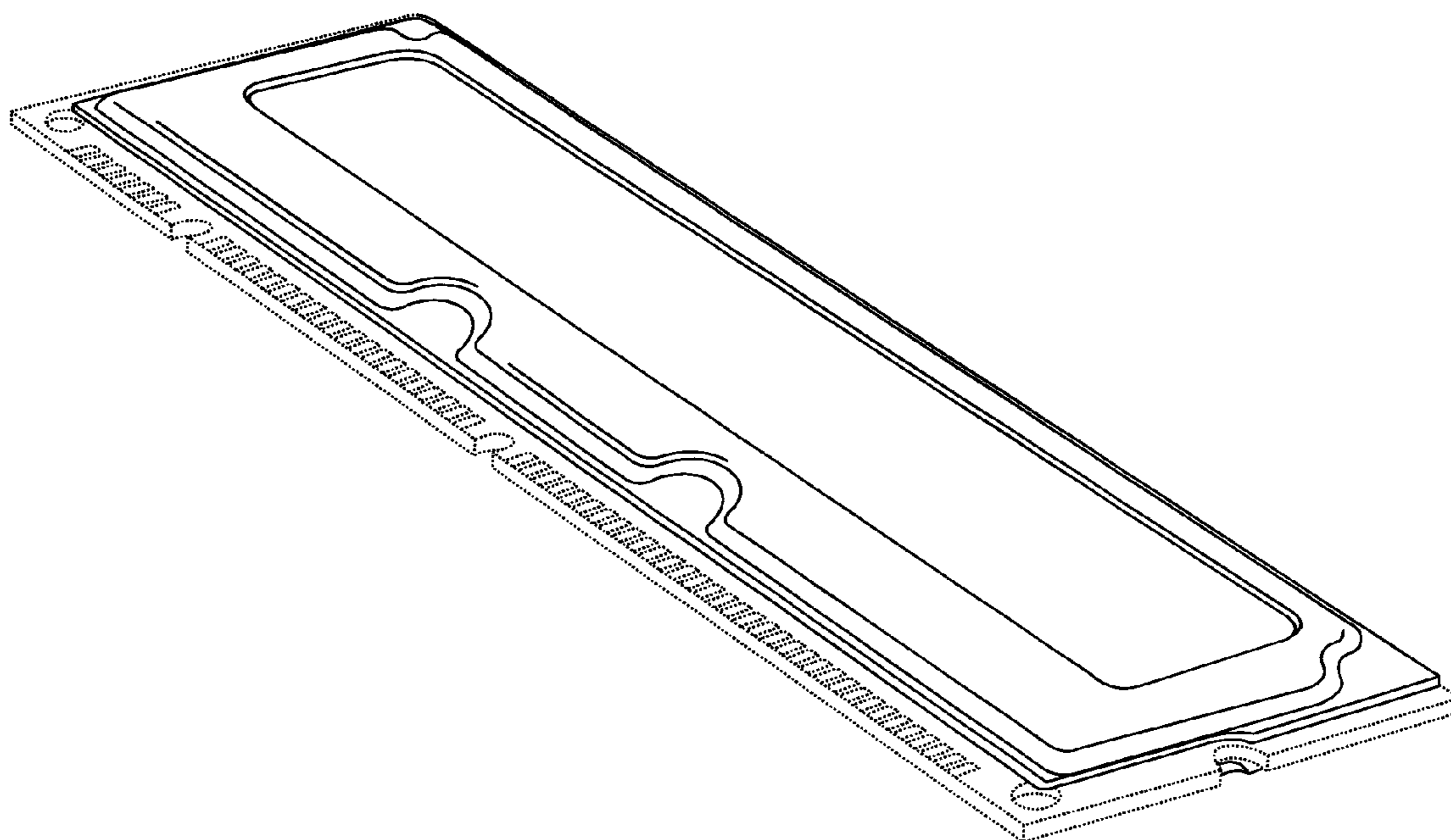
FIG. 9 is an end elevational view thereof;

FIG. 10 is a top perspective view thereof, on a reduced scale; and,

FIG. 11 is a cross-sectional view thereof, taken on line 11—11 of FIG. 1.

The broken line drawings of a circuit board in FIGS. 1, 4-7 and 9-11 is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 11 Drawing Sheets



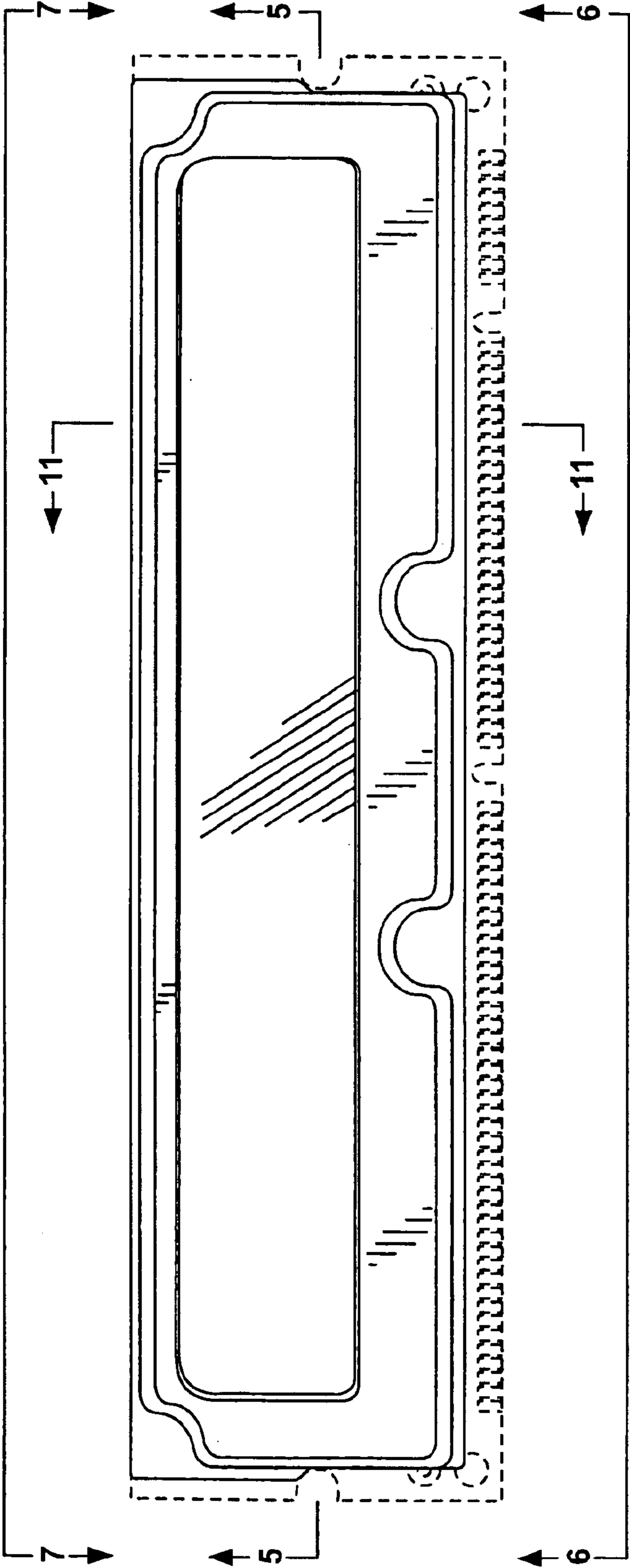


Fig. 1

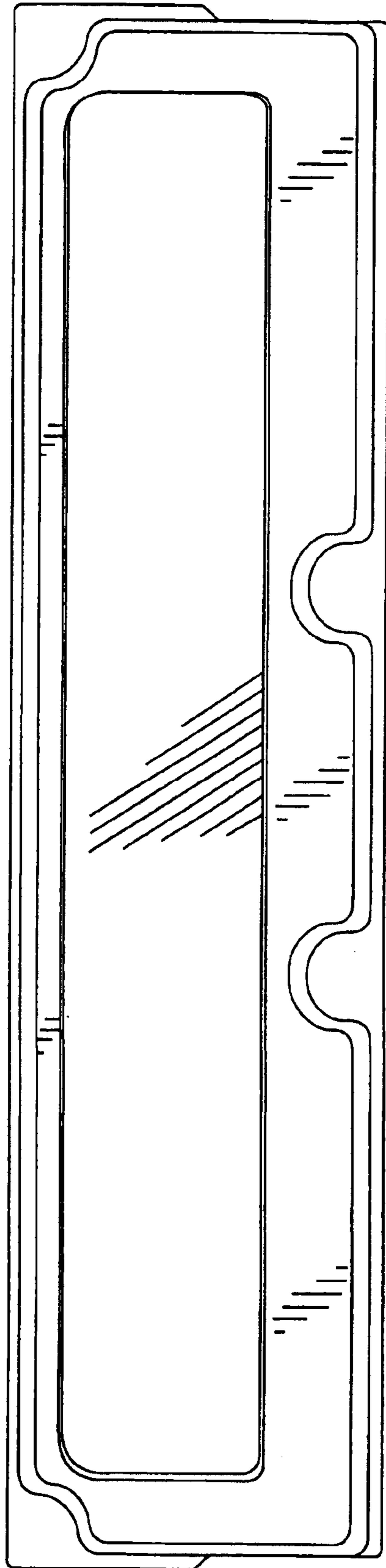


Fig. 2

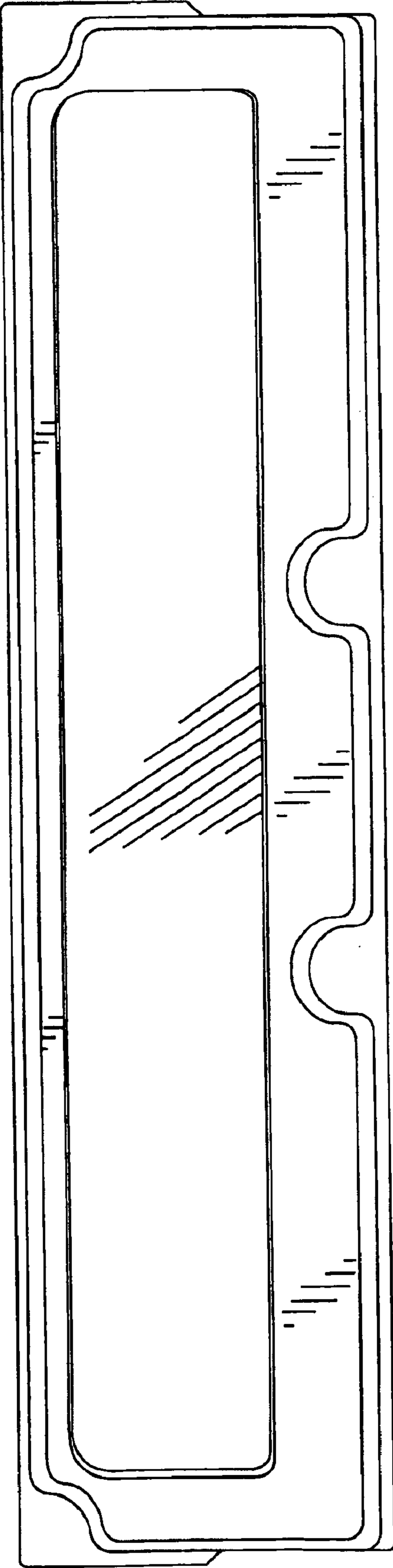


Fig. 3

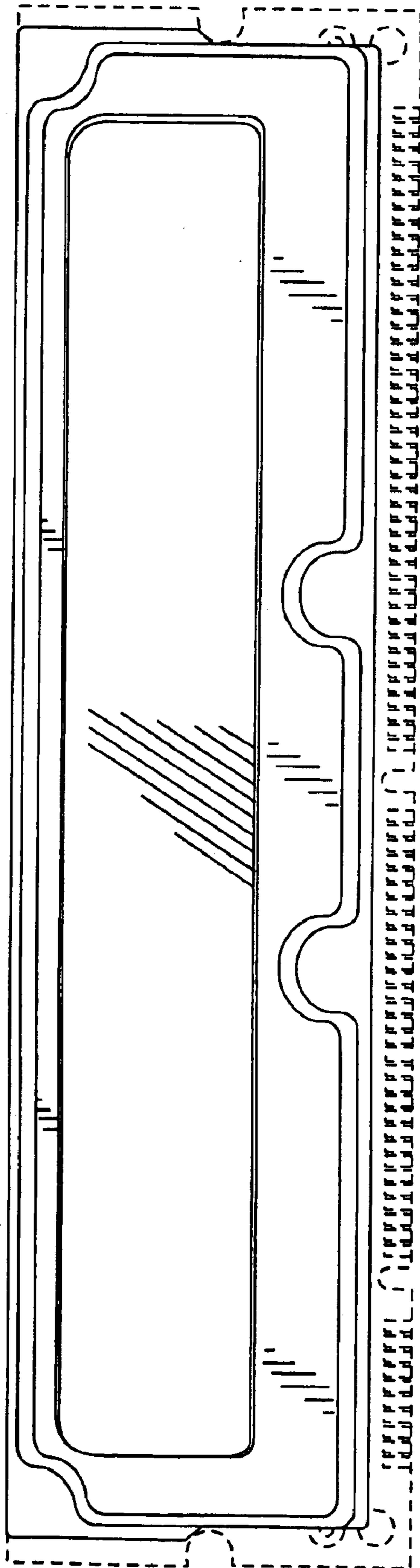


Fig. 4

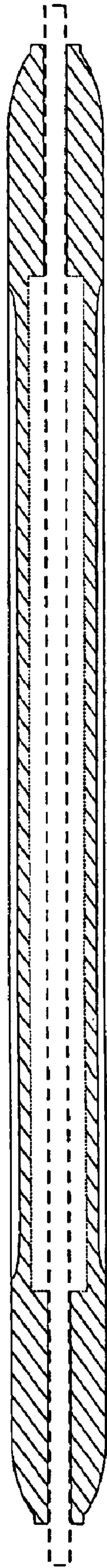


Fig. 5

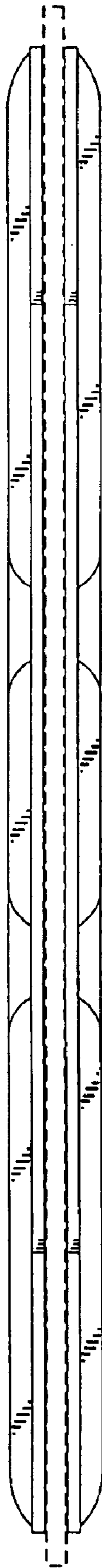


Fig. 6



Fig. 7



Fig. 8

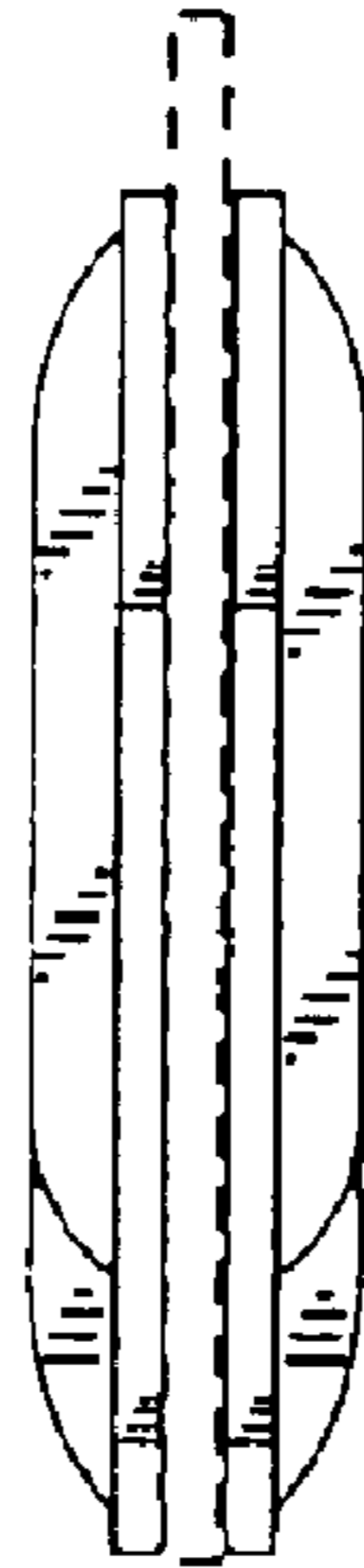


Fig. 9

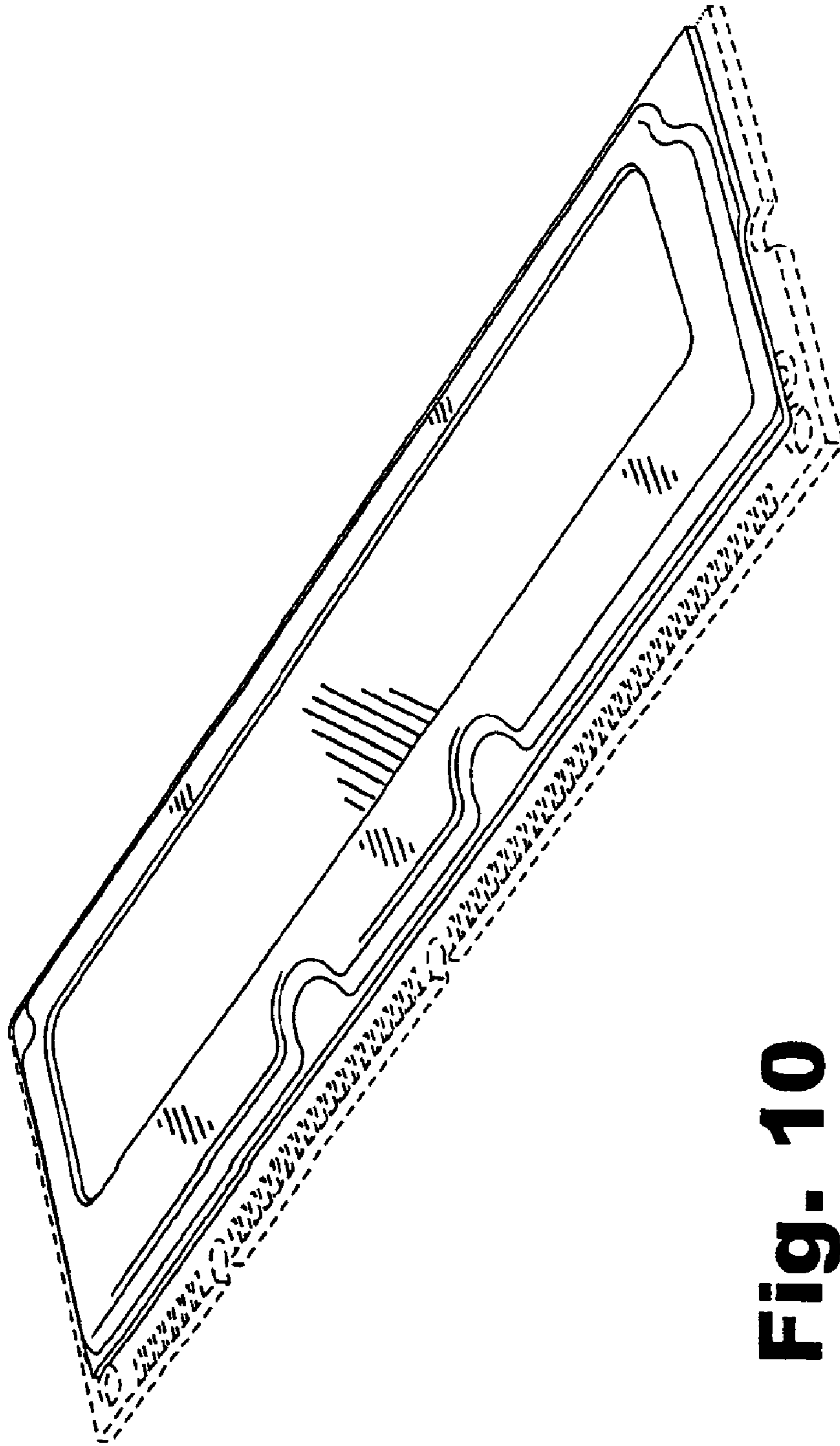


Fig. 10

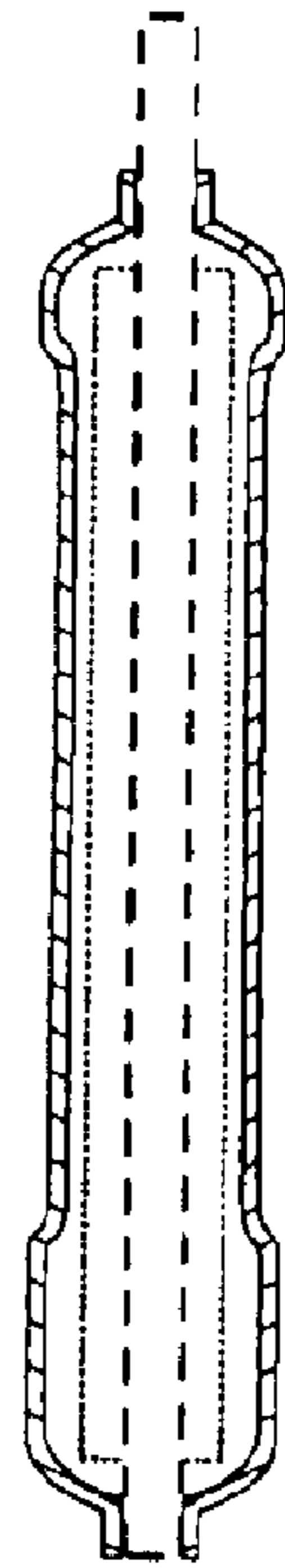


Fig. 11