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(12) **United States Design Patent**
Nakamura et al.

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(45) **Date of Patent:** **** Feb. 28, 2006**

(54) **BASE FOR A SEMICONDUCTOR CARRIER**

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(75) Inventors: **Yuji Nakamura**, Tokyo (JP); **Katsumi Suzuki**, Tokyo (JP); **Takahiro Ishibashi**, Tokyo (JP); **Eiji Kobori**, Tokyo (JP)

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(73) Assignee: **Yamaichi Electronics Co.**, Tokyo (JP)

(**) Term: **14 Years**

Primary Examiner—Stella Reid
Assistant Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Finnegan, Henderson, Farabow, Garrett & Dunner, LLP

(21) Appl. No.: **29/229,567**

(22) Filed: **May 10, 2005**

(57) **CLAIM**

Related U.S. Application Data

The ornamental design for a base for a semiconductor carrier, as shown and described.

(62) Division of application No. 29/211,532, filed on Aug. 18, 2004, now Pat. No. Des. 507,545.

DESCRIPTION

(30) **Foreign Application Priority Data**

Feb. 20, 2004 (JP) 2004-004834

FIG. 1 is a front view of a base for a semiconductor carrier showing our new design, the rear view being a mirror image thereof;

(51) **LOC (8) Cl.** **13-03**

FIG. 2 is a top view thereof;

(52) **U.S. Cl.** **D13/182**

FIG. 3 is a bottom view thereof, the perforations shown in dashed lines being no part of the claimed design;

(58) **Field of Classification Search** D13/182;
257/666, 669, 675, 676; 324/755
See application file for complete search history.

FIG. 4 is a right-side view thereof;

FIG. 5 is a left-side view thereof; and,

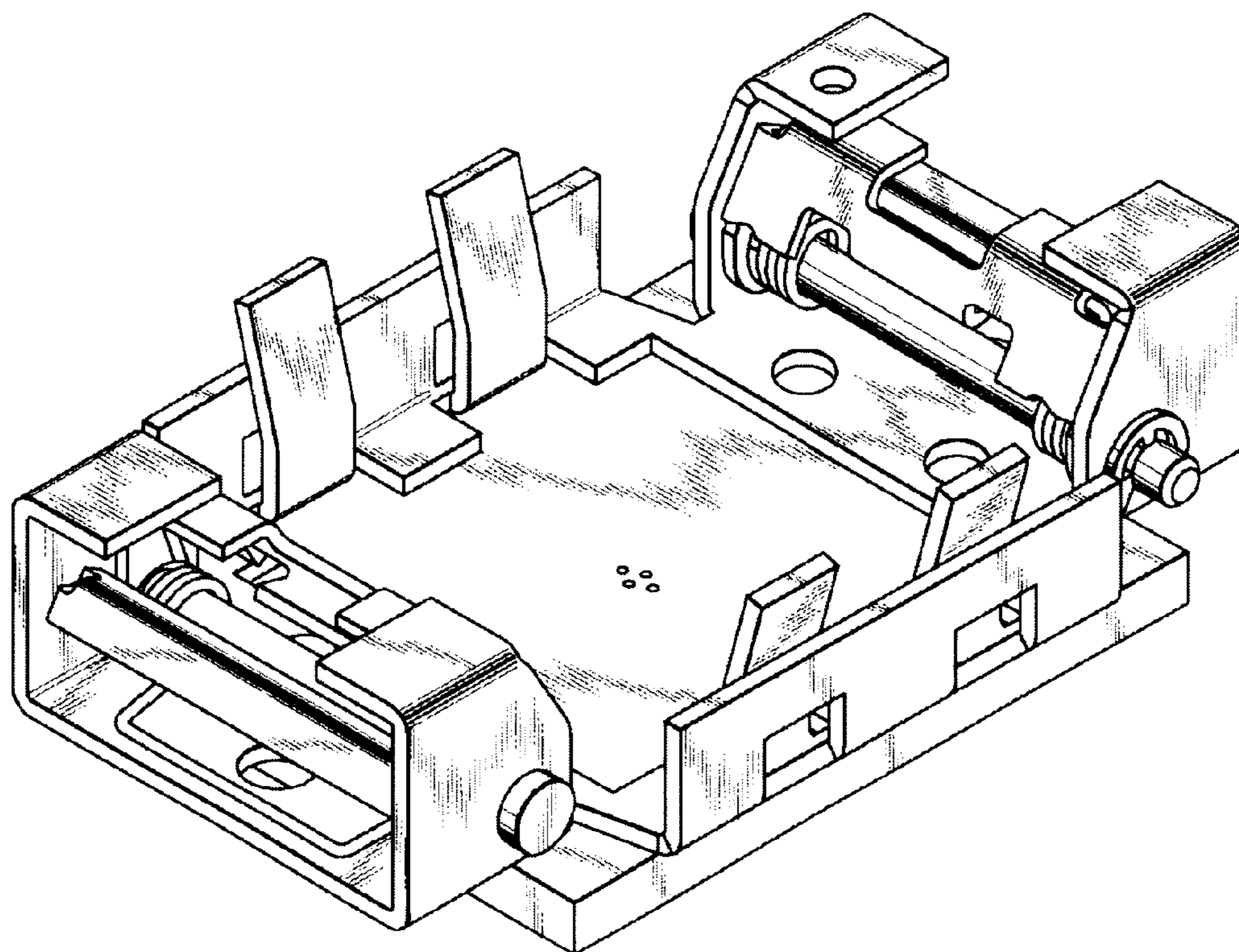
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FIG. 6 is a perspective view thereof.

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1 Claim, 3 Drawing Sheets



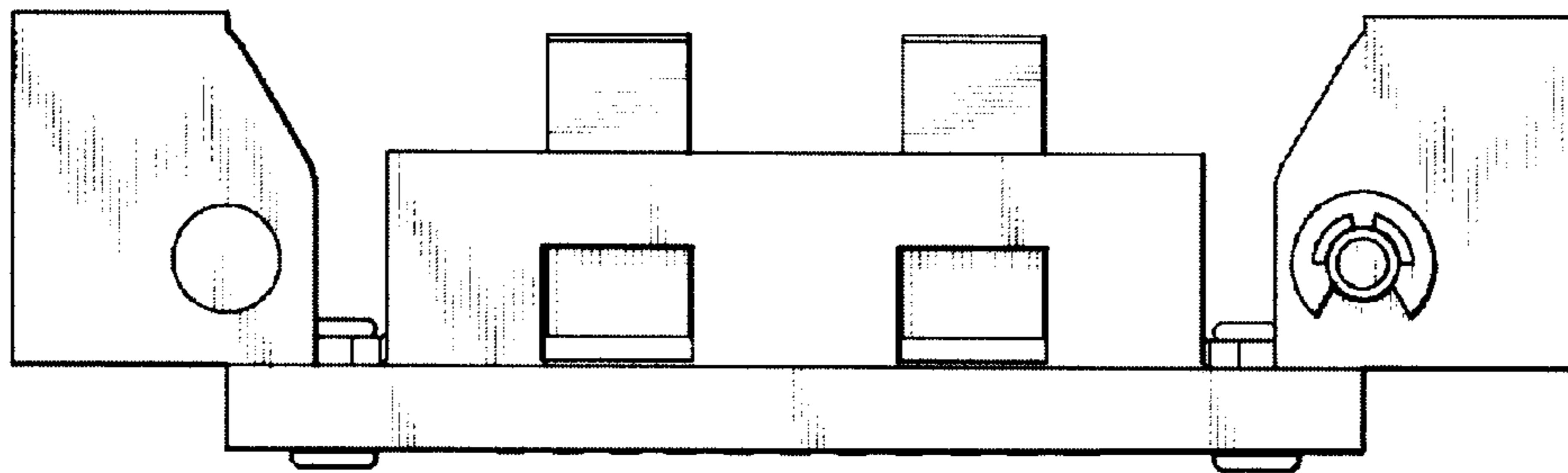


FIG.1

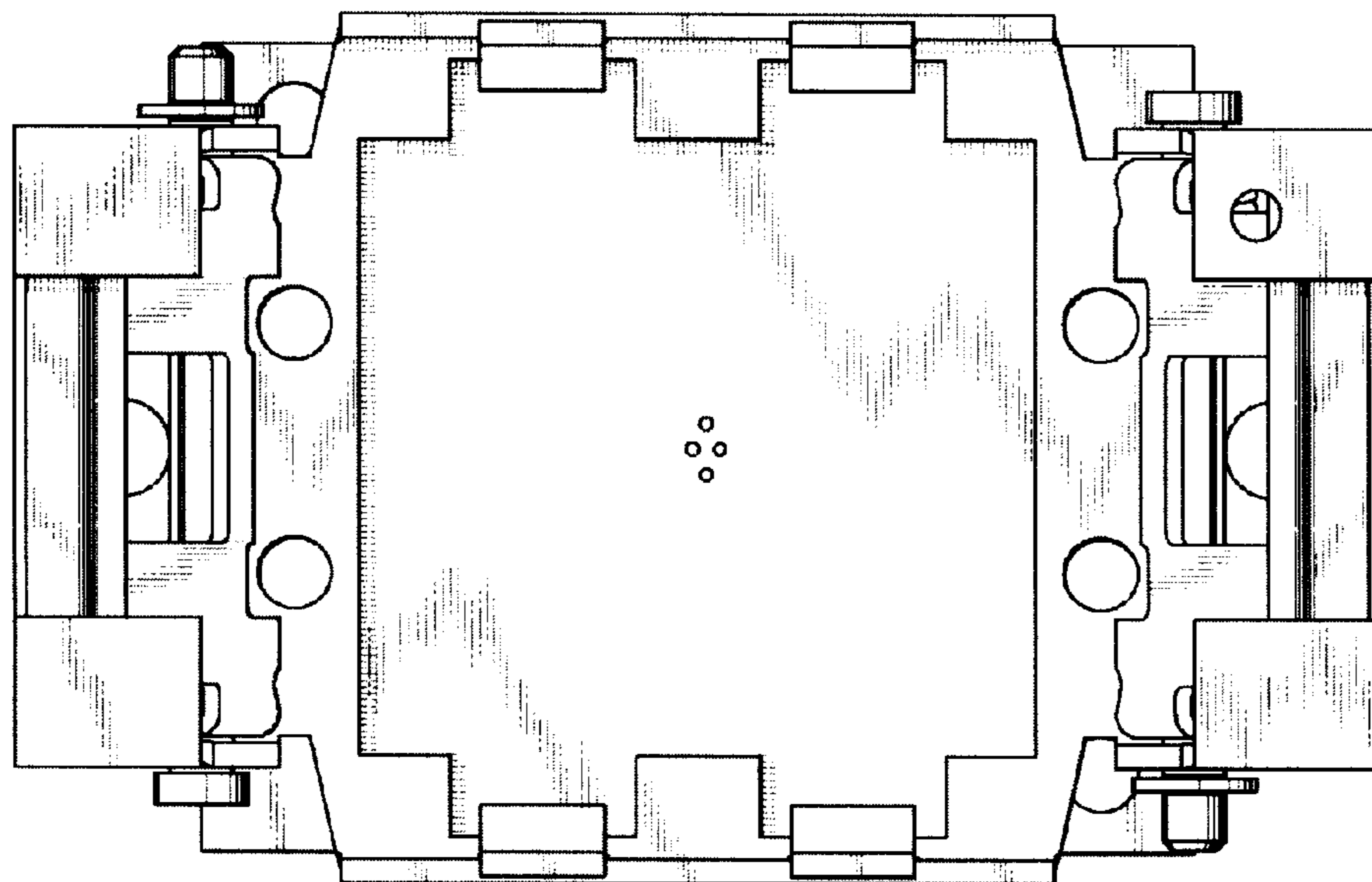


FIG.2

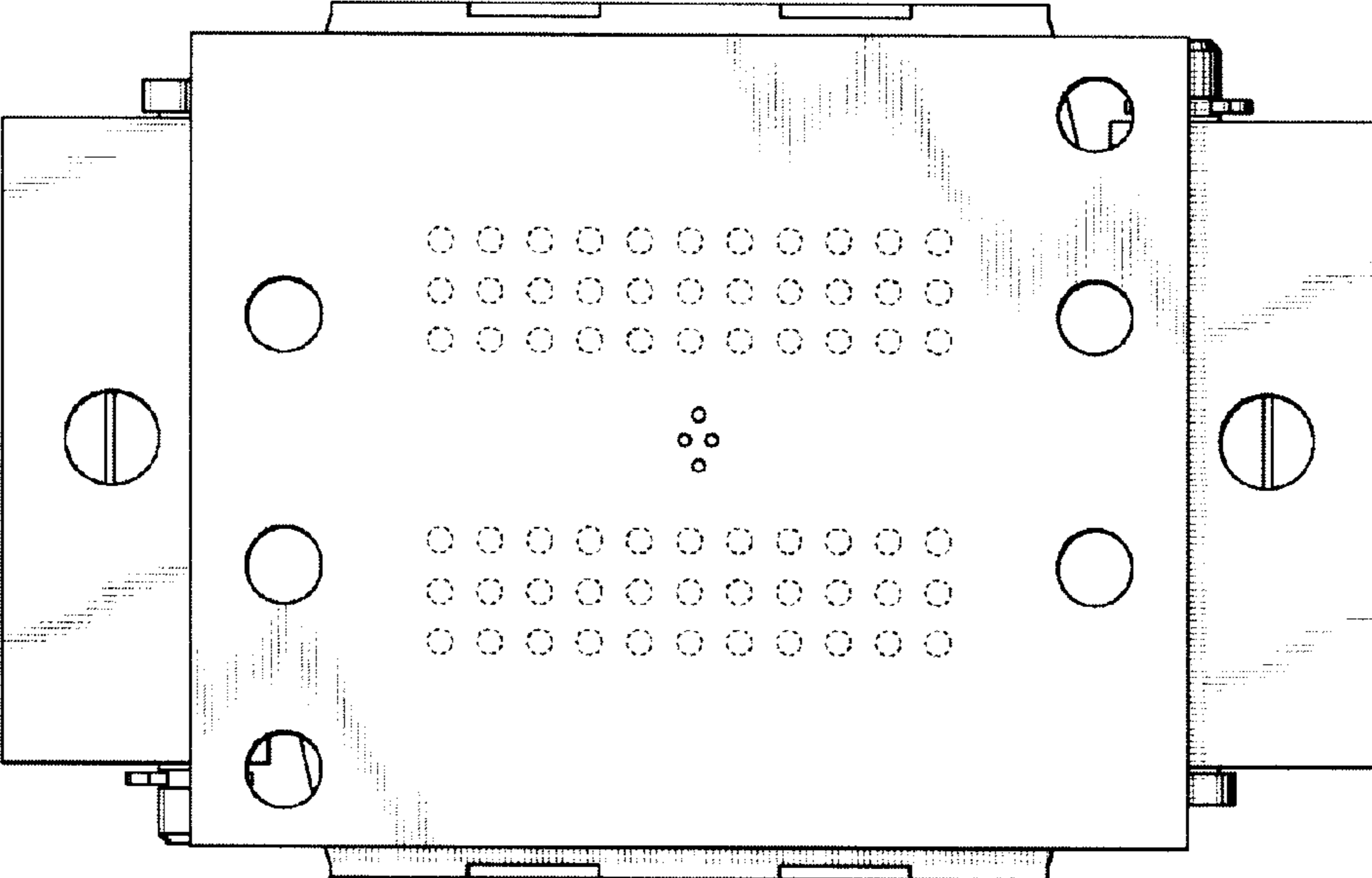


FIG.3

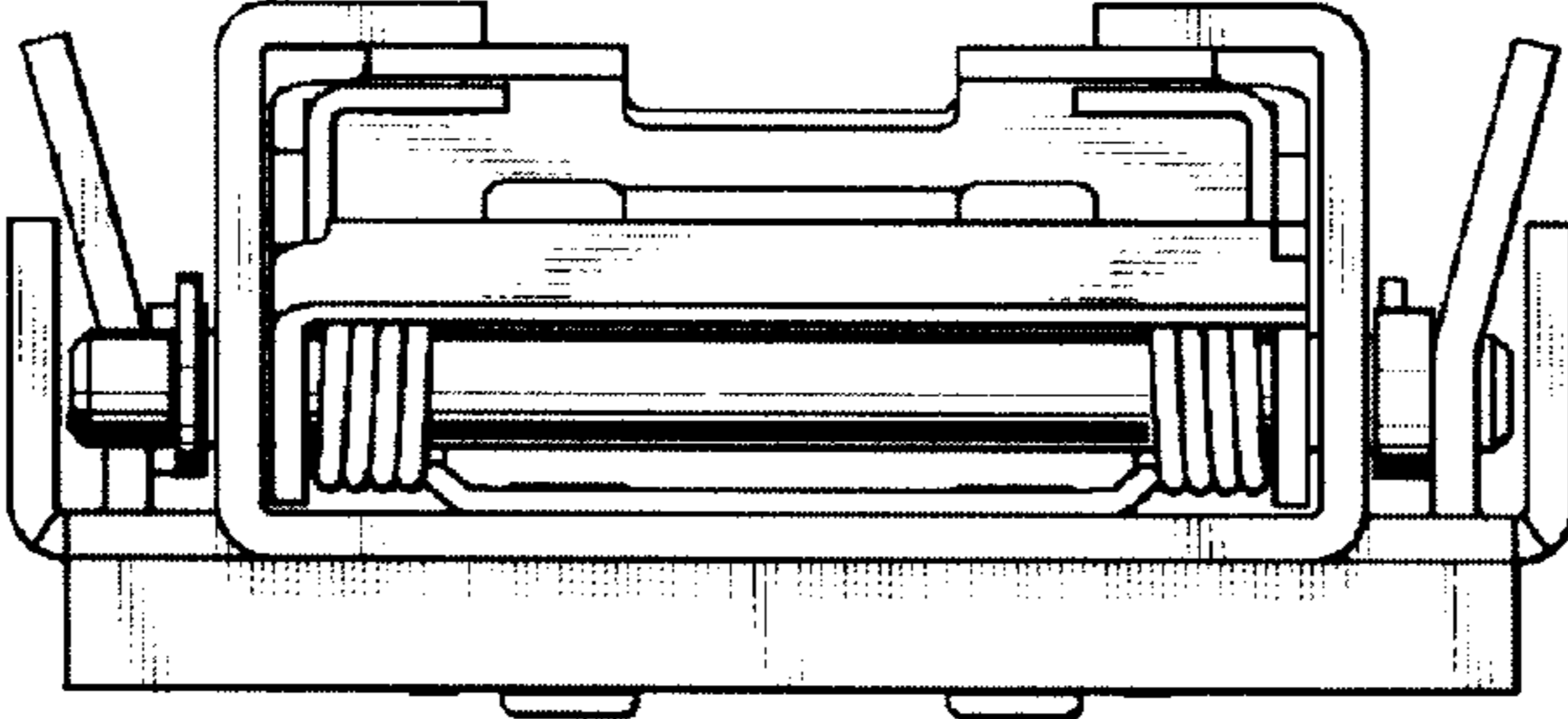


FIG.4

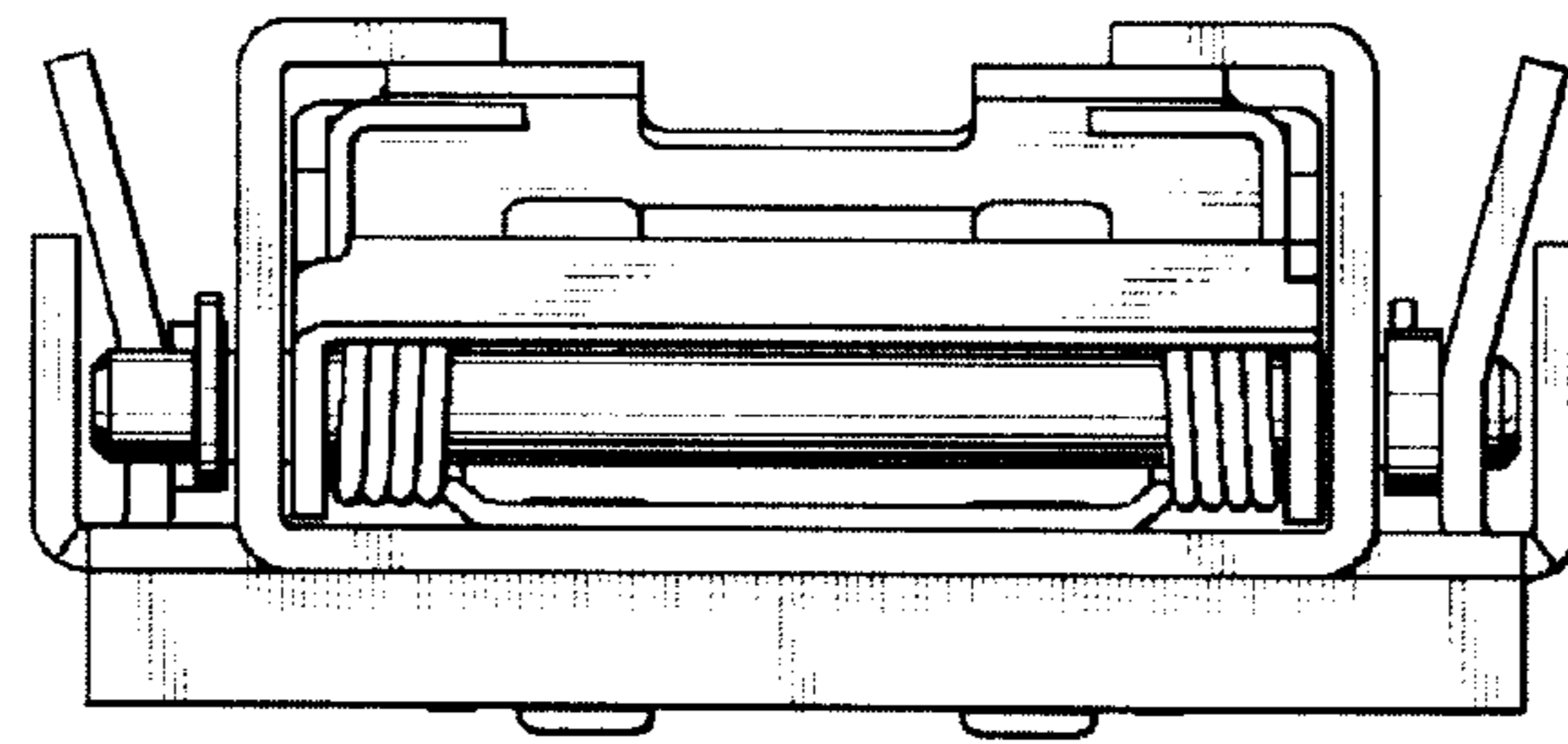


FIG.5

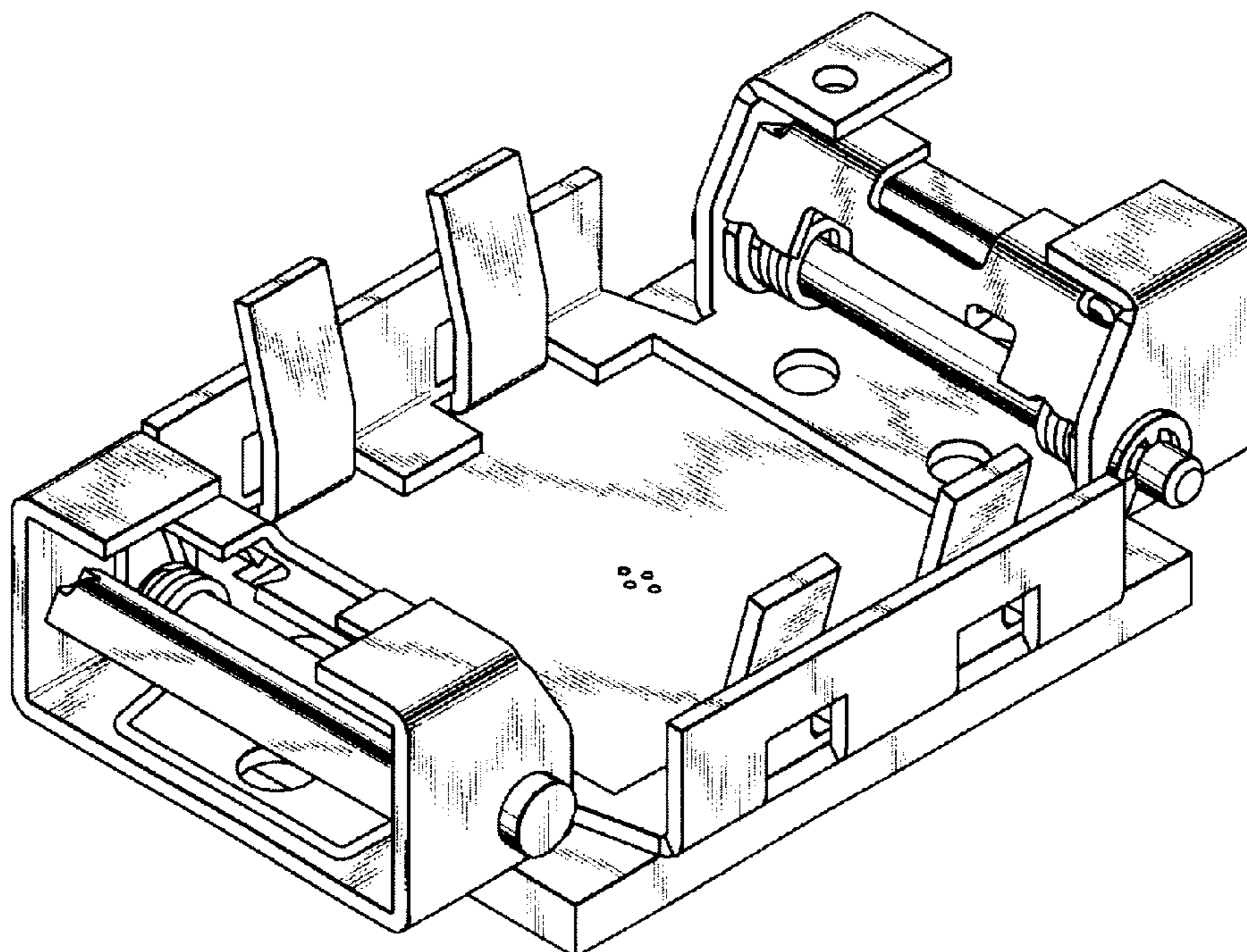


FIG.6