



US00D515520S

(12) **United States Design Patent**
Komoto

(10) **Patent No.:** **US D515,520 S**
(45) **Date of Patent:** **** Feb. 21, 2006**

(54) **SEMICONDUCTOR DEVICE**

FOREIGN PATENT DOCUMENTS

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JP 751629 12/1988
JP 865628 4/1993

(73) **Assignee:** **Kabushiki Kaisha Toshiba, Tokyo (JP)**

OTHER PUBLICATIONS

(**) **Term:** **14 Years**

Extract of Denpa Shimbun (newspaper) showing an insulated gate transistor, Oct. 13, 1998.

(21) **Appl. No.:** **29/168,222**

* cited by examiner

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(30) **Foreign Application Priority Data**

Mar. 29, 2002 (JP) 2002-008490

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
174/52.1, 52.4; 257/666, 669, 675, 676, 678,
257/690, 692, 696, 697, 730, 787; 361/773,
361/820; 438/64, 65

See application file for complete search history.

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Maier & Neustadt, P.C.

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

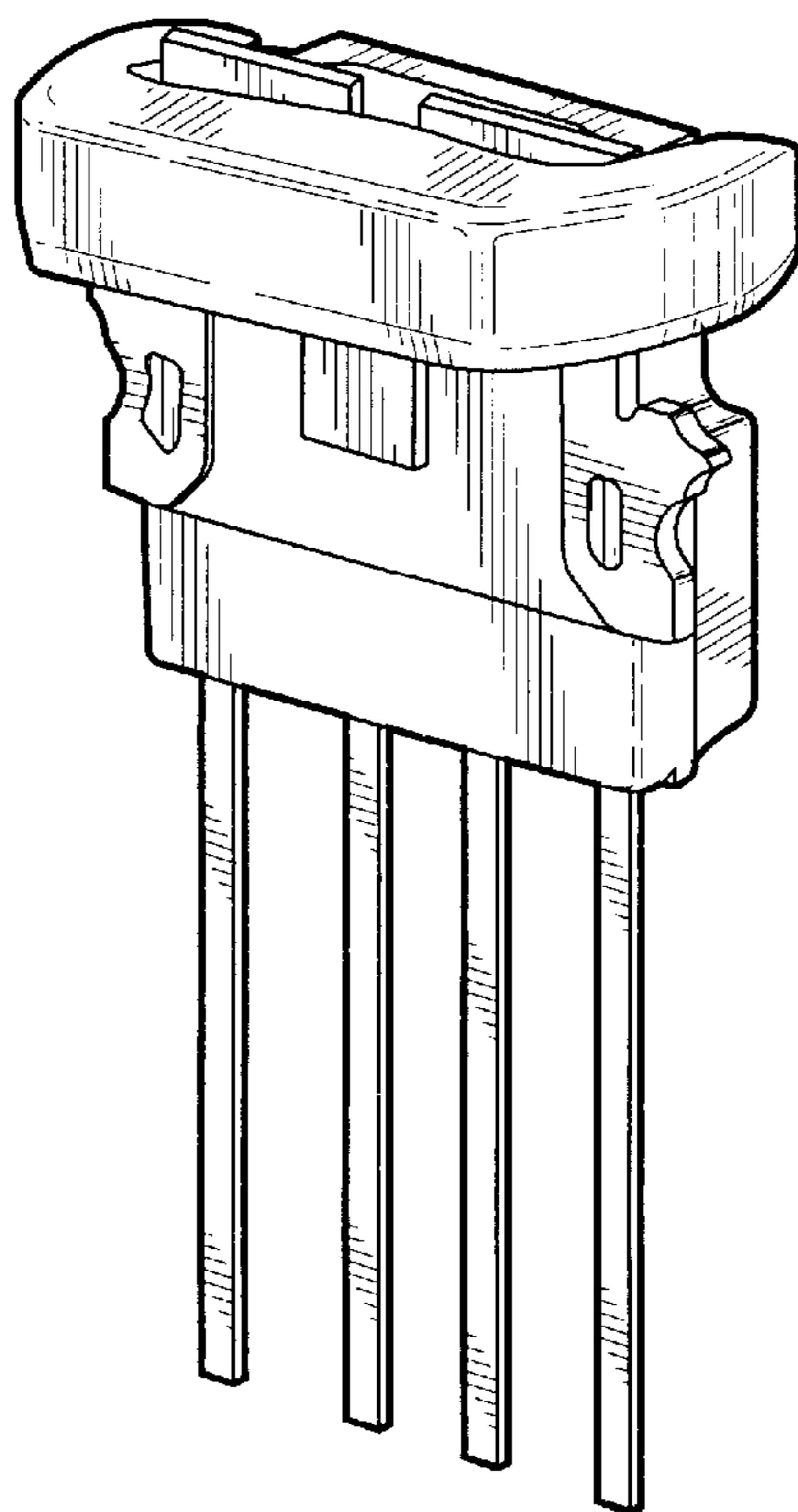
FIG. 1 is a front, top and right side perspective view of a semiconductor device, showing my new design; FIG. 2 is a front elevational view thereof; FIG. 3 is a rear elevational view thereof; FIG. 4 is a top plan view thereof; FIG. 5 is a bottom plan view thereof; FIG. 6 is a left side elevational view thereof; and, FIG. 7 is a right side elevational view thereof.

(56) **References Cited**

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1 Claim, 4 Drawing Sheets



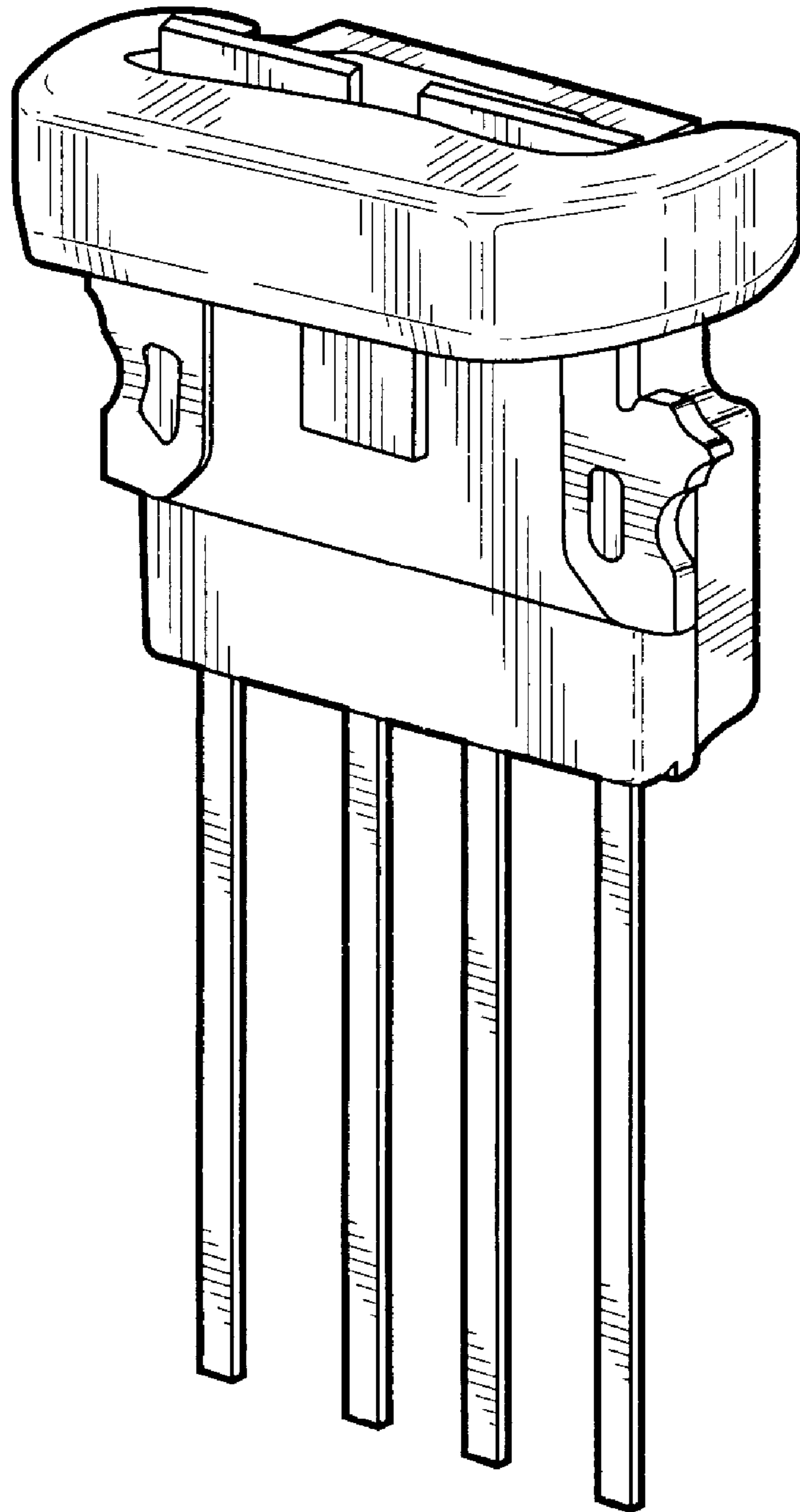


FIG. 1

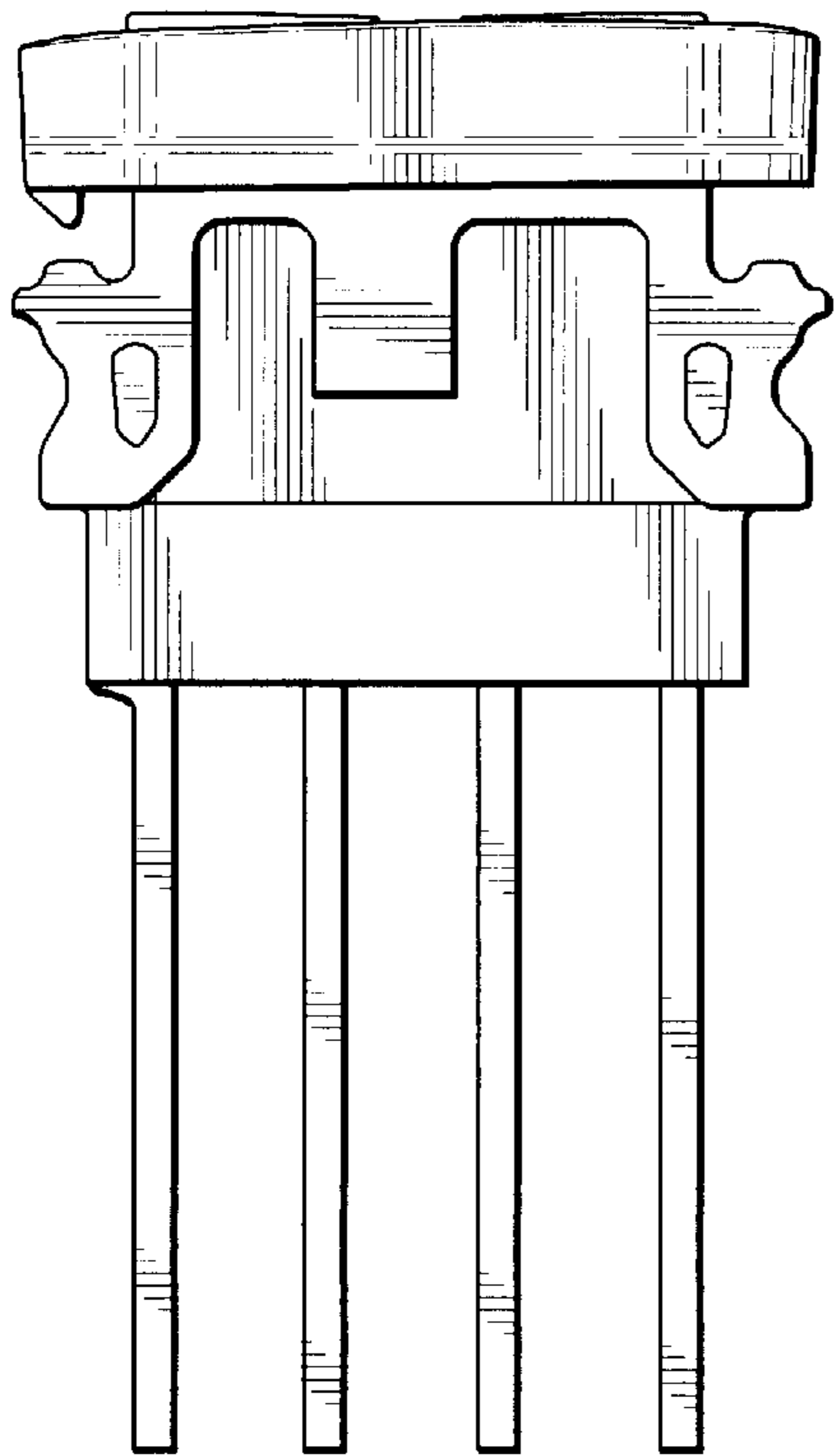


FIG. 2

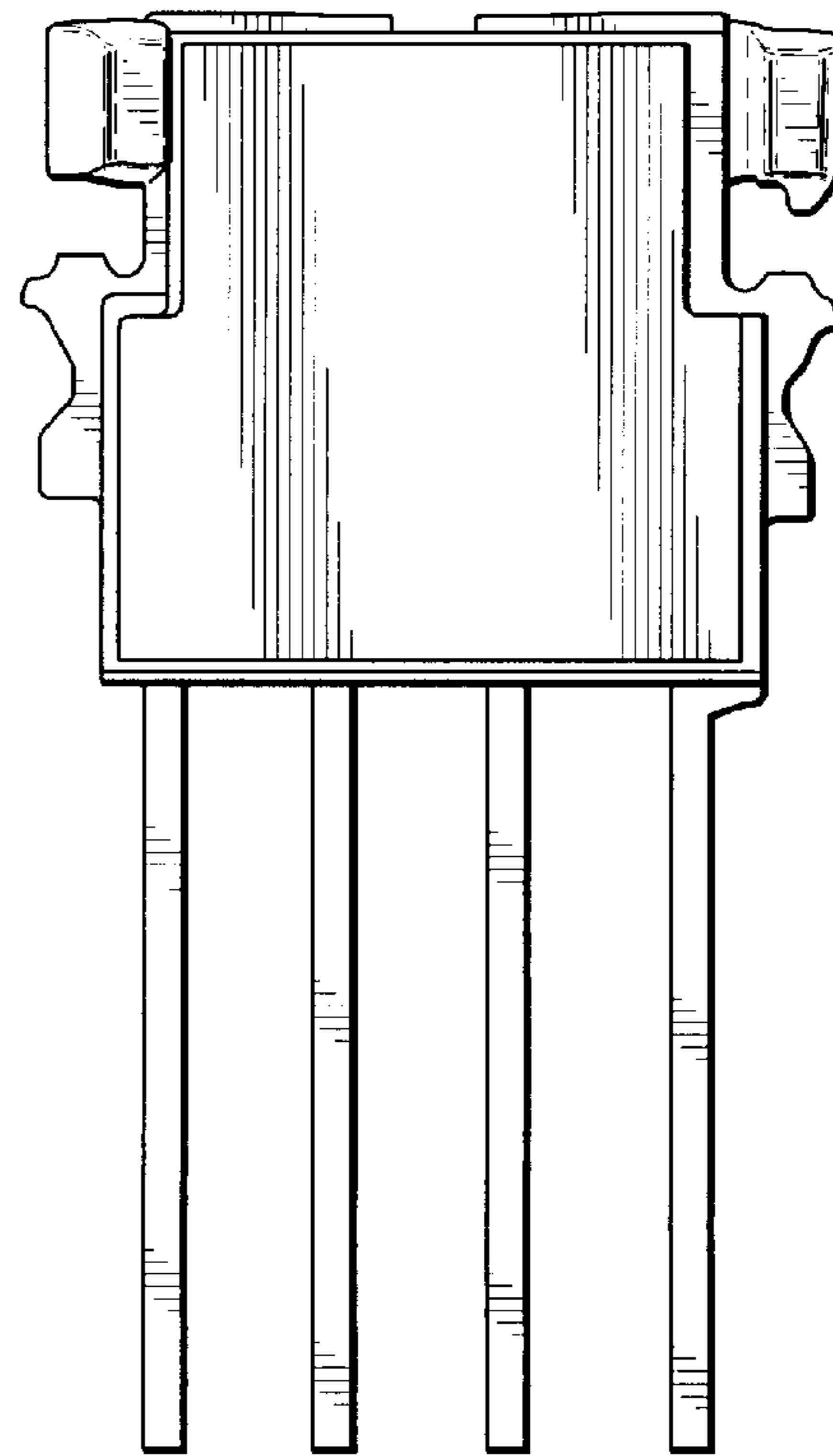


FIG. 3

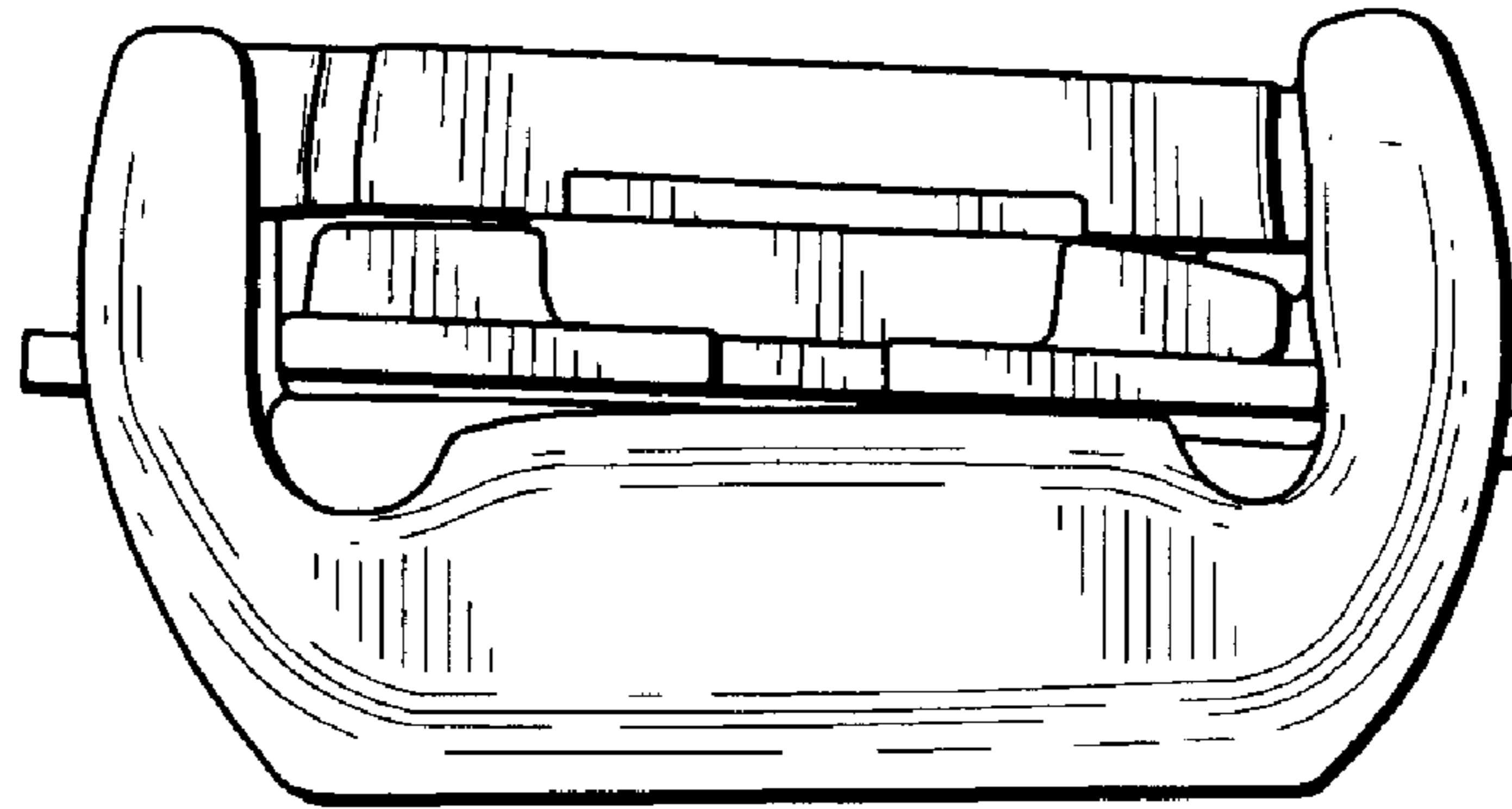


FIG. 4

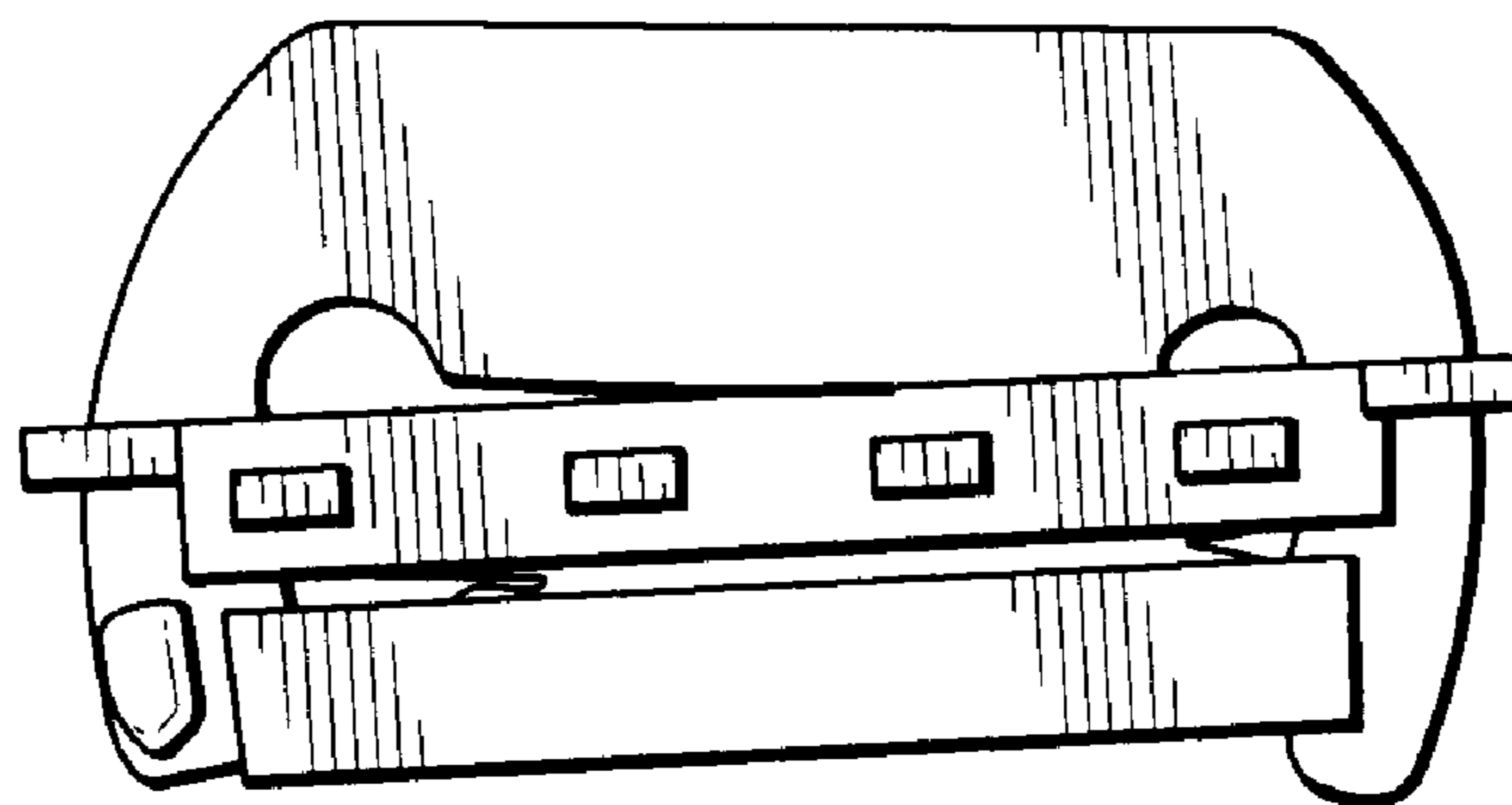


FIG. 5

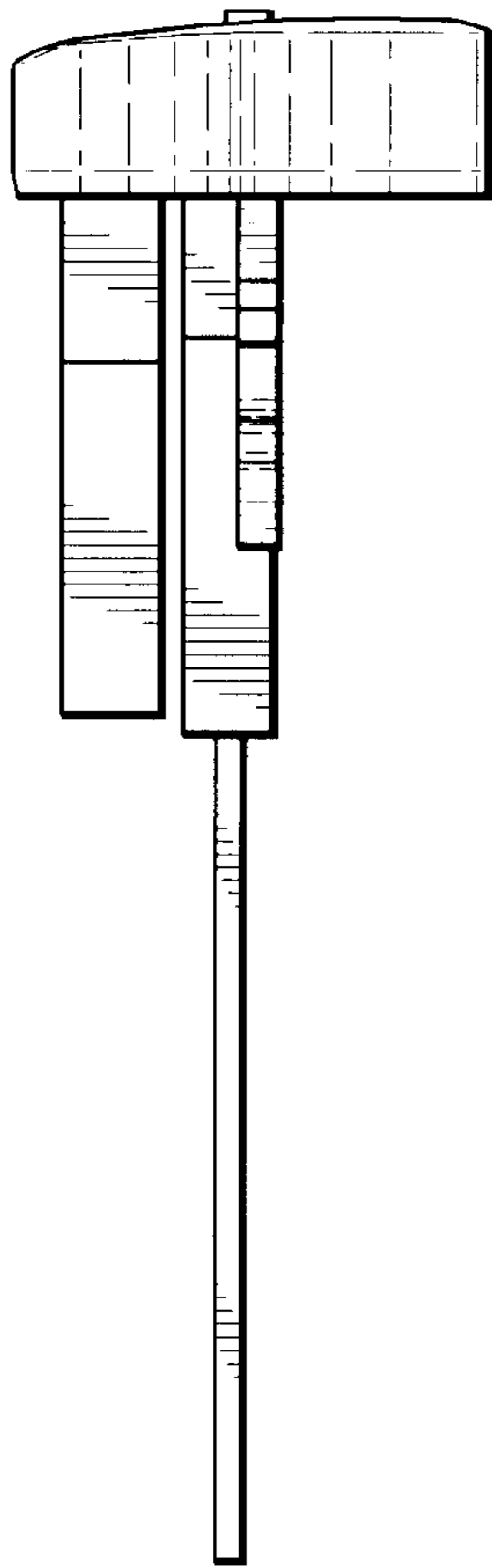


FIG. 6

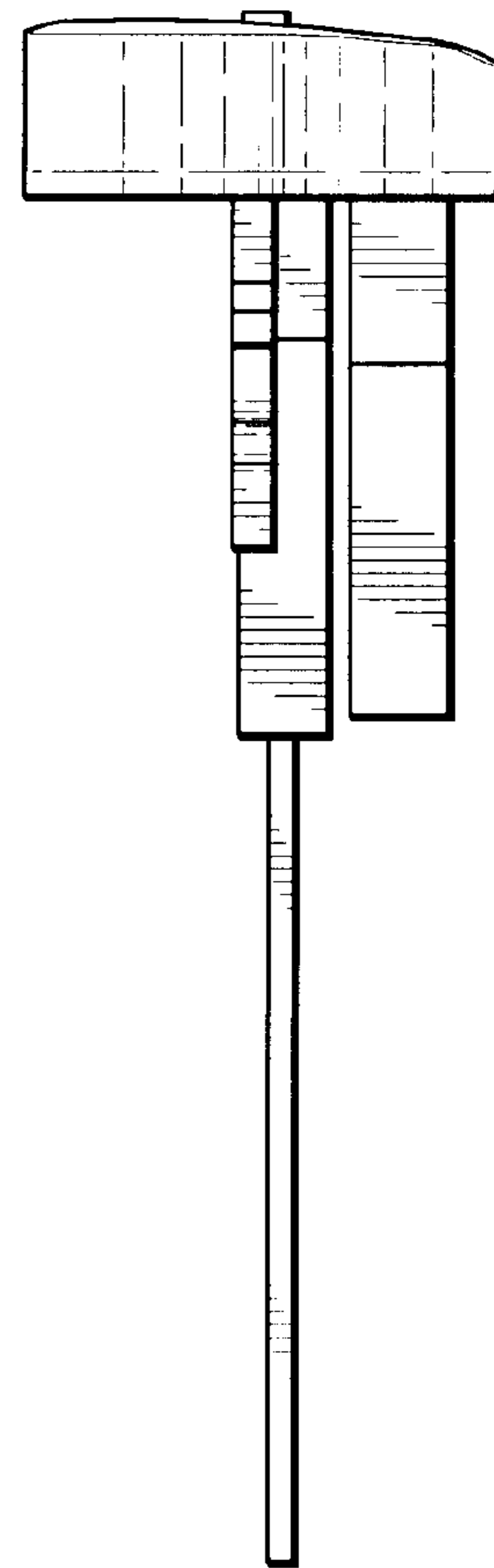


FIG. 7