US00D512970S

(12) **United States Design Patent**
**Hart**

(10) **Patent No.: US D512,970 S**
(45) **Date of Patent: ** Dec. 20, 2005**

(54) **UNIVERSAL LEAD STRAIGHTENER FOR INTEGRATED CIRCUIT DEVICES**

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(73) Assignee: **Topline Corporation**, Garden Grove, CA (US)

(**) Term: **14 Years**

(21) Appl. No.: **29/192,710**

(22) Filed: **Oct. 29, 2003**

(51) **LOC (6) Cl.** ..... **13-03**
(52) **U.S. Cl.** ..... **D13/182**
(58) **Field of Search** ..... D13/182; 174/52.1, 174/250, 260, 265; 140/105, 147; 29/407.1, 840

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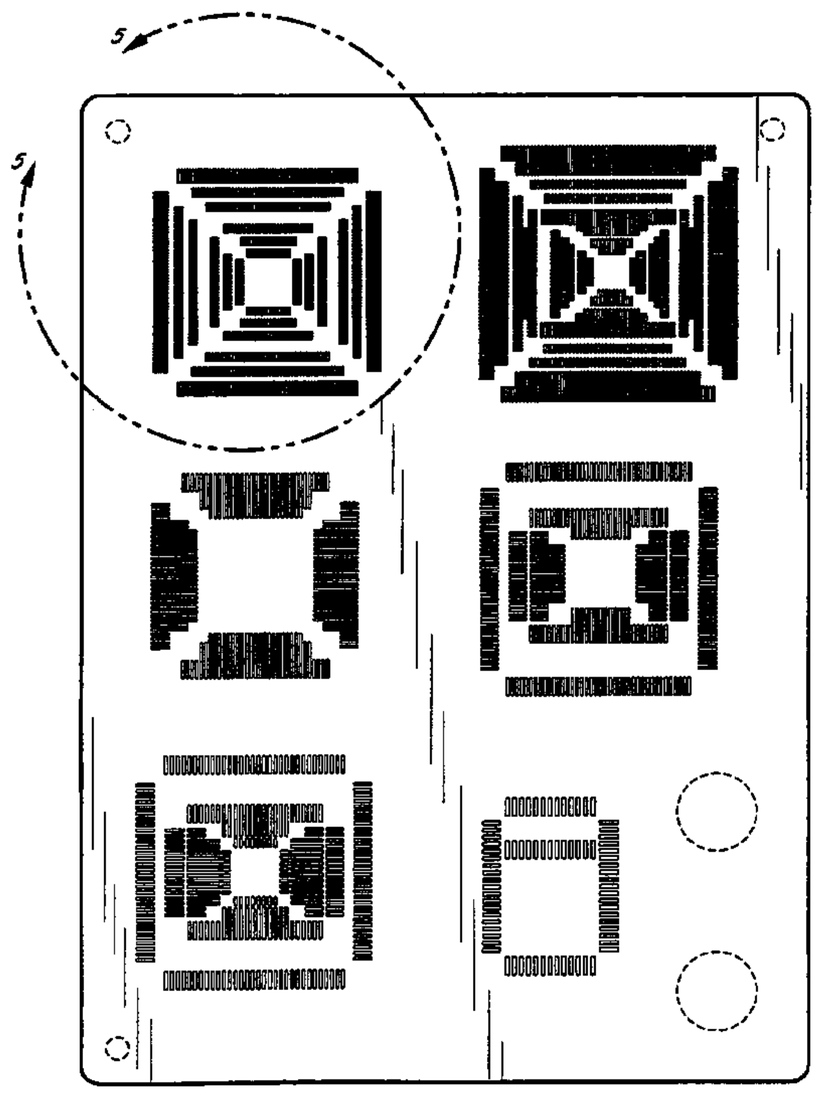
(57) **CLAIM**

The ornamental design for a universal lead straightener for integrated circuit devices, as shown and described.

**DESCRIPTION**

FIG. **1** is a front view of a universal lead straightener for integrated circuit devices showing the ornamental design.
FIG. **2** is a back view thereof.
FIG. **3** is a left side view thereof, which is a mirror image of the right side.
FIG. **4** is a bottom edge view thereof which is a mirror image of a top edge.
FIG. **5** is an enlarged view of a portion of FIG. **1**, taken along the line **5—5** in FIG. **1**; and,
FIG. **6** is a perspective, partially sectionalized view taken along the line **6—6** in FIG. **5** to illustrate the shallow recesses of the arrays and to illustrate in phantom lines the manner in which the leads of an integrated circuit device fit within the shallow recesses.
The broken line showing of the environment is for illustrative purposes only and forms no part of the claimed design.

**1 Claim, 5 Drawing Sheets**



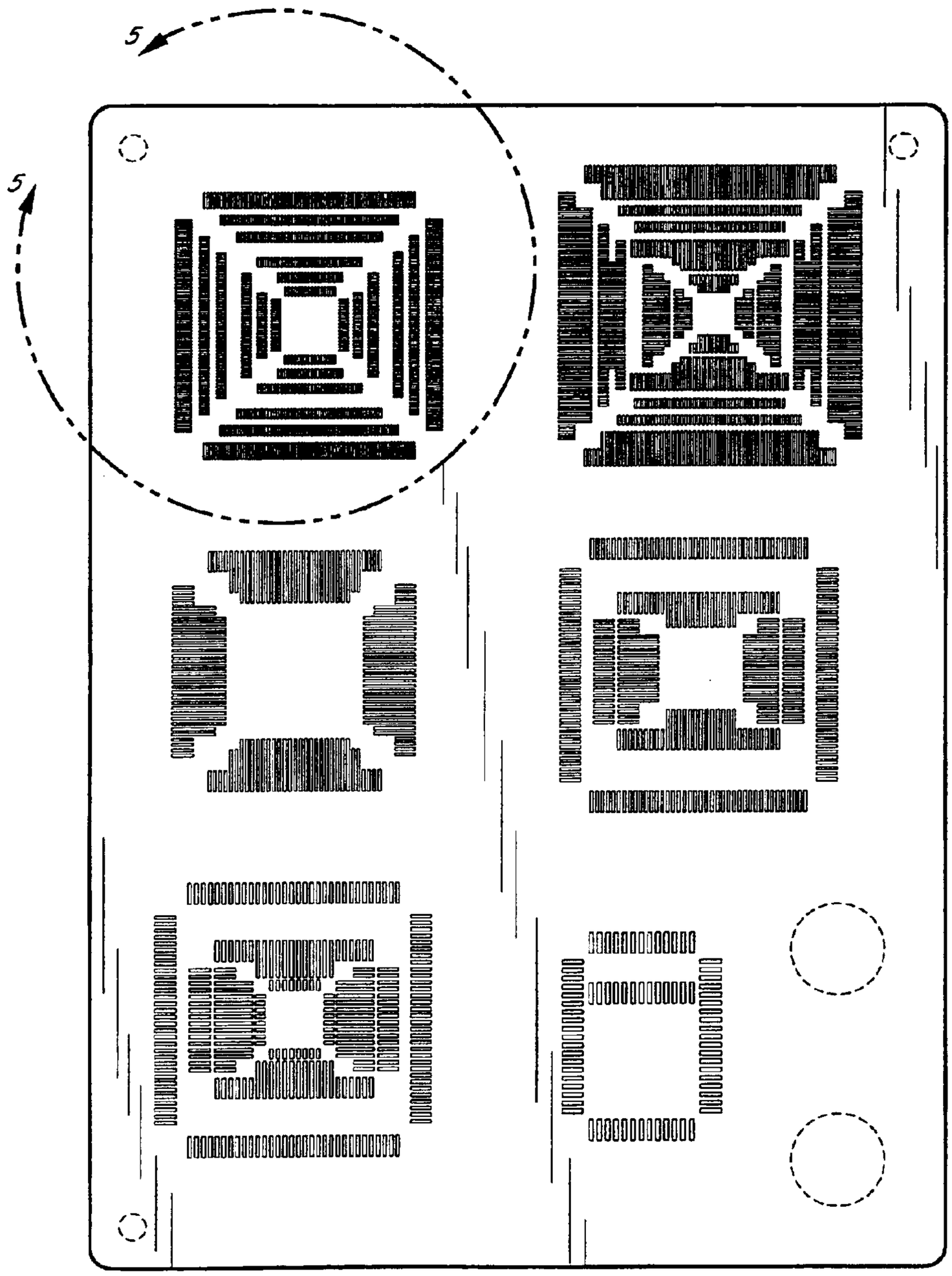



*FIG. 1*

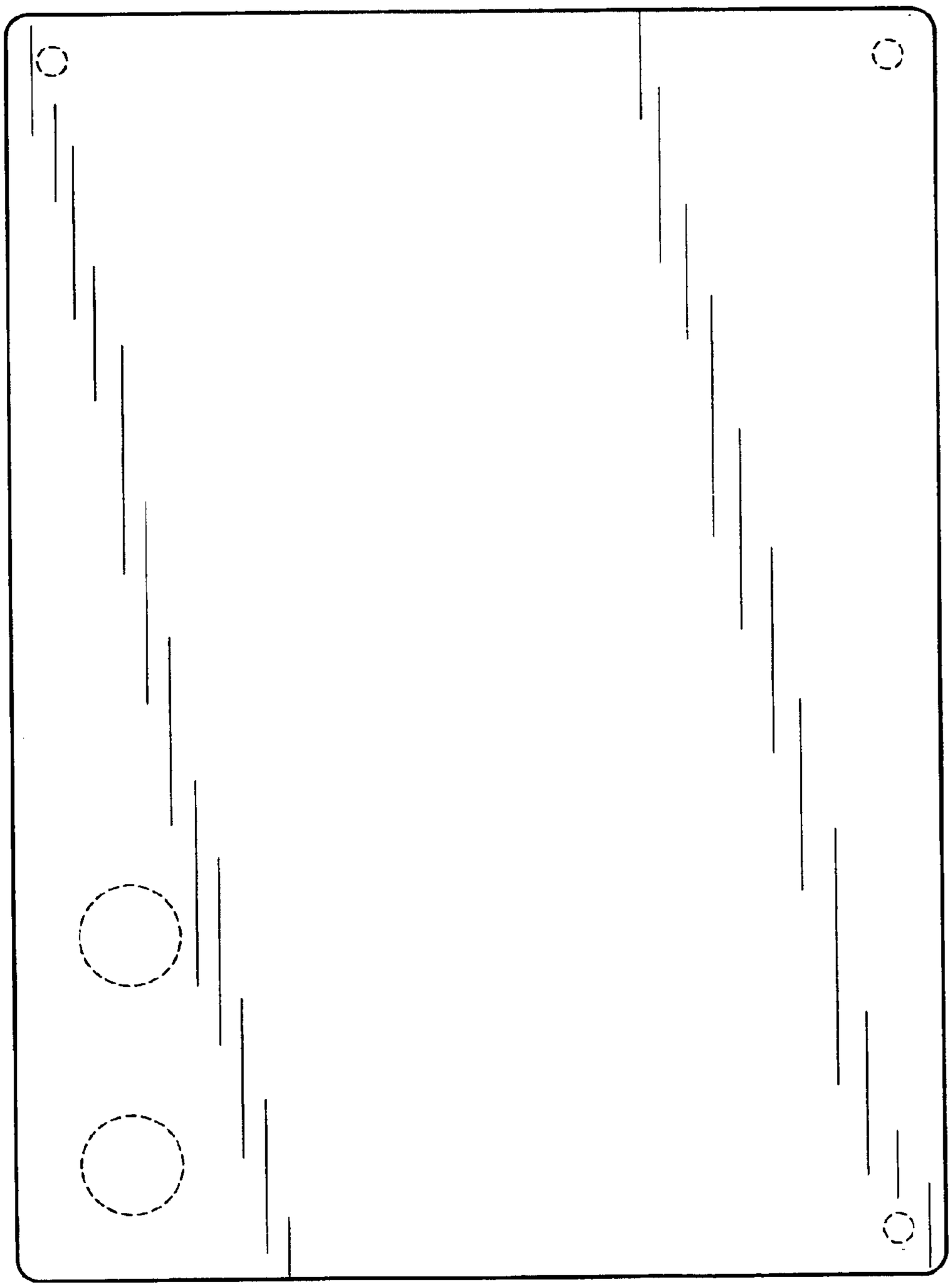


*FIG. 2*

FIG. 3

FIG. 4

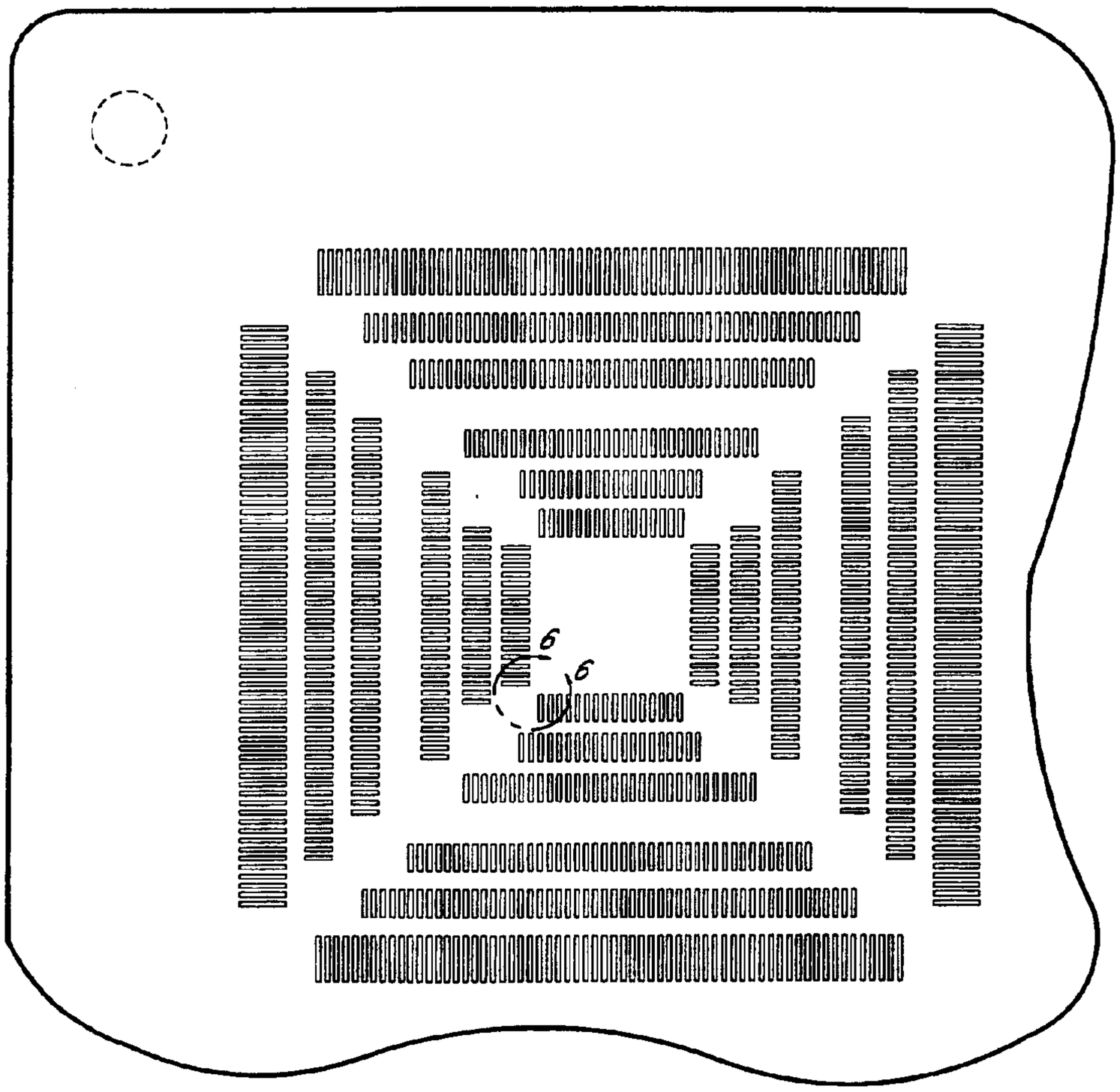



*FIG. 5*

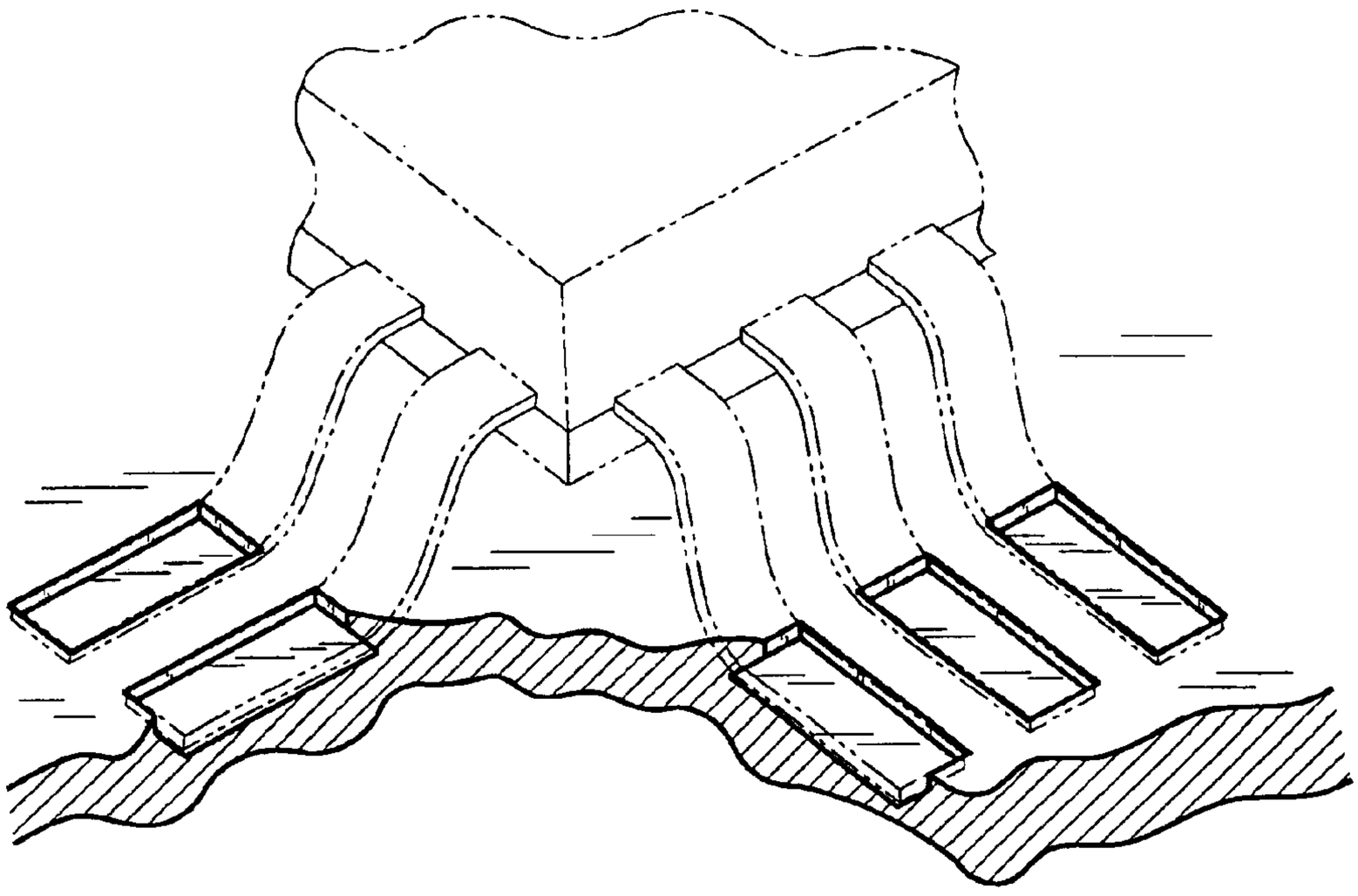


*FIG. 6*