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(12) **United States Design Patent** (10) **Patent No.:** **US D512,969 S**
Sato et al. (45) **Date of Patent:** **** Dec. 20, 2005**

(54) **TWIN AND PARALLEL DIODE WITH LEAD TERMINALS**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (6) Cl.** **13-03**

(52) **U.S. Cl.** **D13/180**

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257/79, 80, 81, 82, 88, 89, 95, 98, 99,
100, 433, 434, 666; 313/483, 498, 500;
361/820; 362/235, 555, 800; 372/45

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(57) **CLAIM**

The ornamental design for twin and parallel diode with lead terminals, as shown.

DESCRIPTION

FIG. 1 is a top view of twin and parallel diode with lead terminals showing our new design;

FIG. 2 is a bottom view thereof;

FIG. 3 is a front view thereof;

FIG. 4 is a rear view thereof;

FIG. 5 is a right side view thereof; and,

FIG. 6 is a left side view thereof.

1 Claim, 1 Drawing Sheet

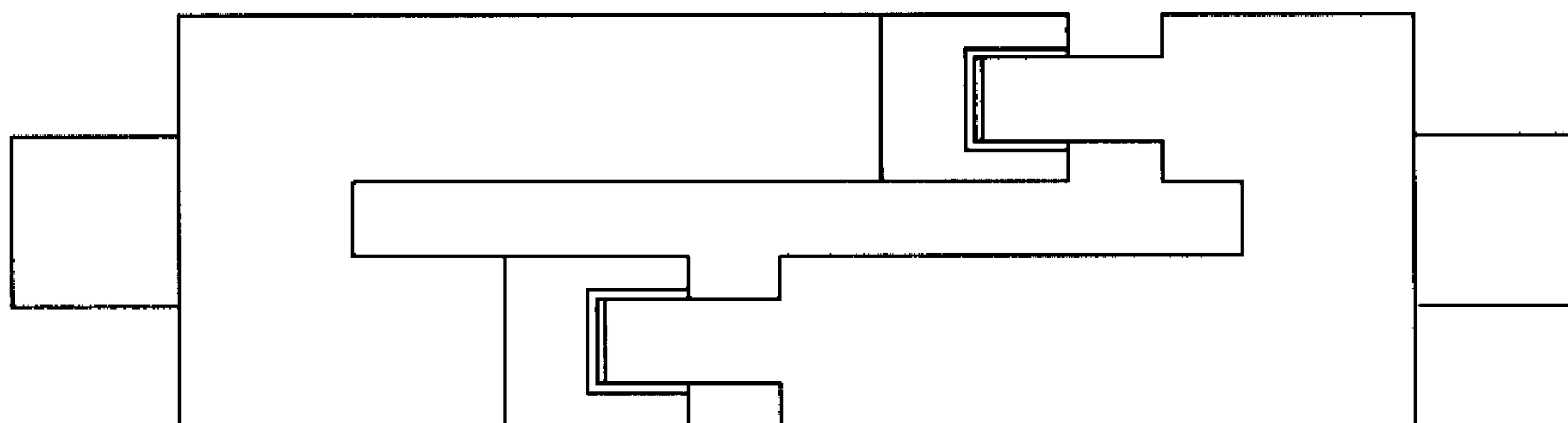


Fig. 1

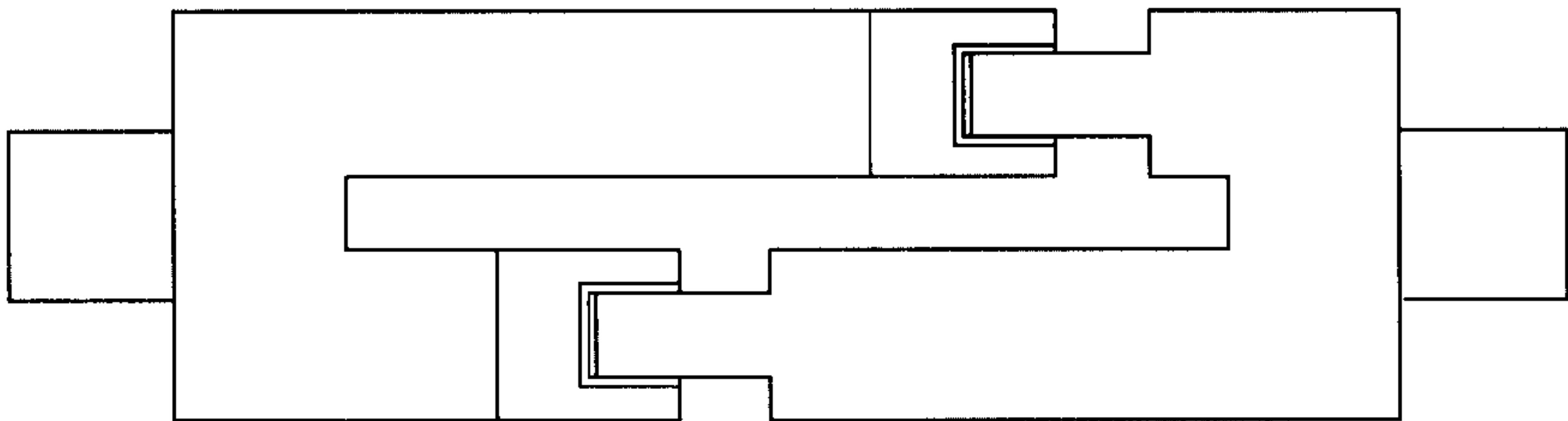


Fig. 2

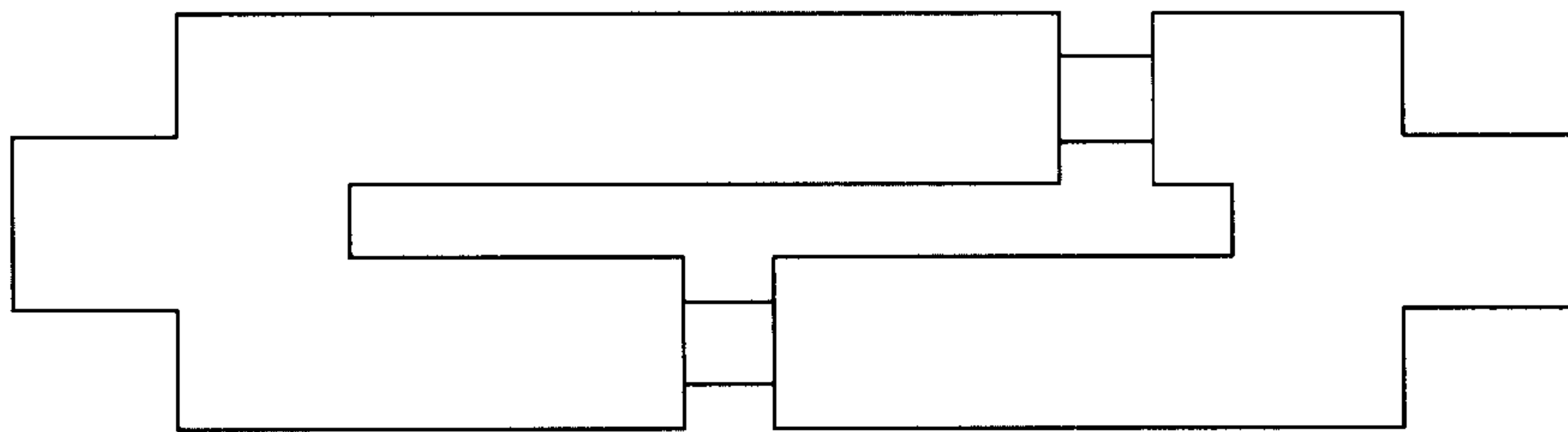


Fig. 3

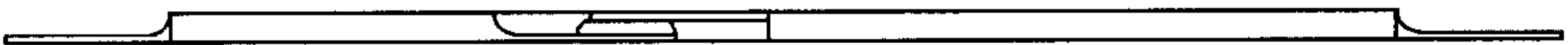


Fig. 4



Fig. 5



Fig. 6

