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(12) **United States Design Patent**
Miller et al.

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(45) **Date of Patent:** **** Nov. 29, 2005**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT TEST HEAD**

D369,983 S * 5/1996 Fisher et al. D10/80
6,642,729 B2 * 11/2003 Kang et al. 324/754

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* cited by examiner

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(**) Term: **14 Years**

(57) **CLAIM**

(21) Appl. No.: **29/201,978**

The ornamental design for a semiconductor integrated circuit test head, as shown and described.

(22) Filed: **Mar. 23, 2004**

DESCRIPTION

(51) **LOC (8) Cl.** **10-04**

(52) **U.S. Cl.** **D10/80**

(58) **Field of Search** D10/75, 78, 80,
D10/102; 324/158.1, 756, 761-762; 439/68,
70, 912

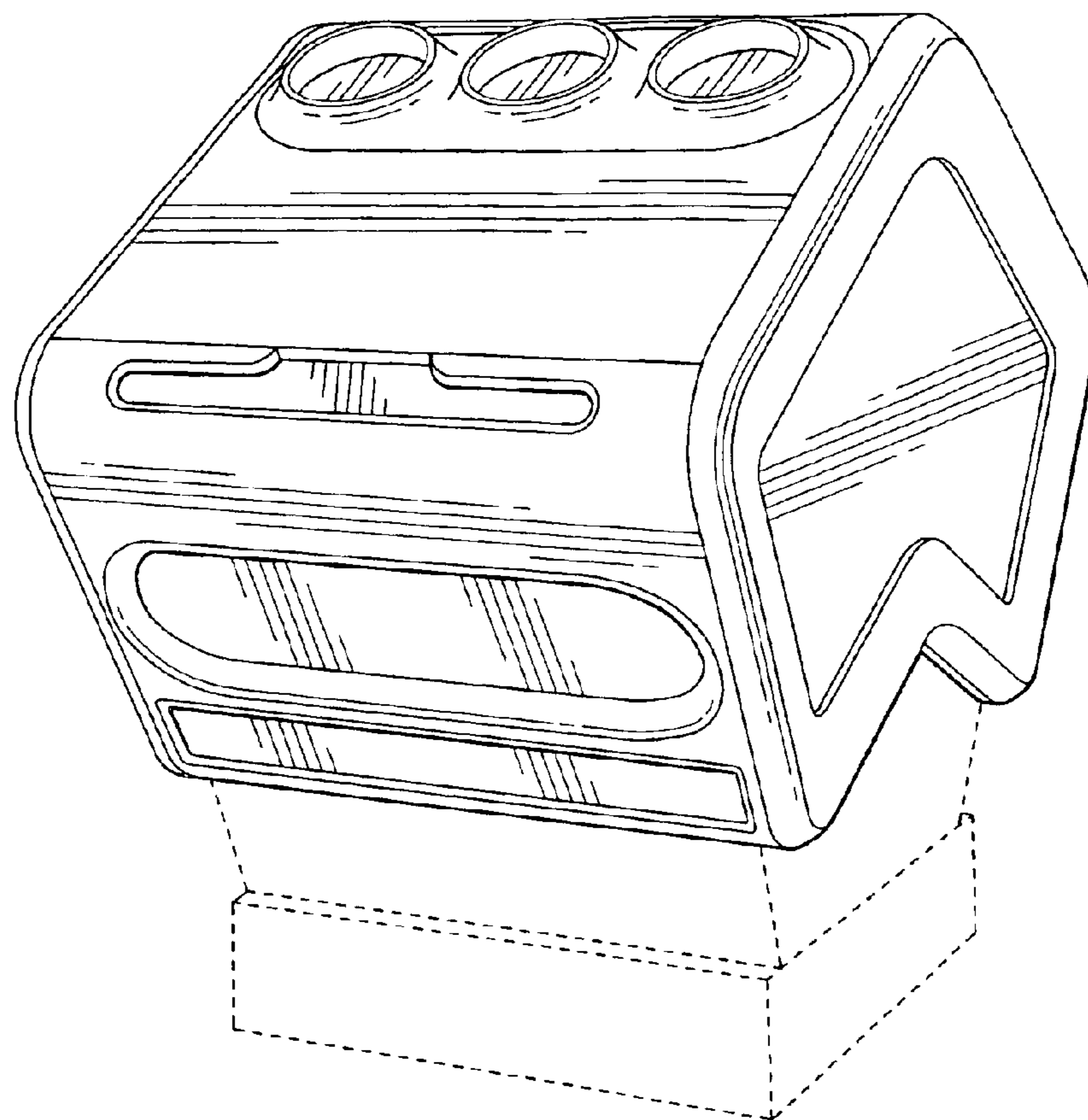
FIG. 1 is a perspective view of a semiconductor integrated circuit test head showing my new design,
FIG. 2 is an end elevation thereof, the opposite end elevation being of corresponding appearance,
FIG. 3 is a side elevation thereof; and,
FIG. 4 is a top plan view thereof.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D345,705 S * 4/1994 Nesbitt et al. D10/80

1 Claim, 2 Drawing Sheets



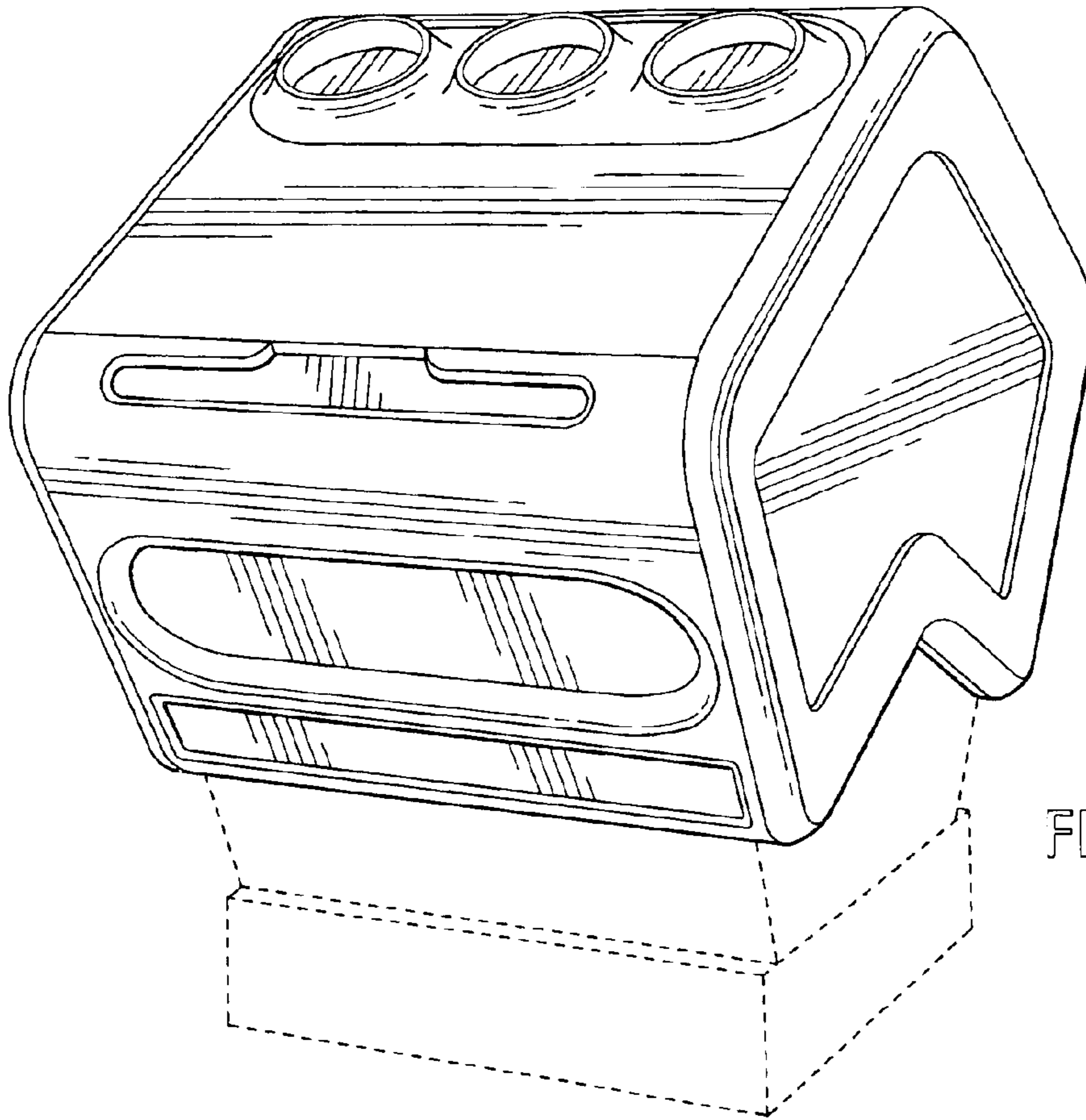


FIG. 1

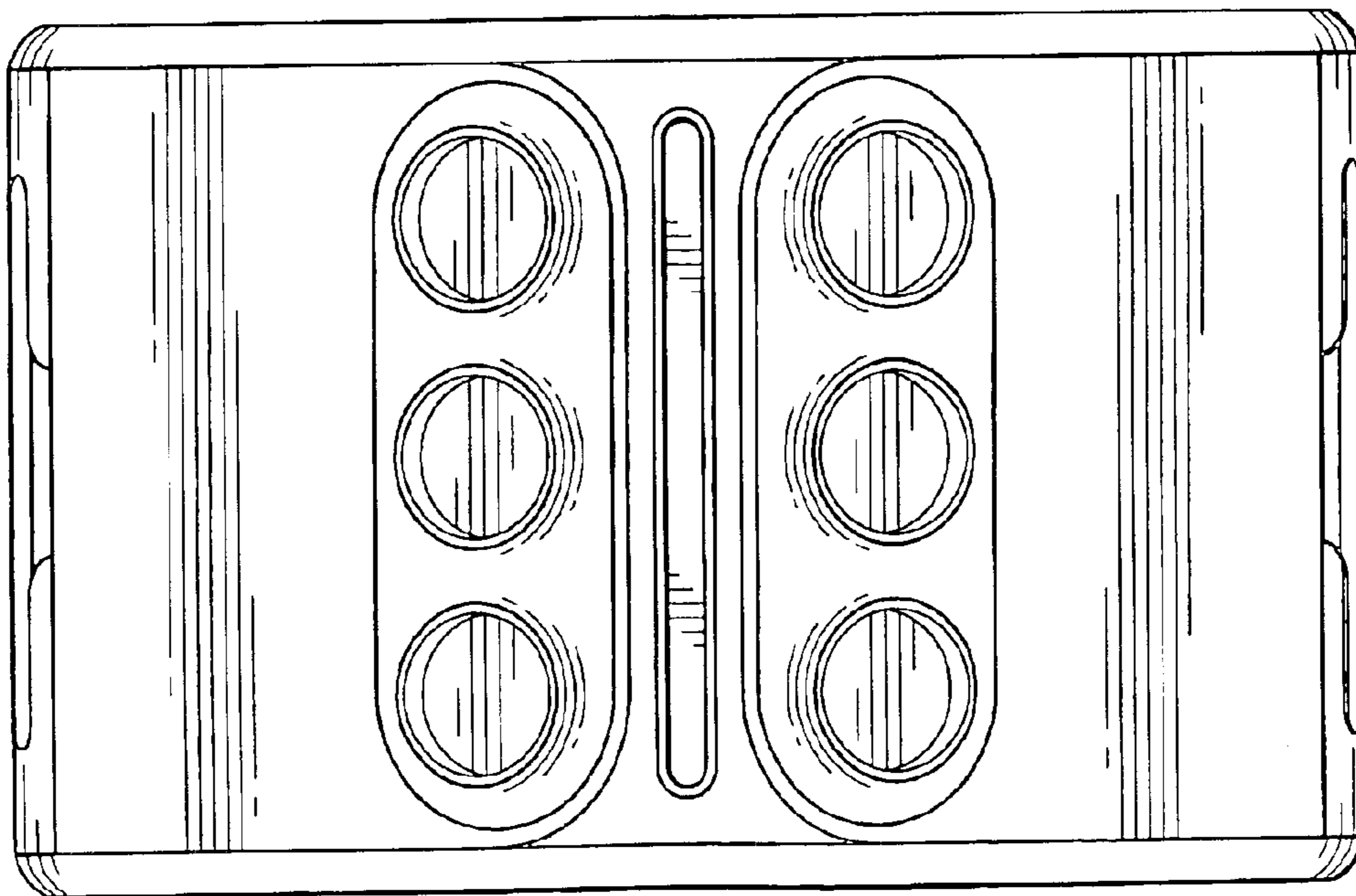


FIG. 4

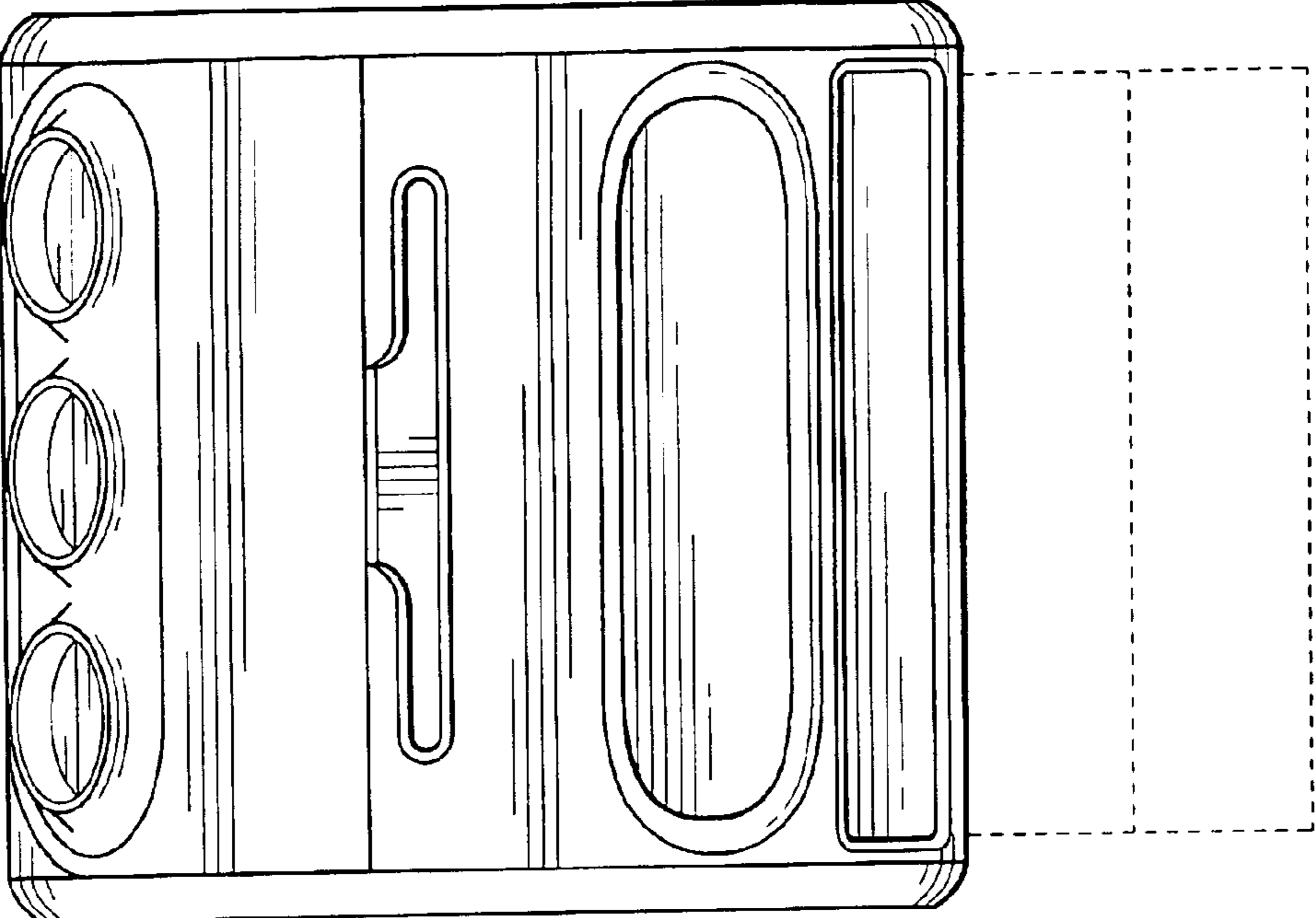


FIG.3

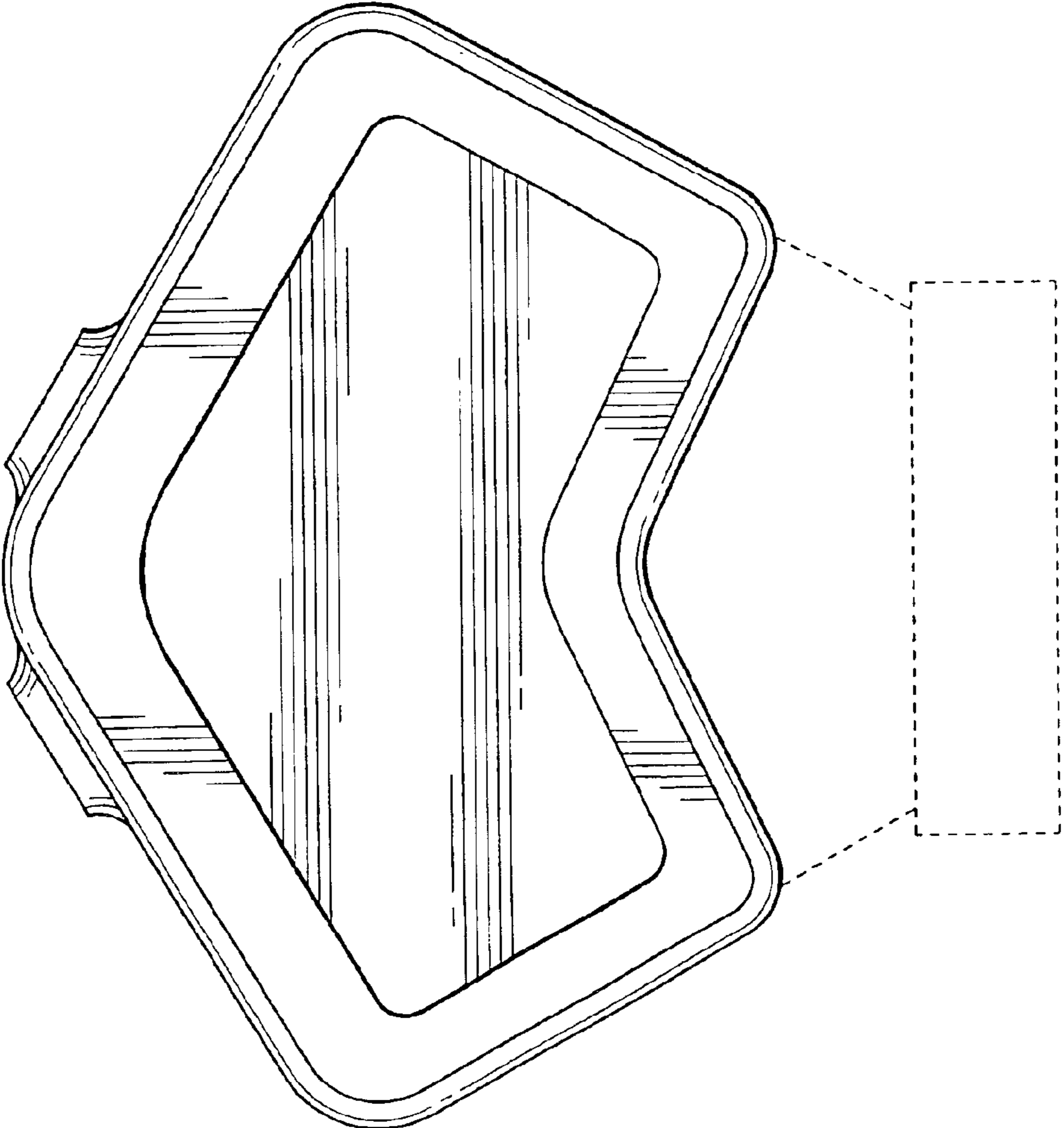


FIG.2