



US00D511331S

(12) **United States Design Patent** (10) **Patent No.:** **US D511,331 S**  
**Horinouchi et al.** (45) **Date of Patent:** **\*\* Nov. 8, 2005**

(54) **OPTOELECTRONIC IC PACKAGE**

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(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

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JP	D1144893	6/2002
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(\*\*) Term: **14 Years**

\* cited by examiner

(21) Appl. No.: **29/191,635**

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(22) Filed: **Oct. 10, 2003**

(74) *Attorney, Agent, or Firm*—Brinks Hofer Gilson & Lione

(30) **Foreign Application Priority Data**

Jul. 9, 2003 (JP) ..... 2003-019764

(57) **CLAIM**

(51) **LOC (8) Cl.** ..... **13-03**

We claim the ornamental design for an optoelectronic IC package, as shown and described.

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Search** ..... D13/182; 174/52.1;  
257/79, 81, 82, 98, 99, 100, 436, 690; 362/800;  
385/92; 438/29

**DESCRIPTION**

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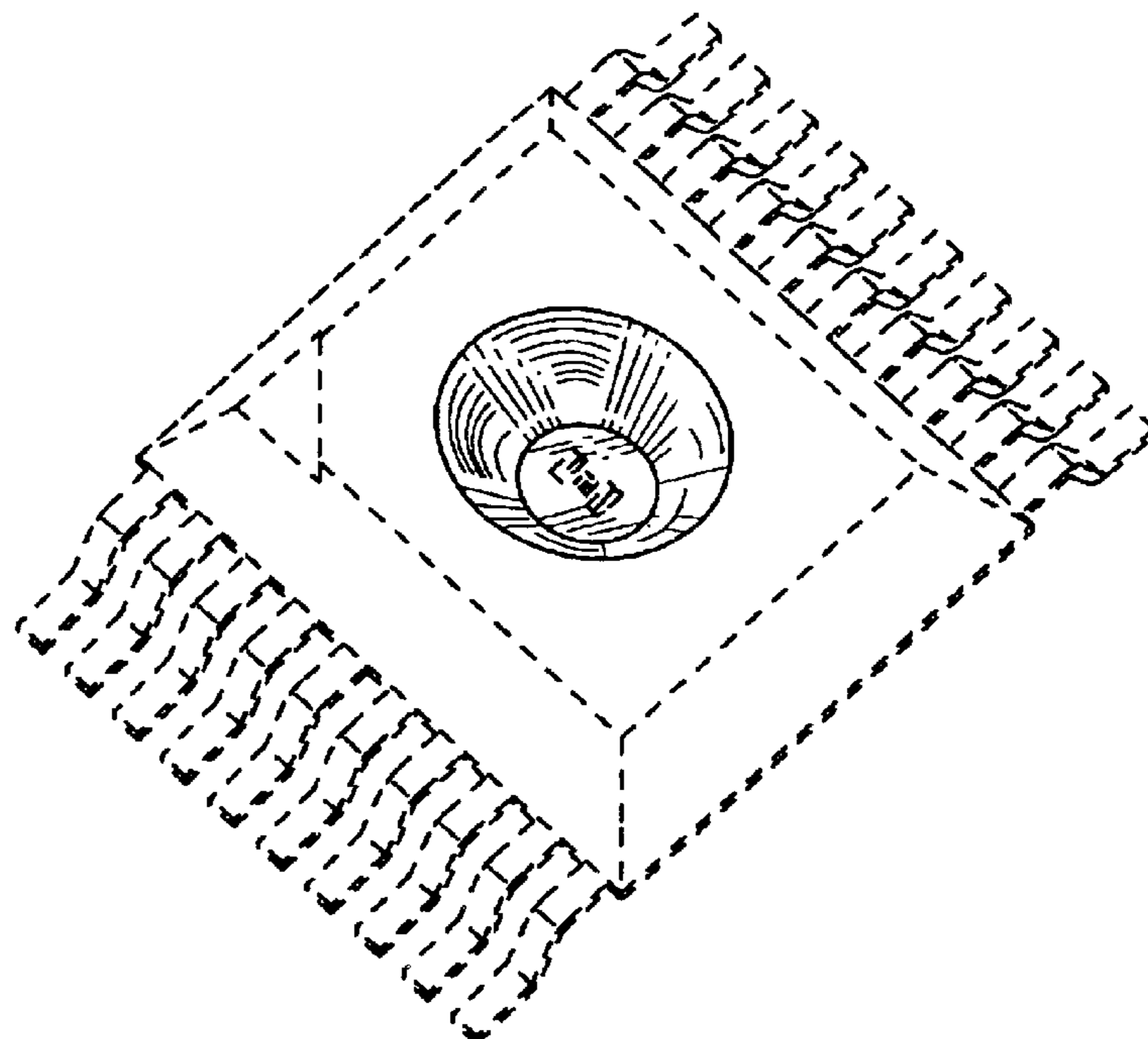
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FIG. 1 is a top perspective view of an optoelectronic IC package of the present invention; FIG. 2 is a first side view thereof; FIG. 3 is a second side view thereof; FIG. 4 is a third side view thereof; FIG. 5 is a top view thereof; and, FIG. 6 is a fourth side view thereof.

The ornamental design which is claimed is shown in solid lines in the drawings. Any broken lines in the drawings are for illustrative purposes only and form no part of the claimed design.

**1 Claim, 2 Drawing Sheets**



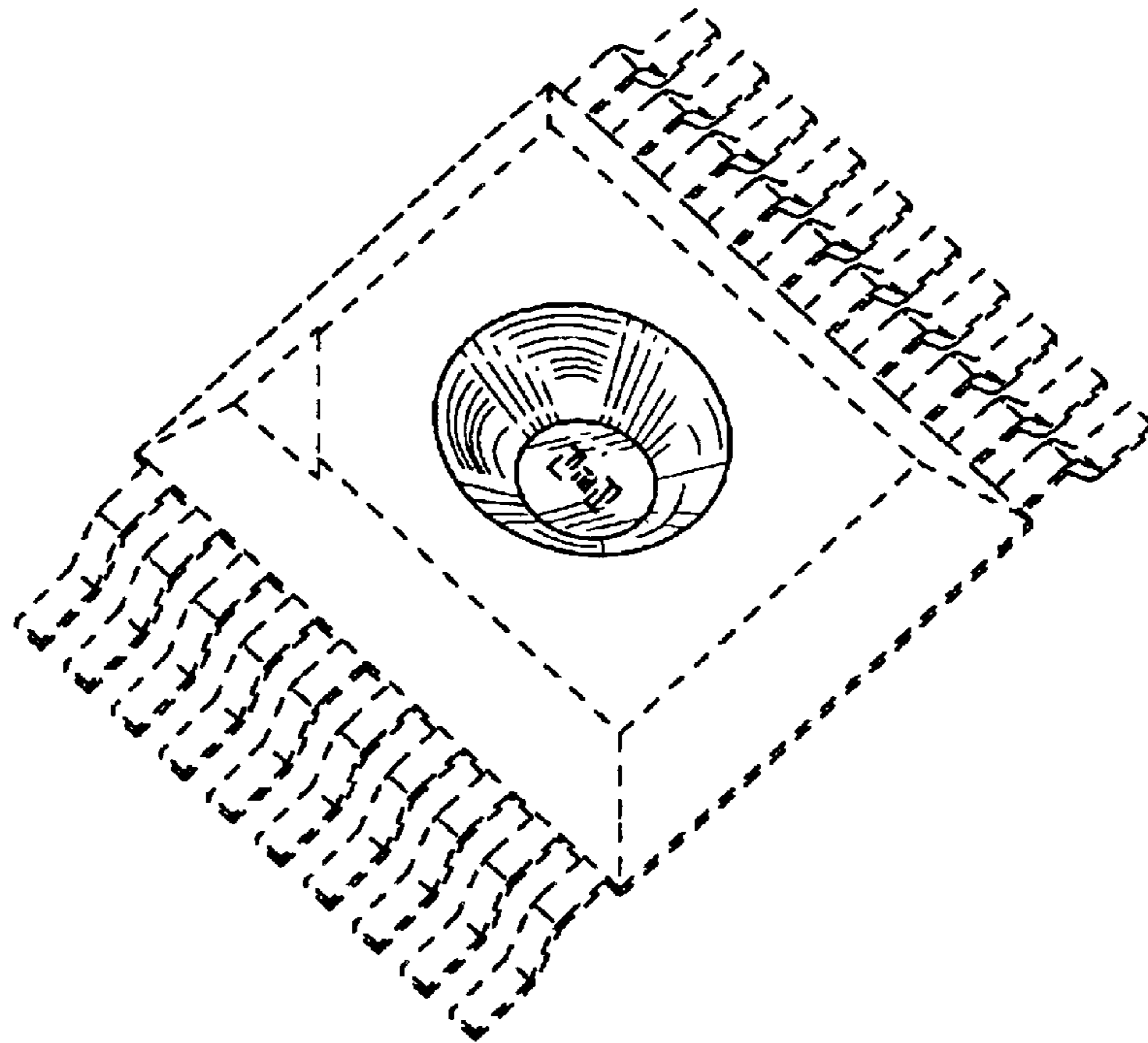


FIG. 1

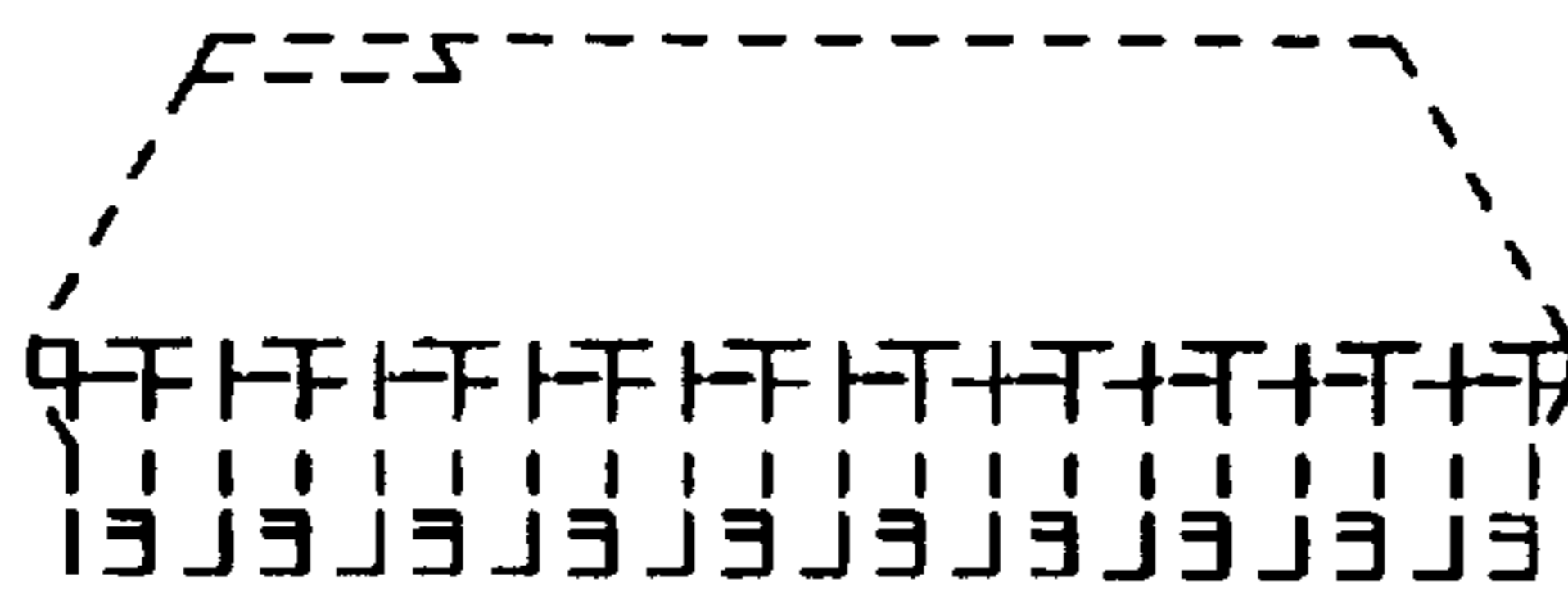


FIG. 2

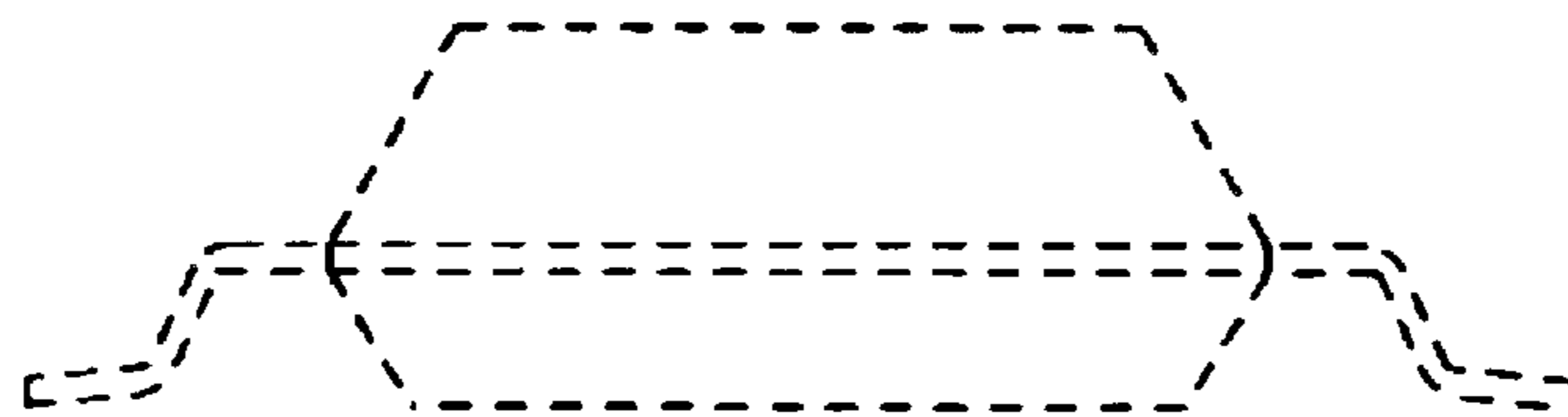


FIG. 3

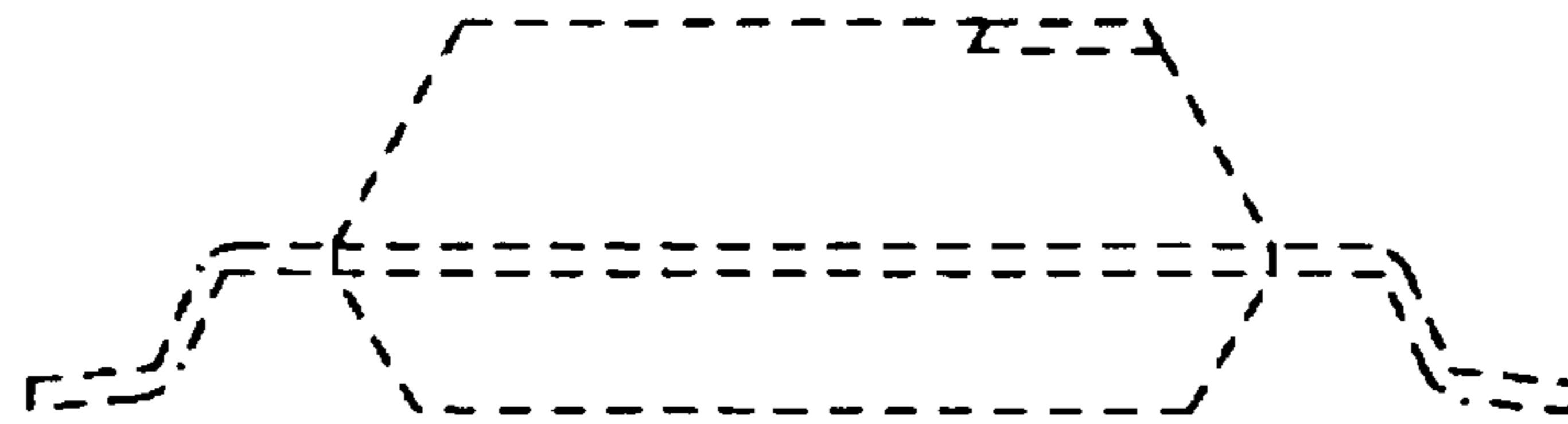


FIG. 4

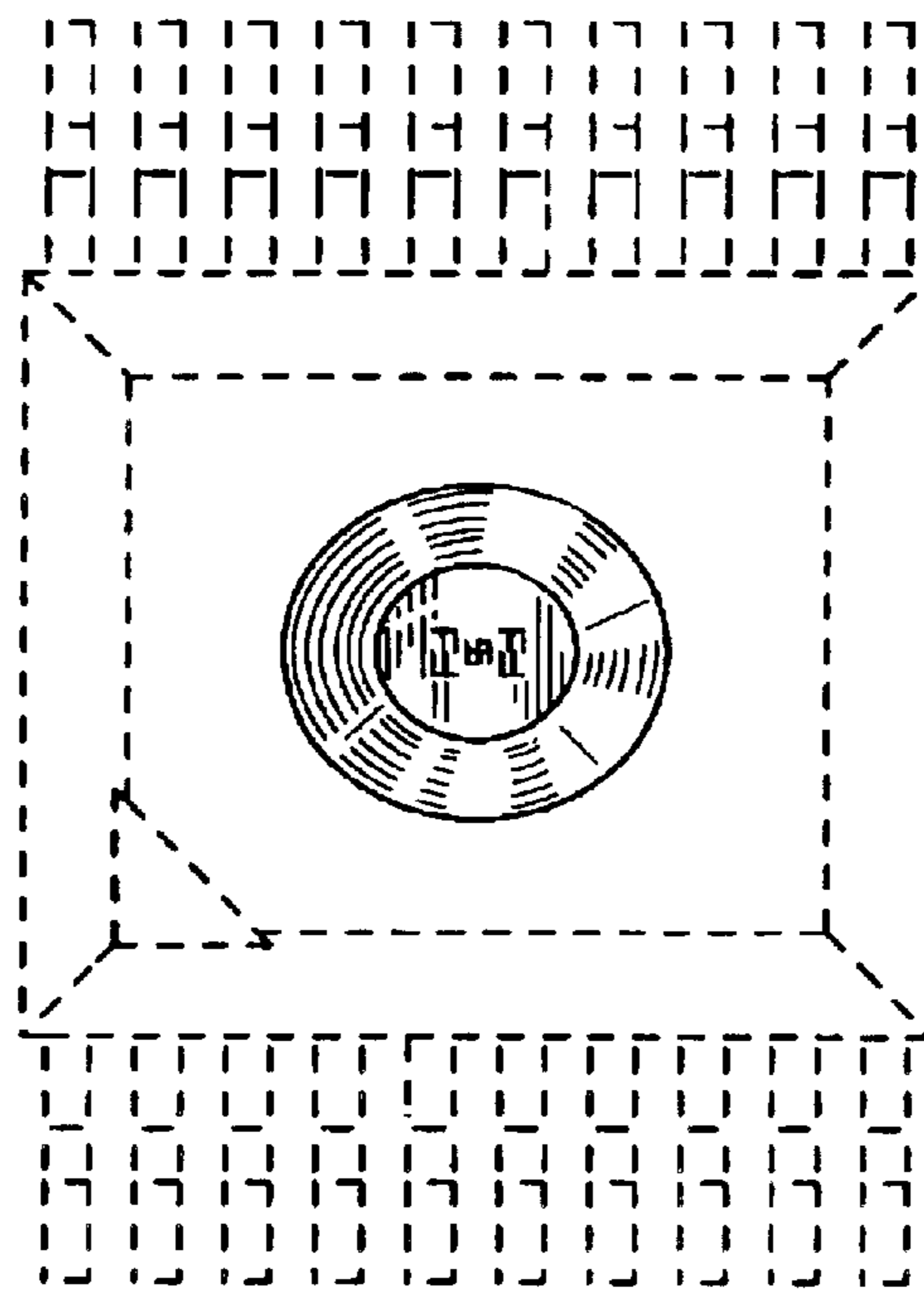


FIG. 5

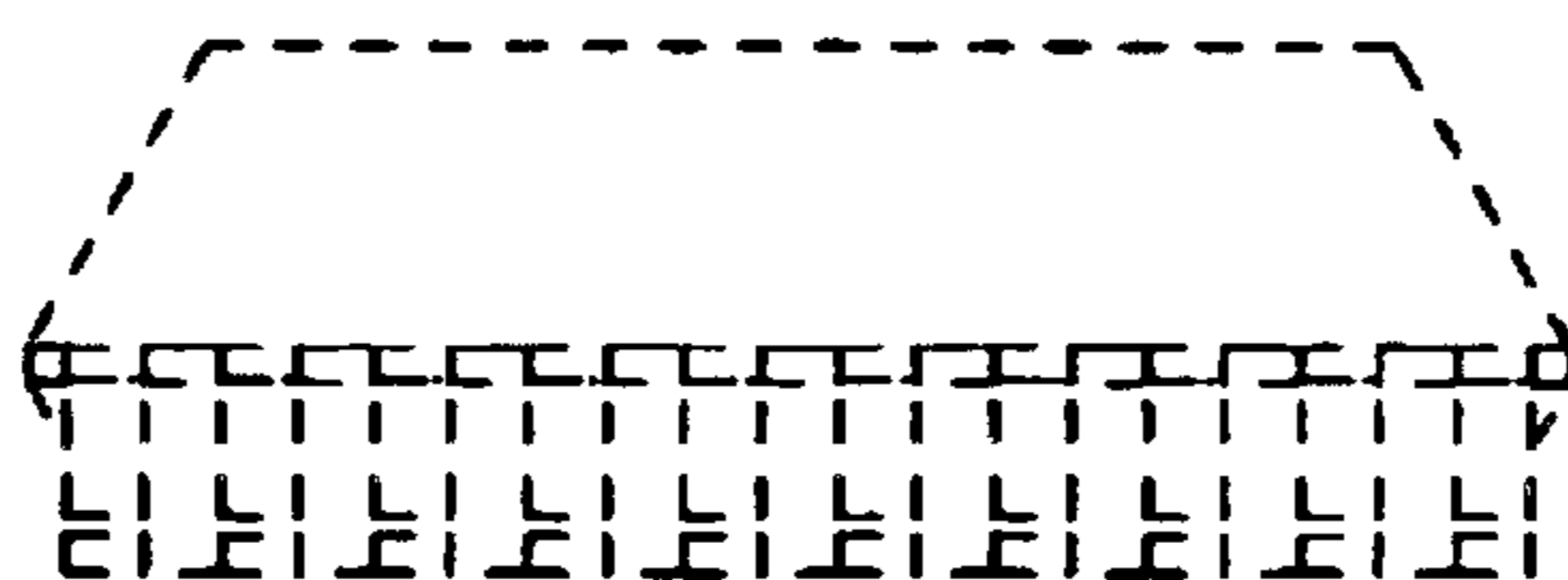


FIG. 6