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(12) United States Design Patent

Hisaishi et al.

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(54) **SEMICONDUCTOR CARRIER**

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(73) Assignee: **Yamaichi Electronics Co., Ltd.**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/210,045**

(22) Filed: **Jul. 27, 2004**

(51) **LOC (8) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 257/666, 257/669, 675, 676; 324/755

(56) **References Cited**

U.S. PATENT DOCUMENTS

D359,028	S	*	6/1995	Siegel et al.	D13/182
5,451,165	A	*	9/1995	Cearley-Cabbiness et al.	439/71
5,519,332	A	*	5/1996	Wood et al.	324/755
5,541,525	A	*	7/1996	Wood et al.	324/755
D401,567	S	*	11/1998	Farnworth et al.	D13/182
2001/0043074	A1	*	11/2001	Hembree et al.	324/755
2004/0016993	A1	*	1/2004	Ham et al.	257/666

* cited by examiner

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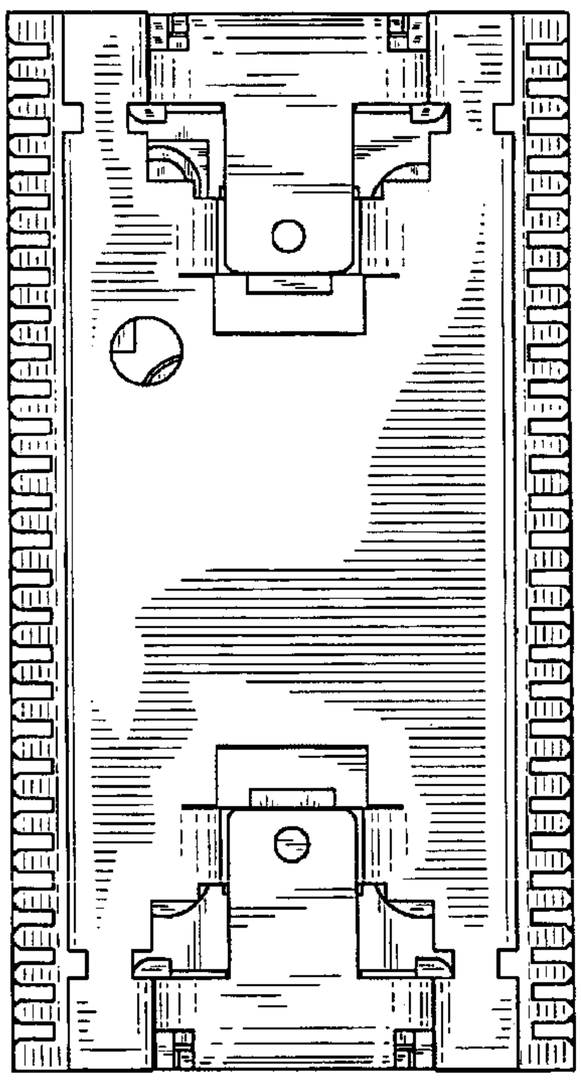
(57) **CLAIM**

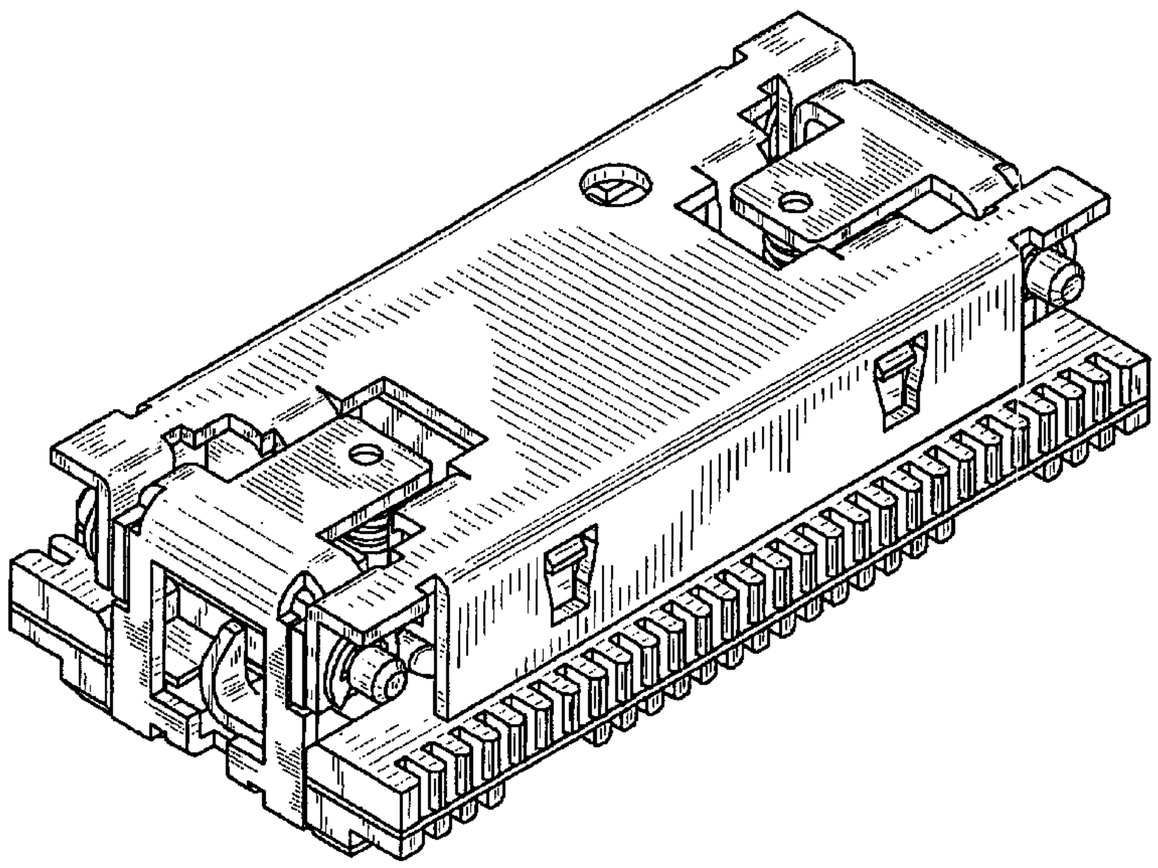
The ornamental design for a semiconductor carrier, as shown and described.

DESCRIPTION

FIG. **1** is a top plan view of a semiconductor carrier of our new design in its entirety;
FIG. **2** is a bottom plan view of our new design;
FIG. **3** is a right end view of our new design;
FIG. **4** is a left end view of our new design;
FIG. **5** is a front view of our new design;
FIG. **6** is a rear view our new design; and,
FIG. **7** is a left, front perspective view of our new design.

1 Claim, 7 Drawing Sheets





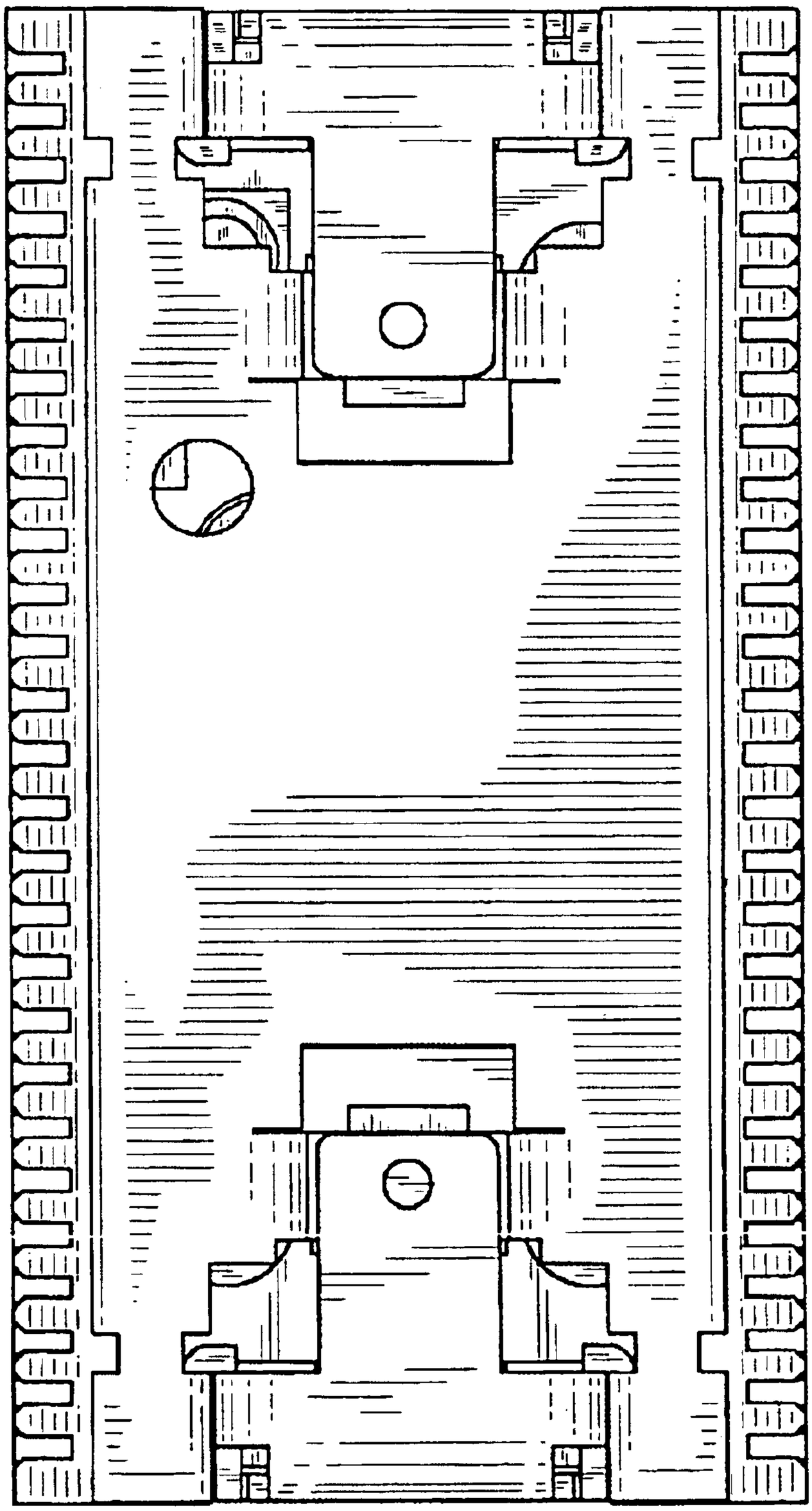


FIG. 1

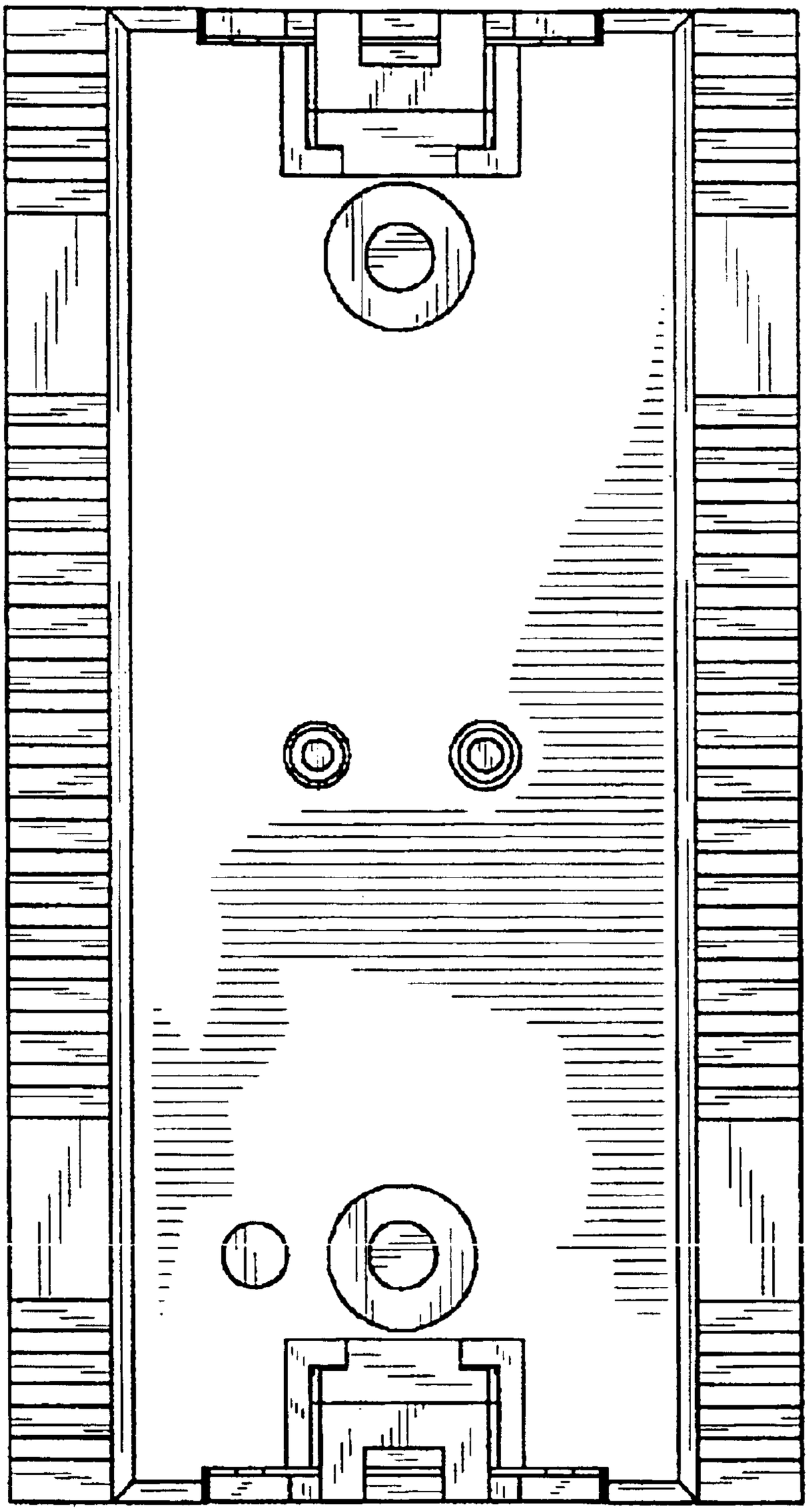


FIG. 2

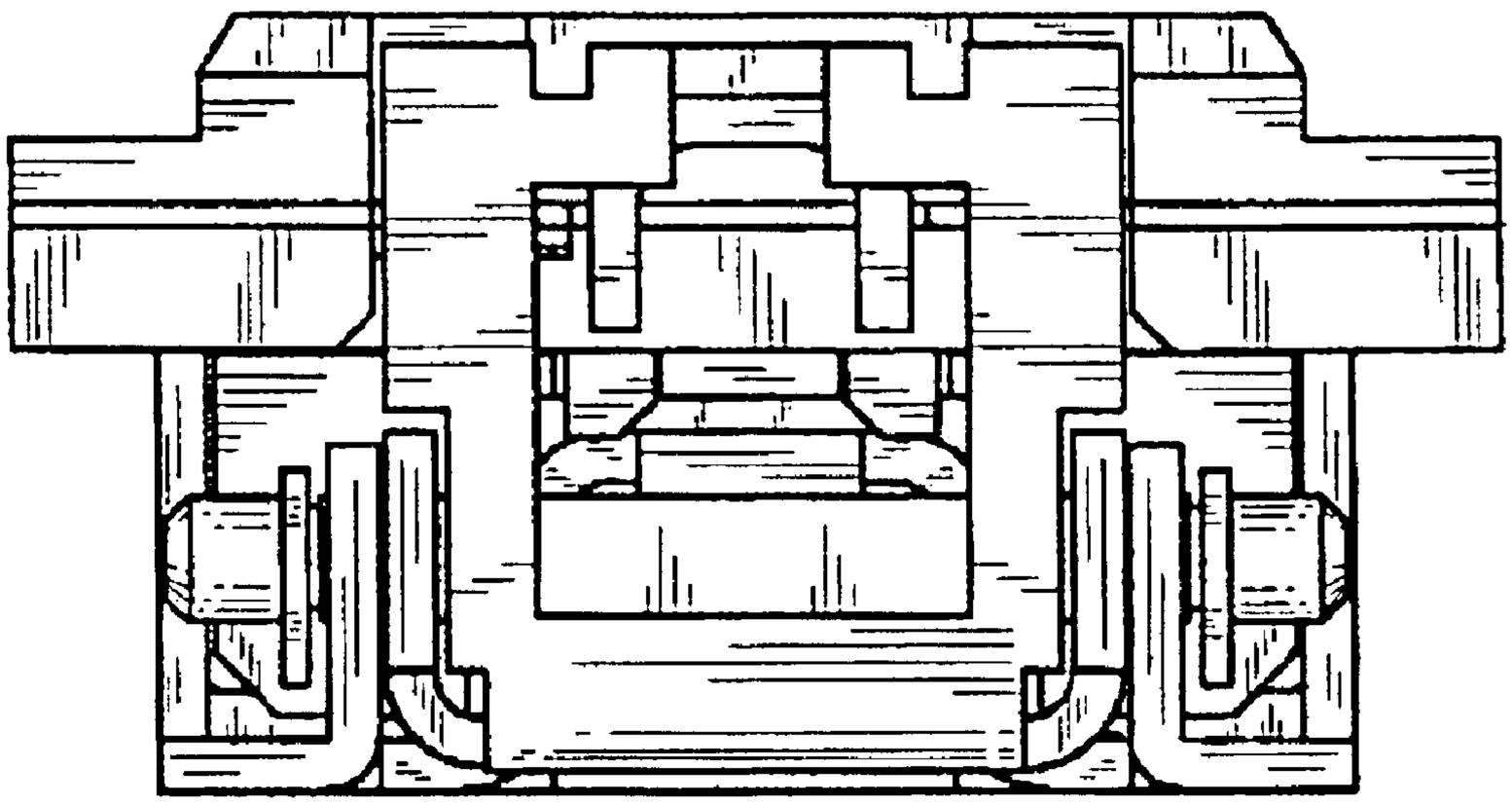


FIG. 3

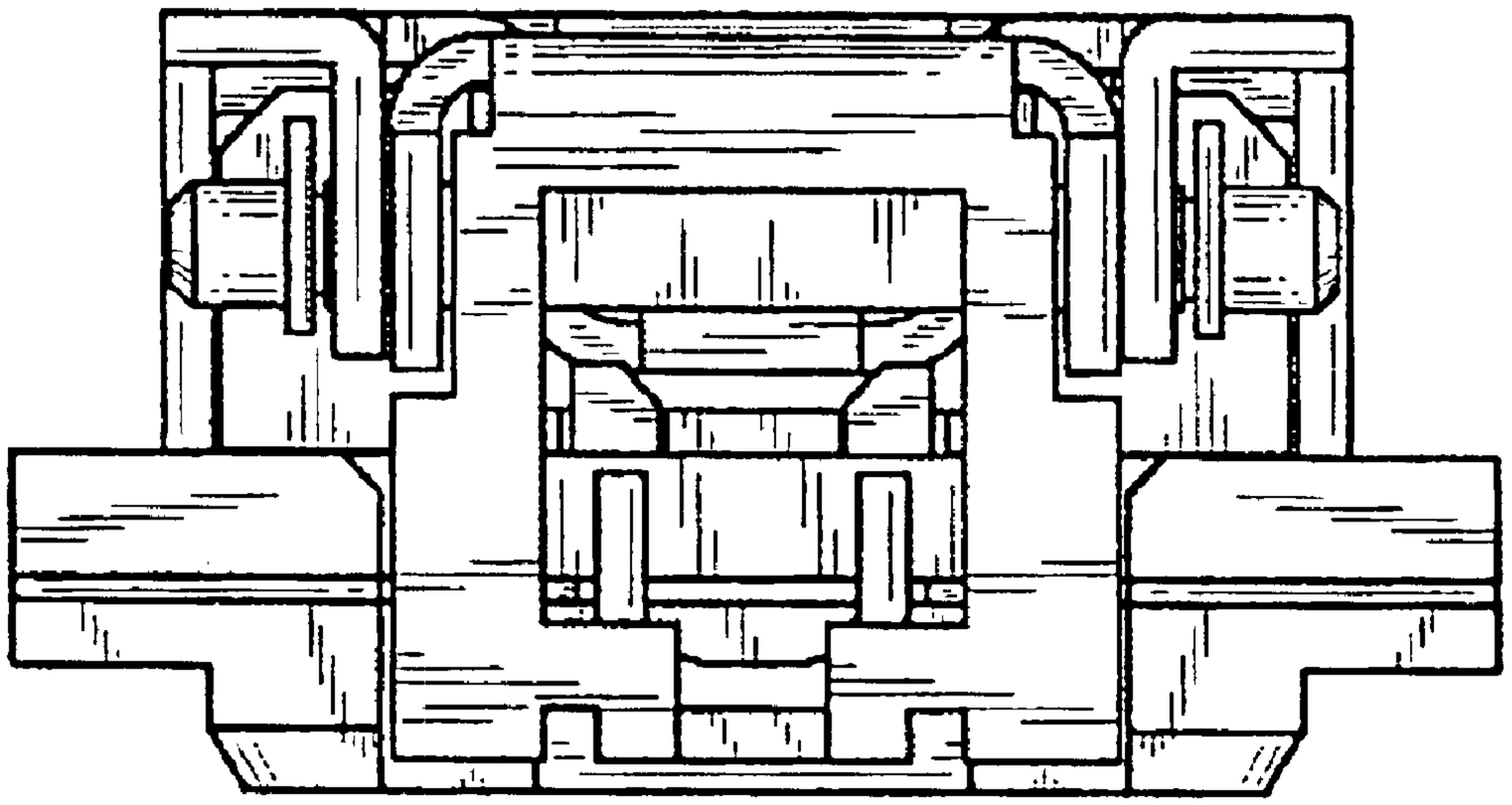


FIG. 4

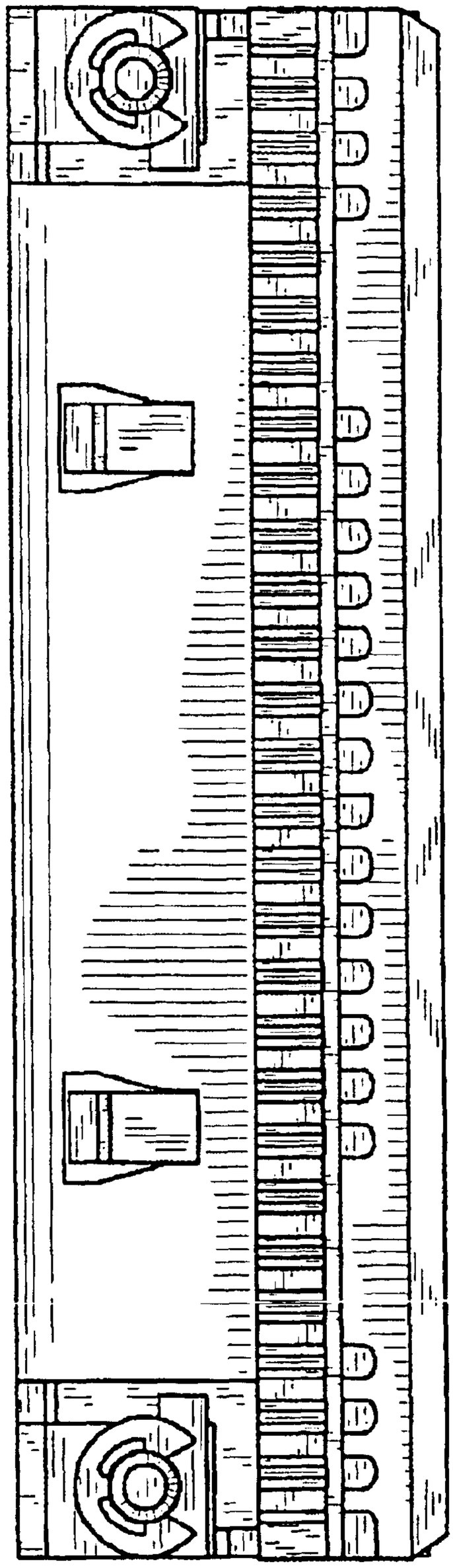


FIG. 5

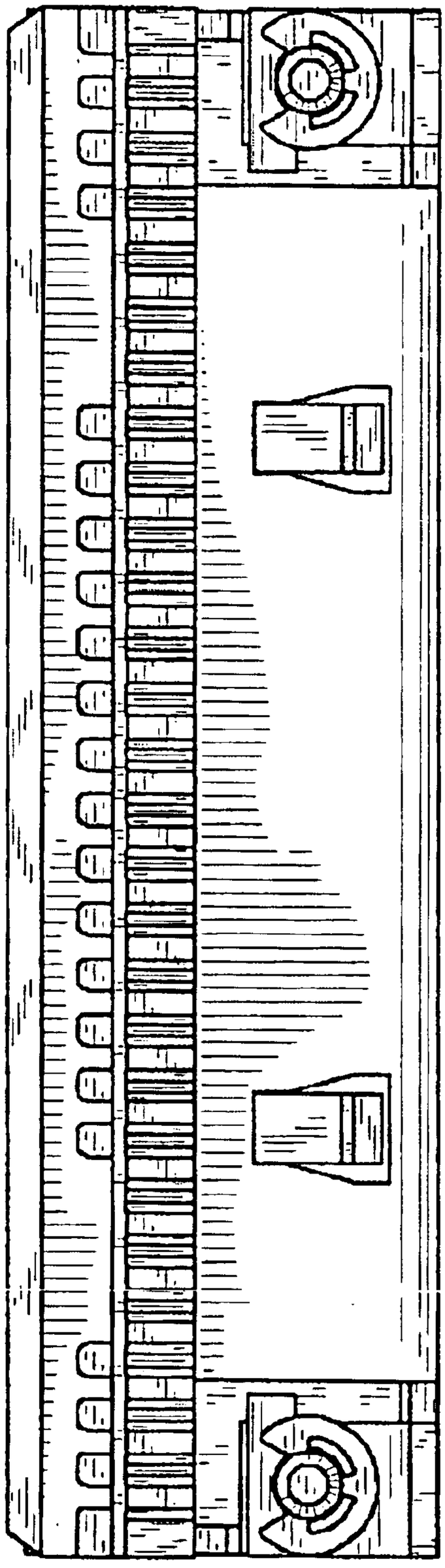


FIG. 6

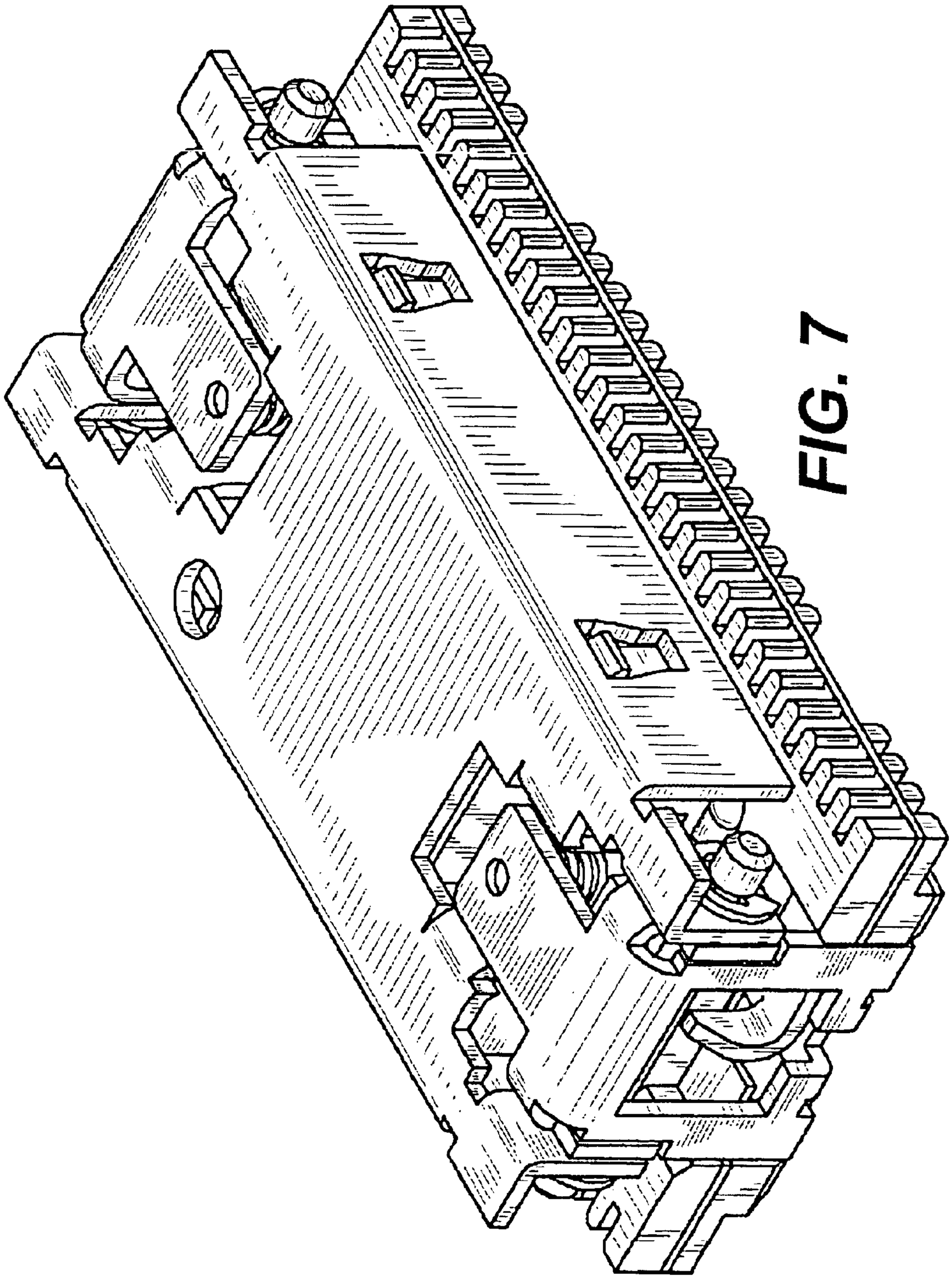


FIG. 7