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(12) United States Design Patent
Standing

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(54) **SEMICONDUCTOR PACKAGE**

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(73) Assignee: **International Rectifier Corporation**, El Segundo, CA (US)

(**) Term: **14 Years**

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(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 174/52.1, 174/52.2; 257/666, 670, 678, 684, 690, 719, 776, 782, 796; 361/760, 771, 774, 792, 798, 820

(56) **References Cited**

U.S. PATENT DOCUMENTS

D379,350	S	*	5/1997	Kerklaan	D13/182
5,949,654	A	*	9/1999	Fukuoka	361/760
5,959,846	A	*	9/1999	Noguchi et al.	361/782
6,130,483	A	*	10/2000	Shizuki et al.	257/778
6,351,027	B1	*	2/2002	Giboney et al.	257/684
6,426,484	B1	*	7/2002	Hembree et al.	219/209
6,646,329	B2	*	11/2003	Estacio et al.	257/666

* cited by examiner

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(57) **CLAIM**

The ornamental design for a semiconductor package, as shown and described.

DESCRIPTION

FIG. **1** is a front elevational view of a semiconductor package, showing our design;
FIG. **2** is a left side elevational view thereof;
FIG. **3** is a top plan view thereof; and,
FIG. **4** is a rear elevational view thereof.
The broken lines shown in the figures are for illustrative purposes only and form no part of the claimed design.

1 Claim, 1 Drawing Sheet

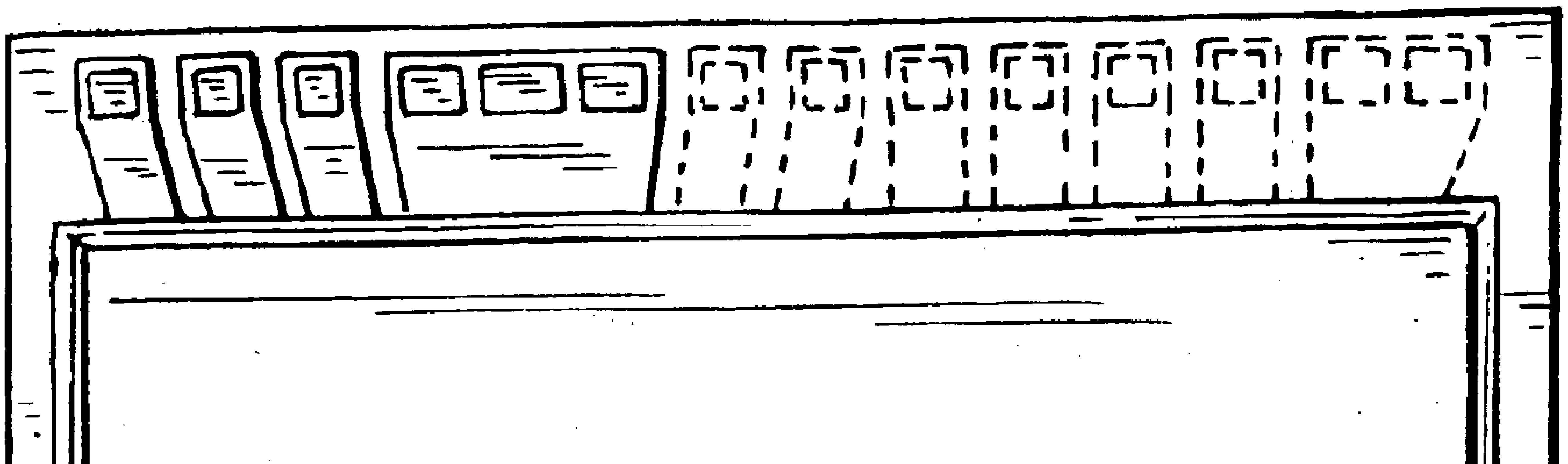

FIG. 1

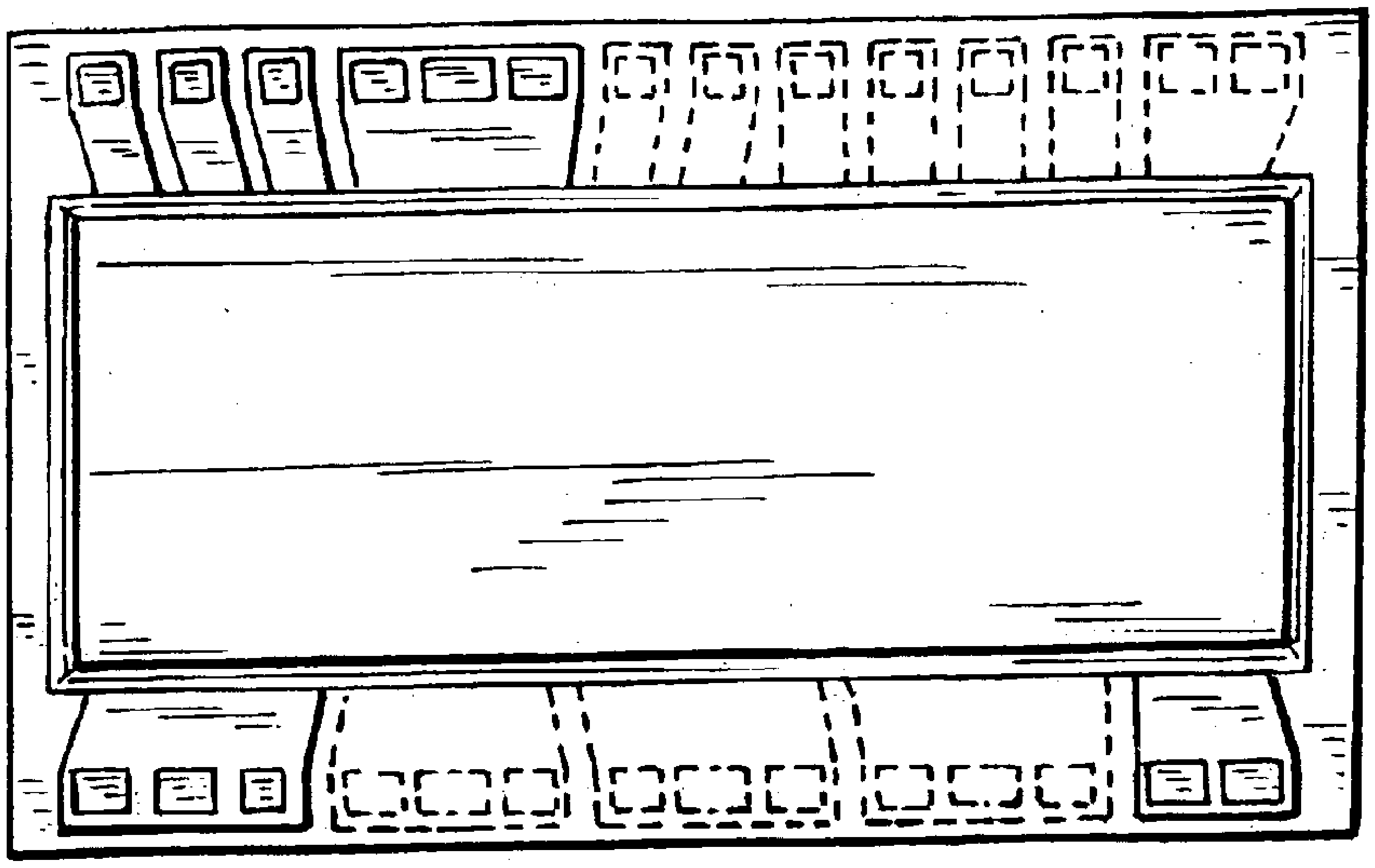

FIG. 2

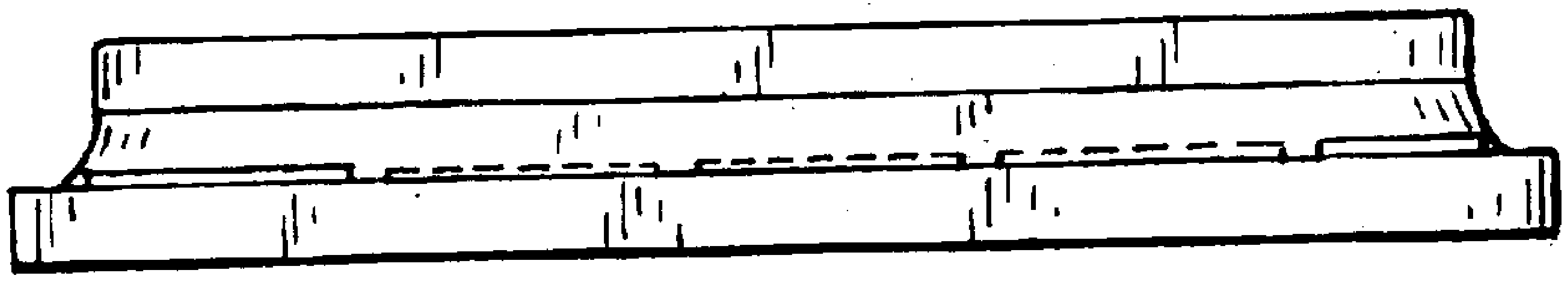

FIG. 3

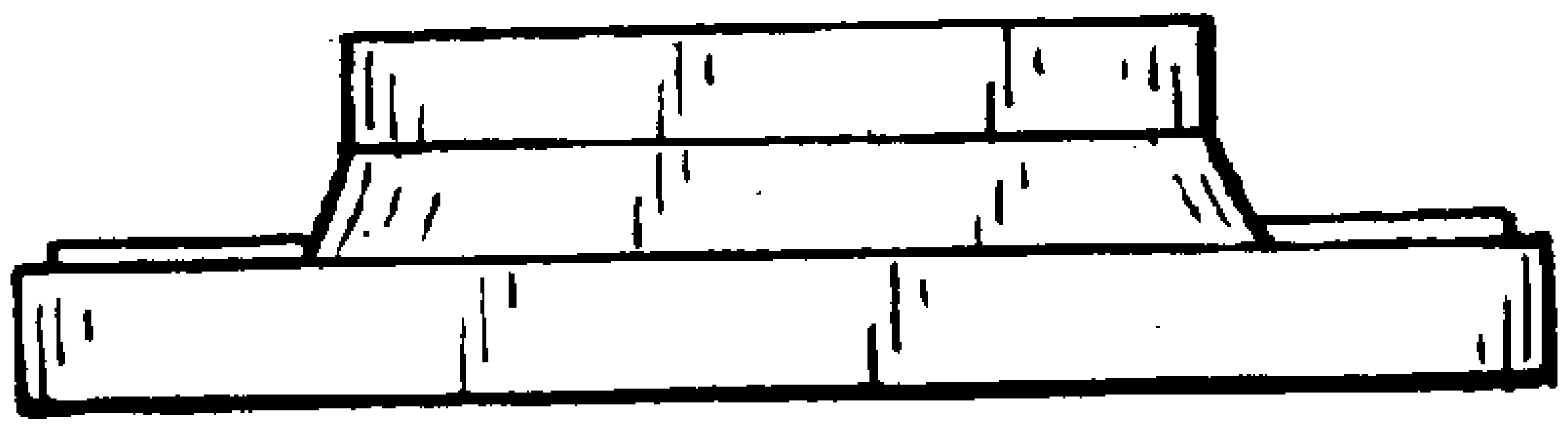

FIG. 4