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(12) **United States Design Patent**
Murakami et al.

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(54) **MEMORY CONTROL EQUIPMENT FOR
COMPUTER**

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(73) Assignee: **NEC Corporation**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/198,678**

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(30) **Foreign Application Priority Data**

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(51) **LOC (7) Cl. 14-02**

(52) **U.S. Cl. D14/356**

(58) **Field of Search D14/356, 358;
361/684, 685**

(56) **References Cited**

U.S. PATENT DOCUMENTS

D333,131 S * 2/1993 Yamamoto D14/357

5,764,480 A * 6/1998 Crump et al. 361/685
D420,336 S * 2/2000 Tanaka D14/389
6,188,571 B1 * 2/2001 Roganti et al. 361/685
D447,746 S * 9/2001 Tonozuka et al. D14/356

* cited by examiner

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(57) **CLAIM**

The ornamental design for a memory control equipment for computer, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of the top, front and right side of a memory control equipment for computer showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a left side elevational view thereof;

FIG. 5 is a right side elevational view thereof;

FIG. 6 is a top plan view thereof; and,

FIG. 7 is a bottom plan view thereof.

1 Claim, 5 Drawing Sheets

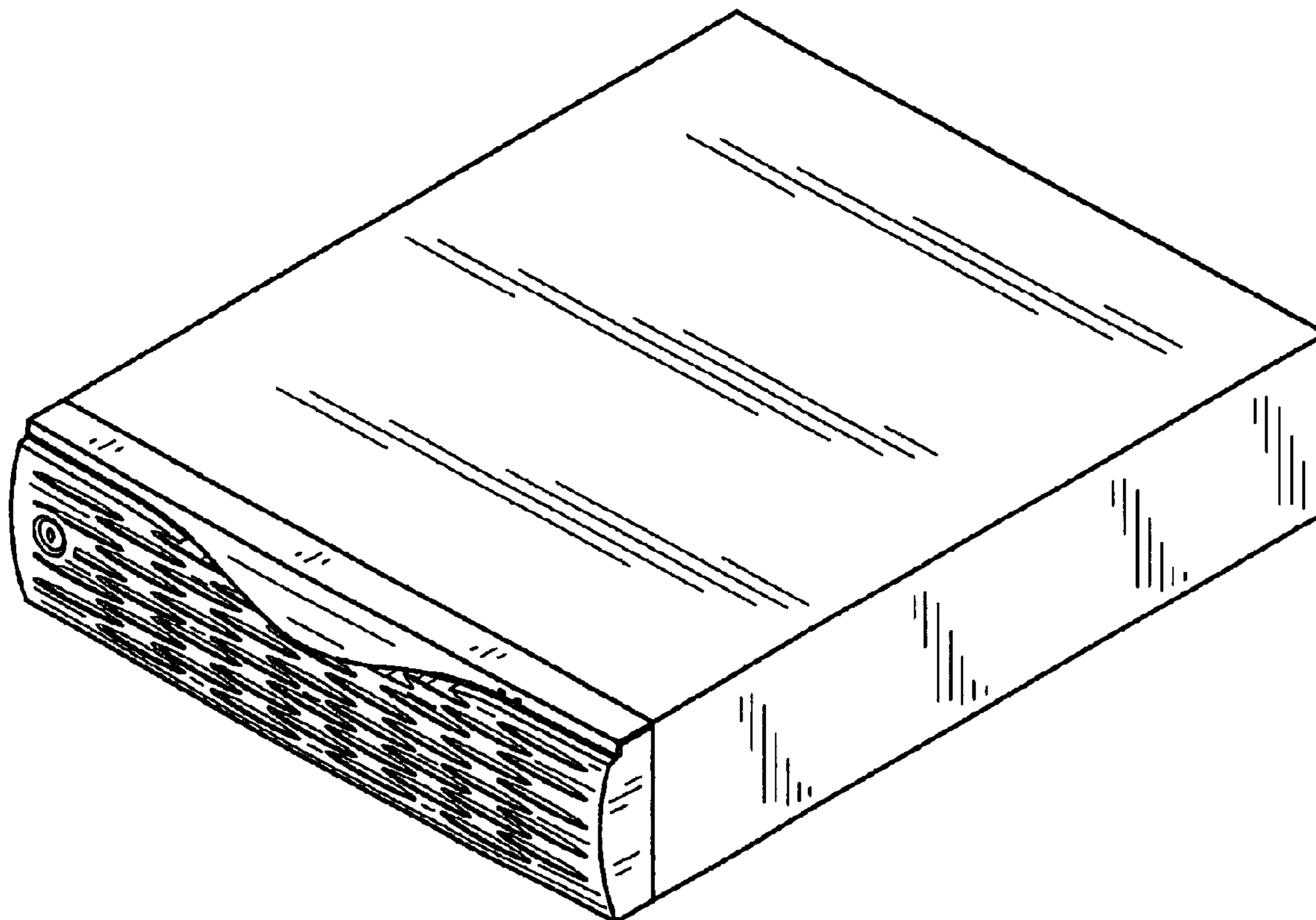


FIG. 1

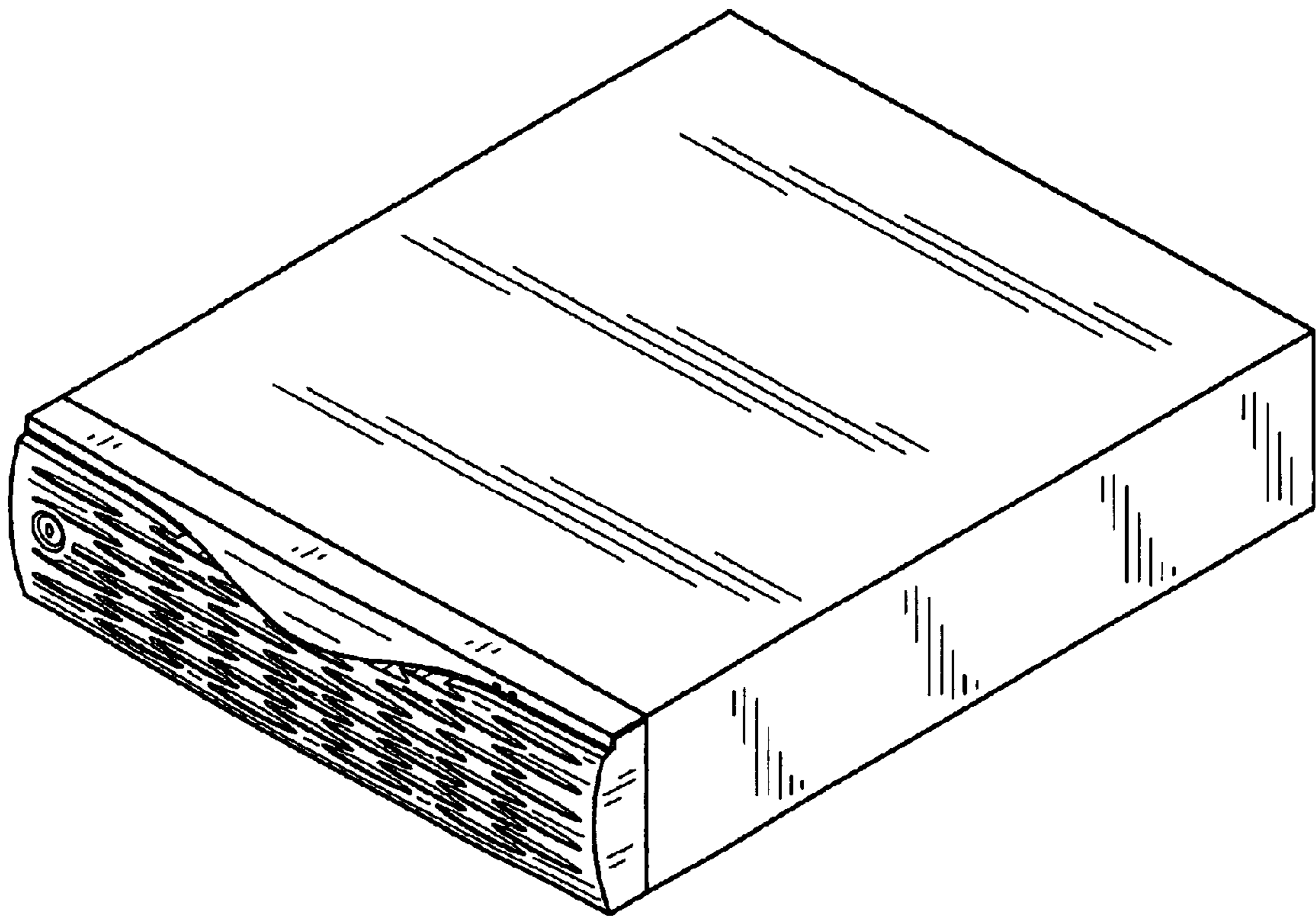


FIG. 2

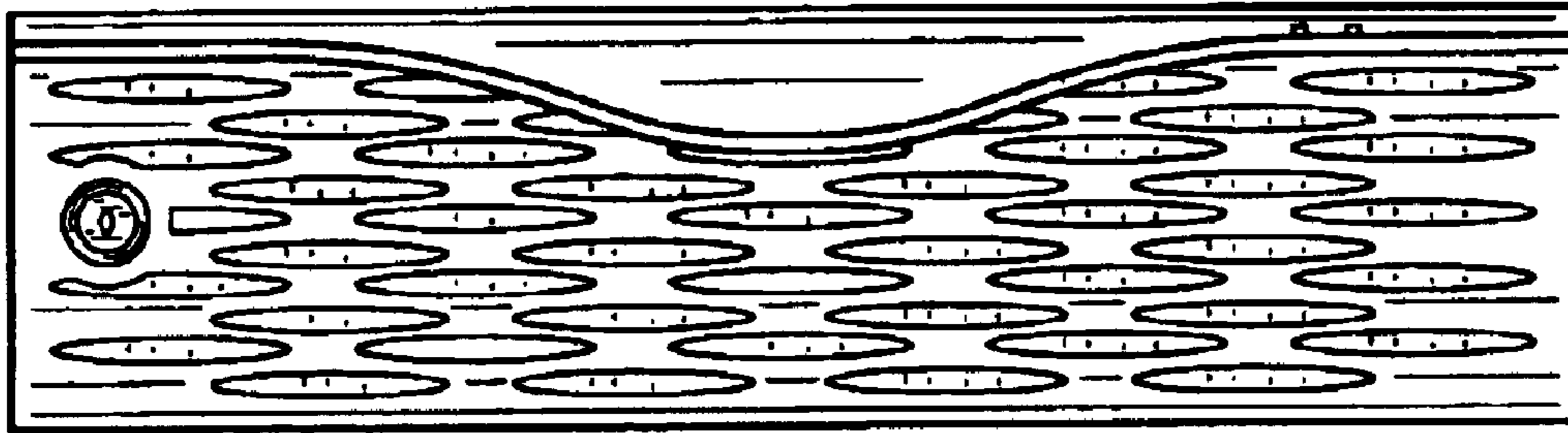


FIG. 3

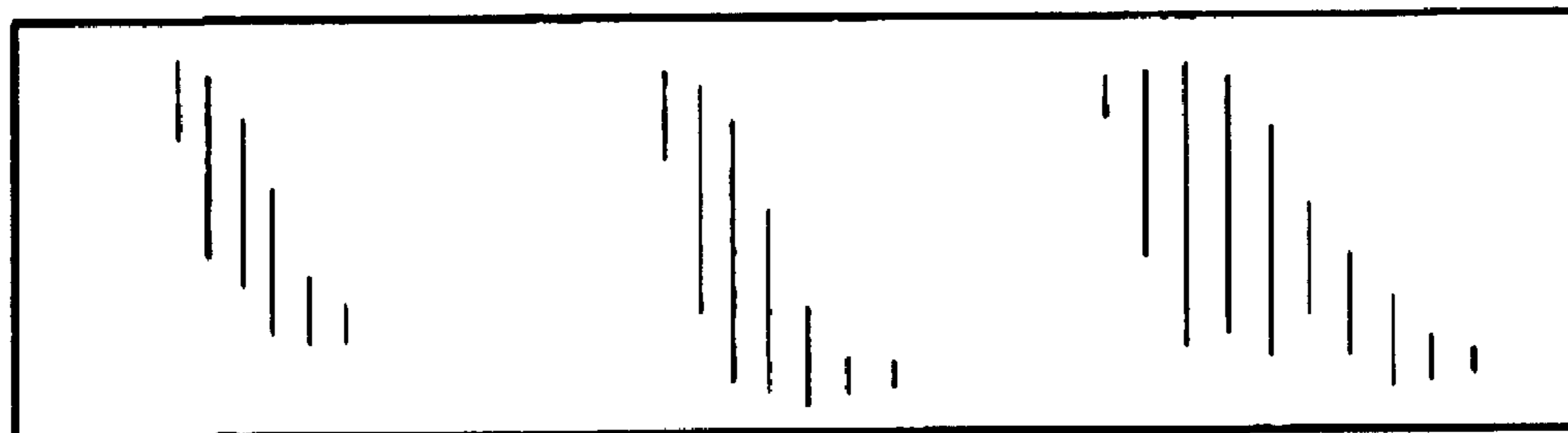


FIG. 4

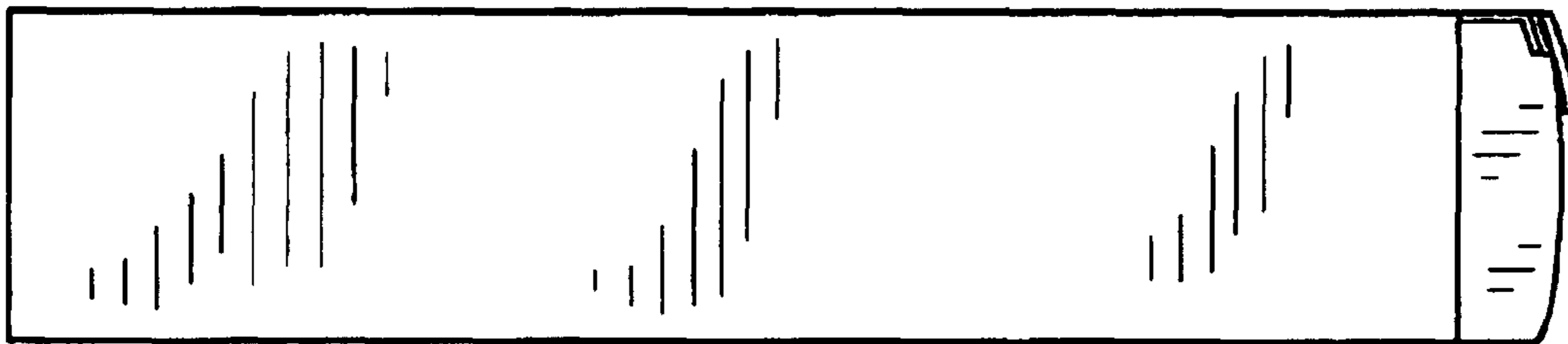


FIG. 5

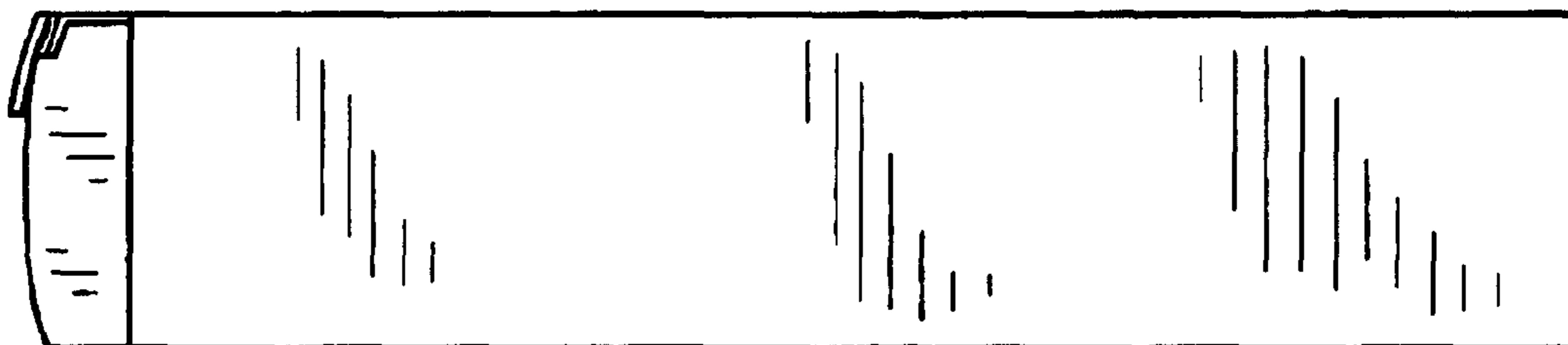


FIG. 6

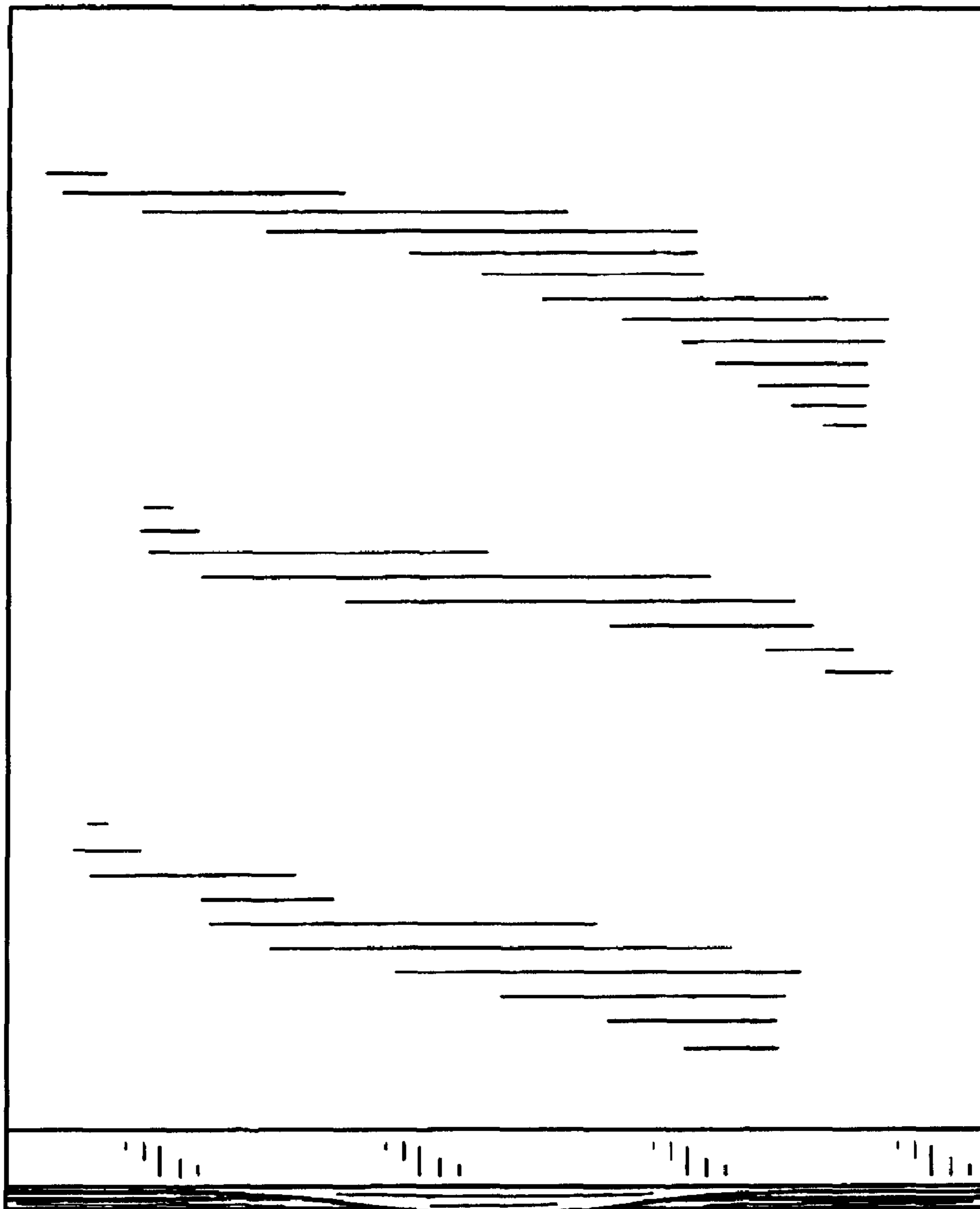


FIG. 7

