US00D495699S1

(12) United States Design Patent

Oura et al.

(10) Patent No.: US D495,699 S
(45) Date of Patent: ** Sep. 7, 2004

(54) **MEMORY CONTROL EQUIPMENT FOR COMPUTERS**

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(73) Assignee: **NEC Corporation**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/178,882**

(22) Filed: **Apr. 2, 2003**

(30) **Foreign Application Priority Data**

Oct. 3, 2002 (JP) 2002-027184

(51) **LOC (7) Cl.** **14-02**
(52) **U.S. Cl.** **D14/356**
(58) **Field of Search** D14/356, 358; 361/684, 685

(56) **References Cited**

U.S. PATENT DOCUMENTS

D333,131 S * 2/1993 Yamamoto D14/357
D355,195 S * 2/1995 Burke D14/217
5,684,671 A * 11/1997 Hobbs et al. 361/683
D421,255 S * 2/2000 Hisatsune et al. D14/125
D422,572 S * 4/2000 Oura et al. D6/632
6,188,571 B1 * 2/2001 Roganti et al. 361/685

* cited by examiner

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(57) **CLAIM**

The ornamental design for a memory control equipment for computers, as shown.

DESCRIPTION

FIG. **1** is a perspective view of the top, front and right side of a memory control equipment for computers showing our new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.

1 Claim, 3 Drawing Sheets

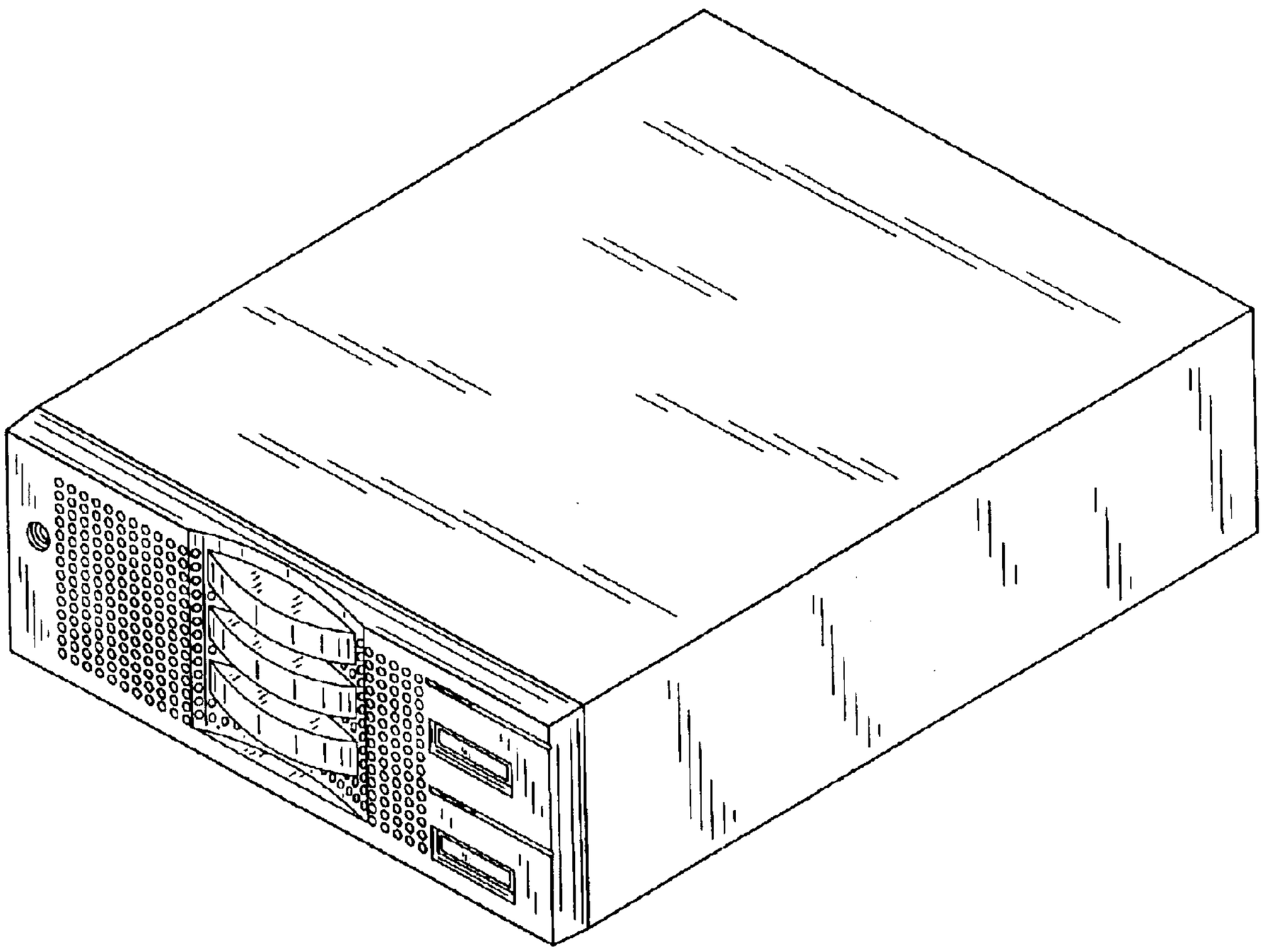

FIG. 1

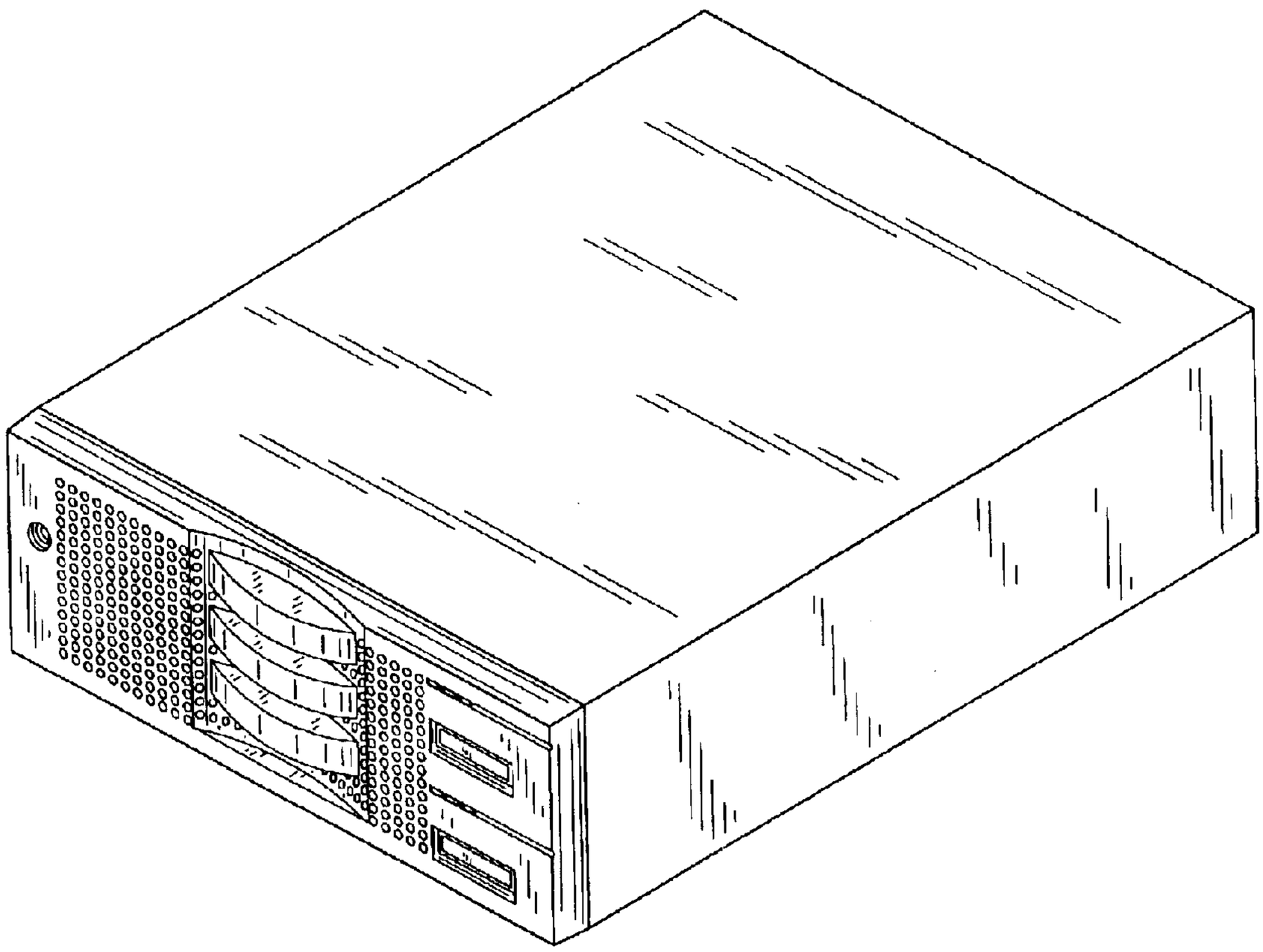

FIG. 2

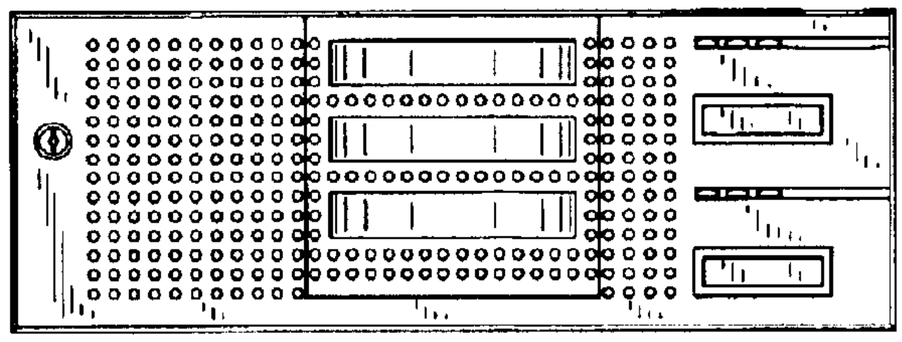

FIG. 3

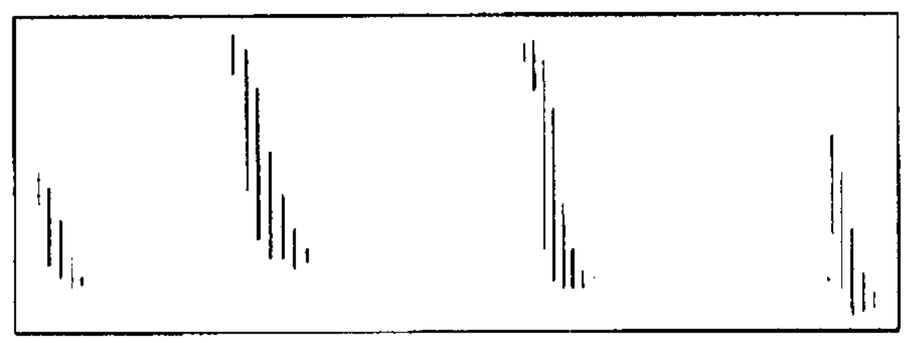

FIG. 4

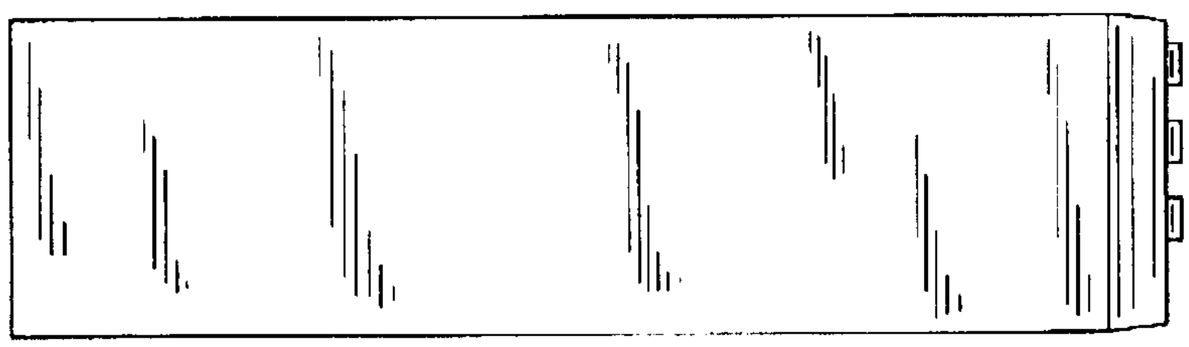

FIG. 5

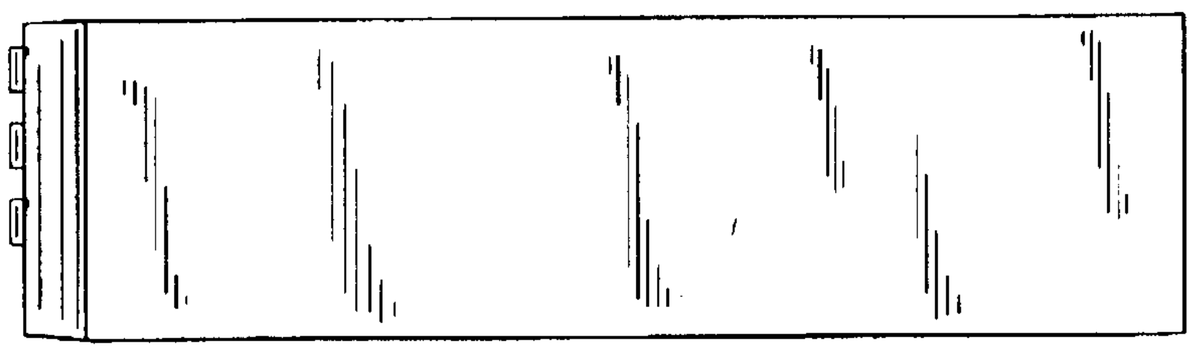

FIG. 6

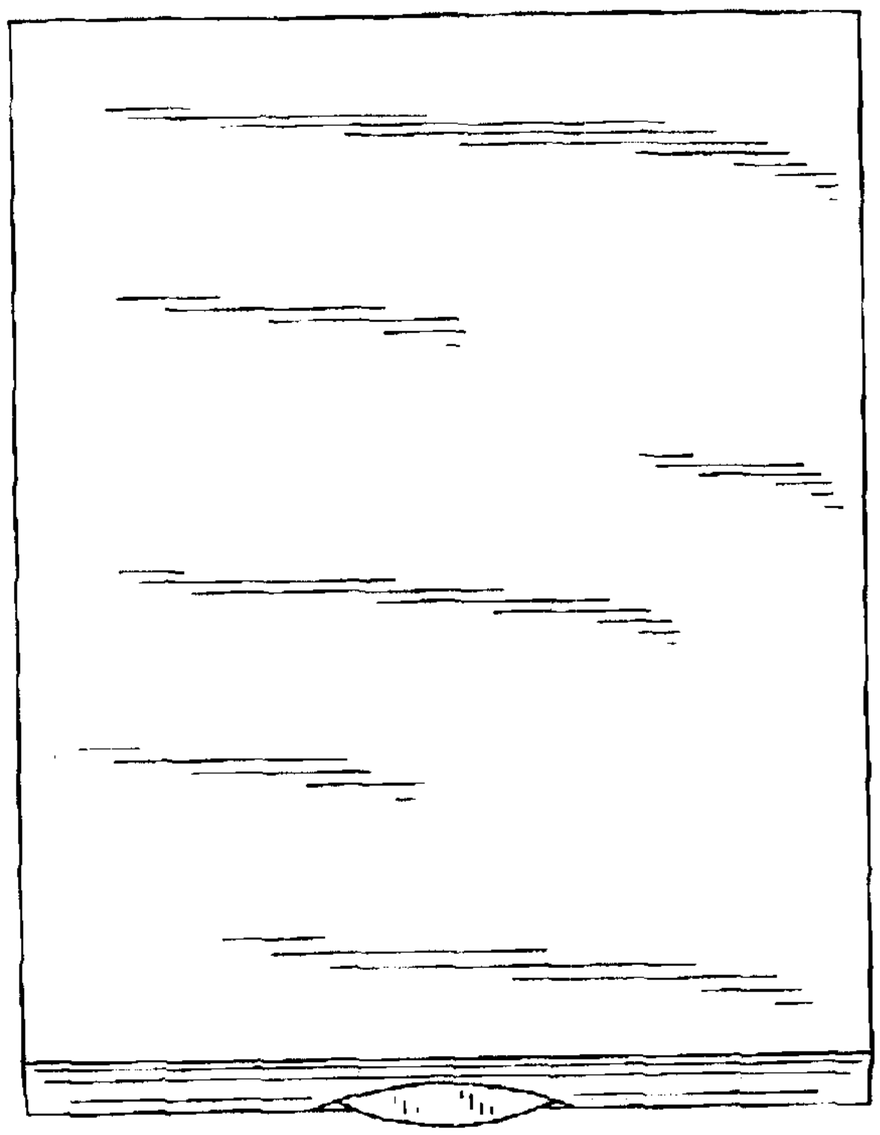

FIG. 7