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(12) **United States Design Patent**
Doba

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(54) **EXHAUST RING FOR MANUFACTURING SEMICONDUCTORS**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)
(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**
Dec. 12, 2002 (JP) 2002-034493

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; D8/399;
D15/144; 118/666, 715, 733; 219/444.1;
414/147, 217, 247, 935-941; 438/482, 706,
716, 758; 451/285

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(57) **CLAIM**

I claim the ornamental design for exhaust ring for manufacturing semiconductors, as shown and described.

DESCRIPTION

FIG. 1 is a front/top perspective view of an exhaust ring for manufacturing semiconductors showing my new design; FIG. 2 is a top plan view thereof, the bottom plan view being a mirror image and, therefore, not shown; FIG. 3 is a front elevational view thereof, the left-side elevational view being a mirror image and, therefore, not shown; FIG. 4 is a right-side elevational view thereof; FIG. 5 is a rear elevational view thereof; FIG. 6 is a reference front elevational view thereof; FIG. 7 is a right-side cross-sectional view taken along line 7—7 in FIG. 6; and, FIG. 8 is an enlarged, partial, cross-sectional view taken along line 8—8 in FIG. 7.

The exhaust ring for manufacturing semiconductors is used in a vacuum vessel for manufacturing semiconductors.

1 Claim, 2 Drawing Sheets

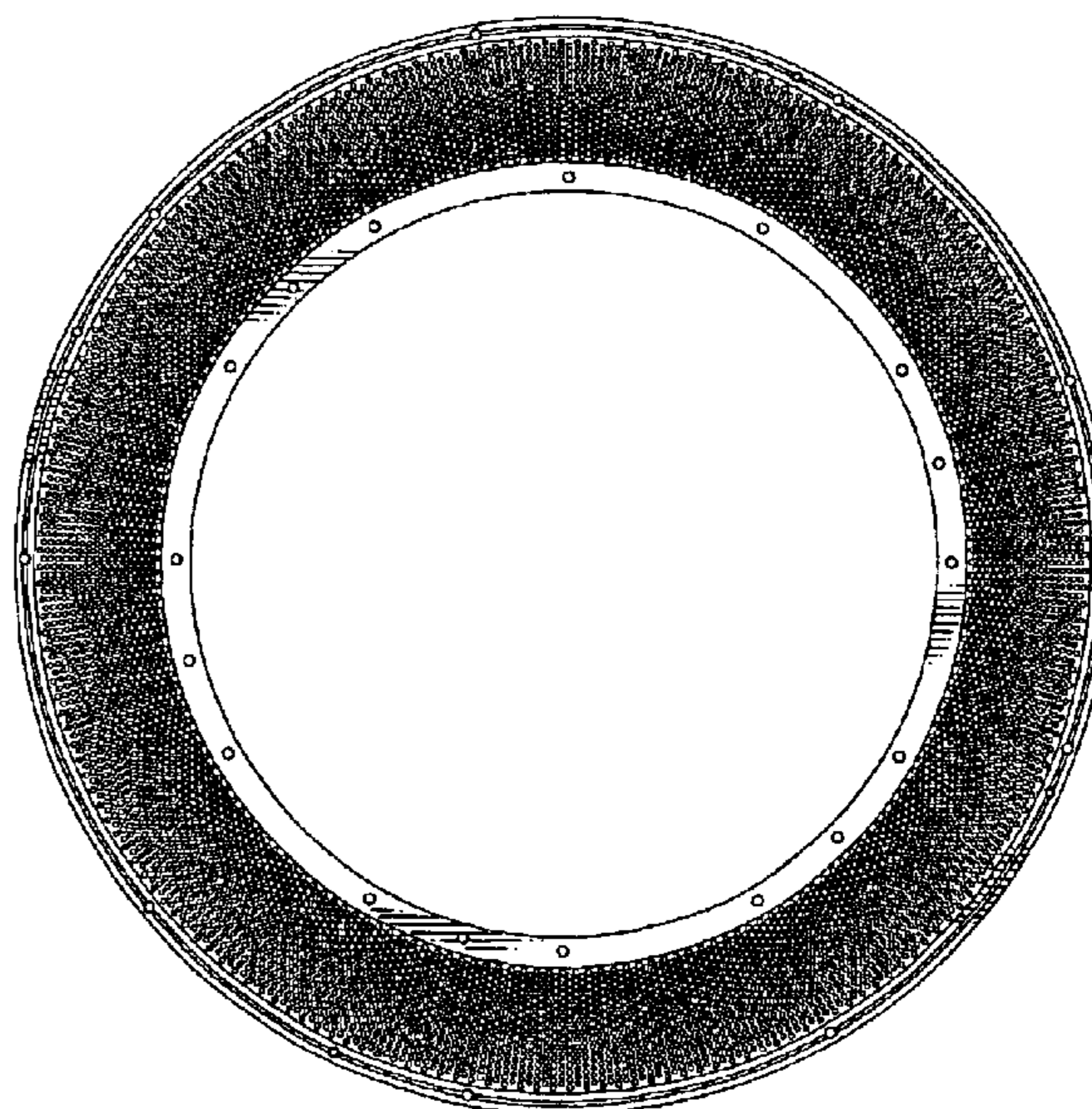
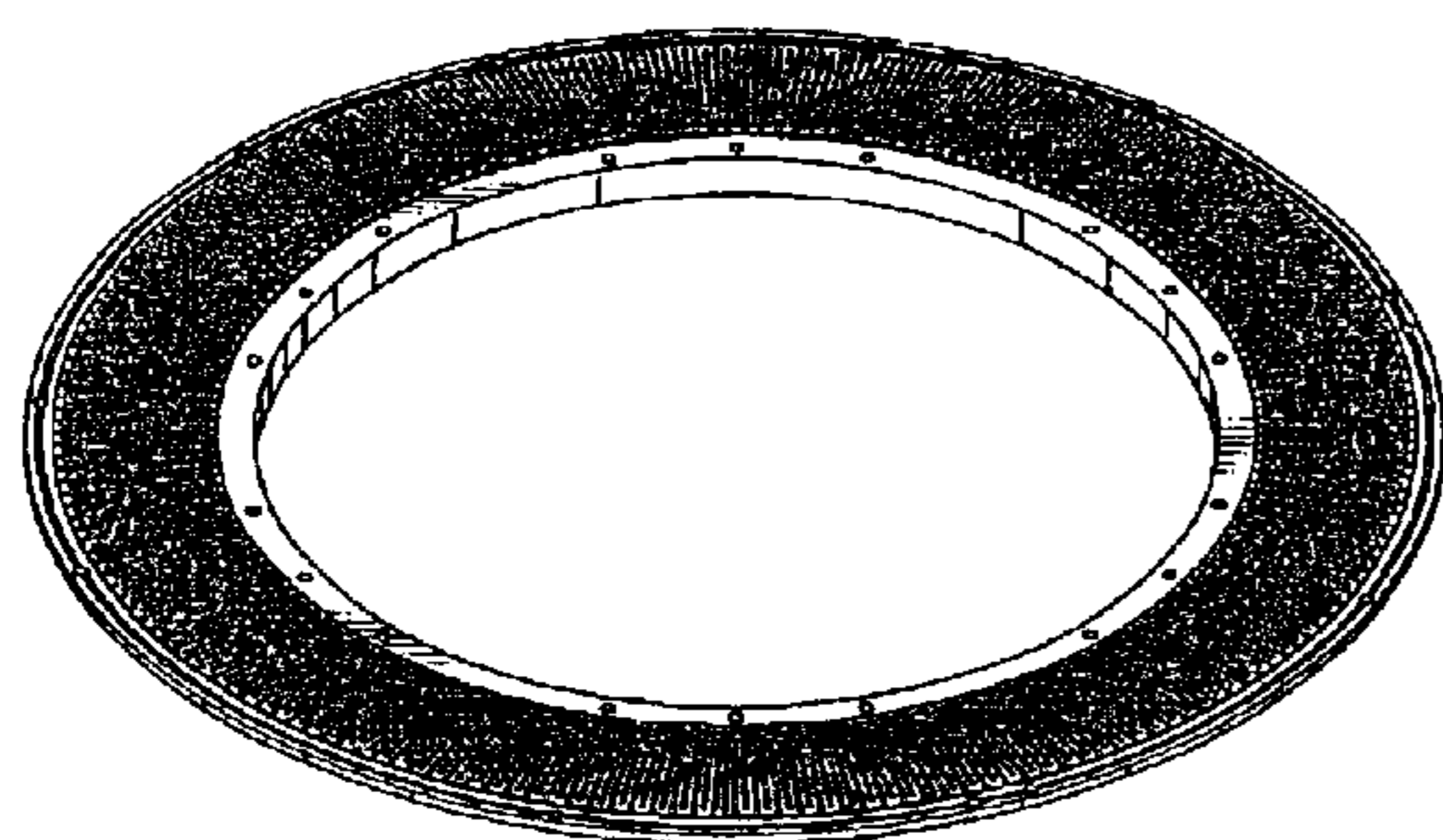


FIG. 1

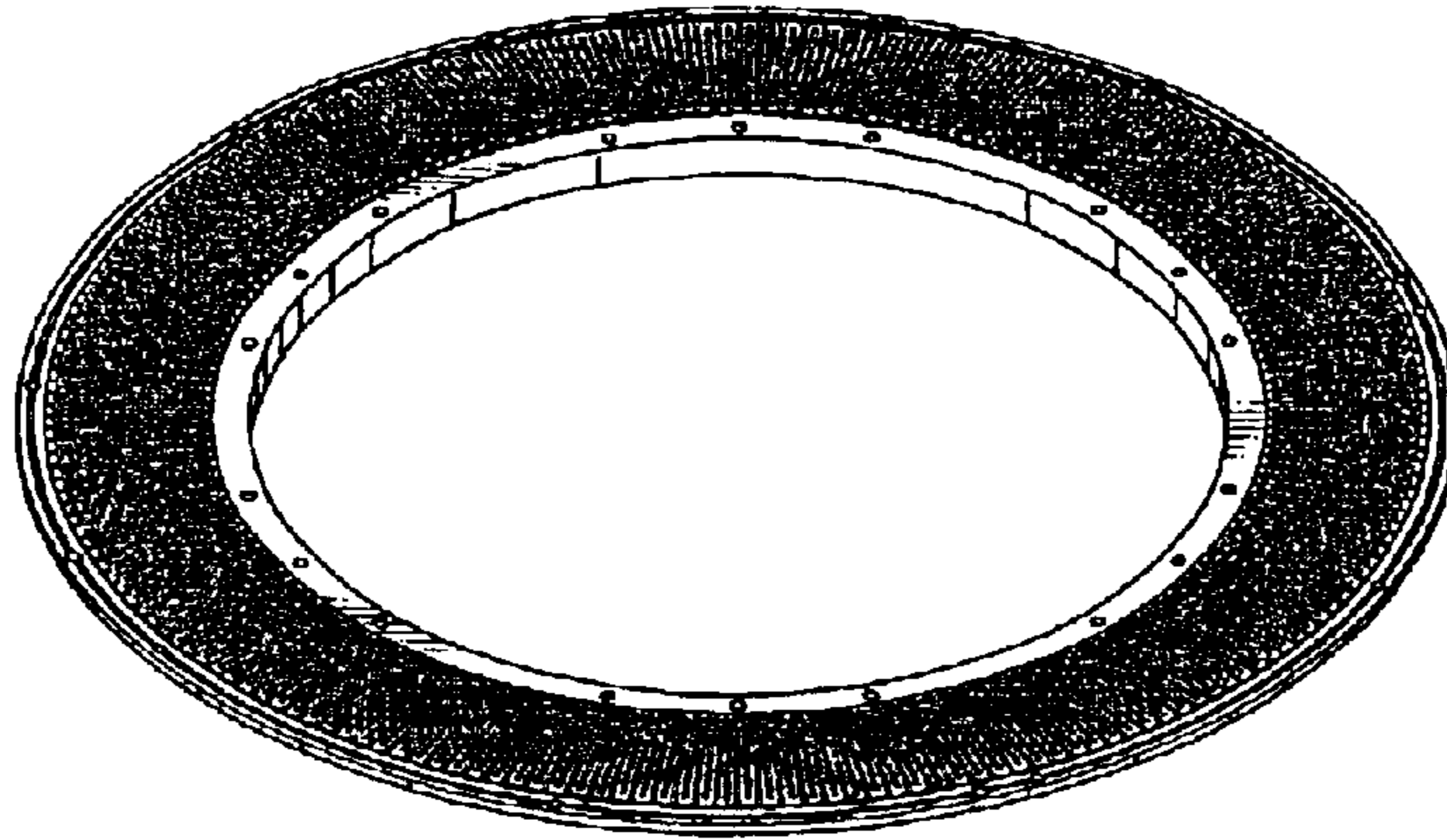


FIG. 2

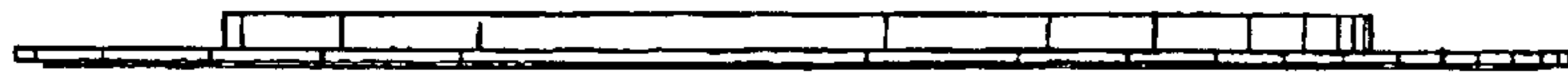


FIG. 3

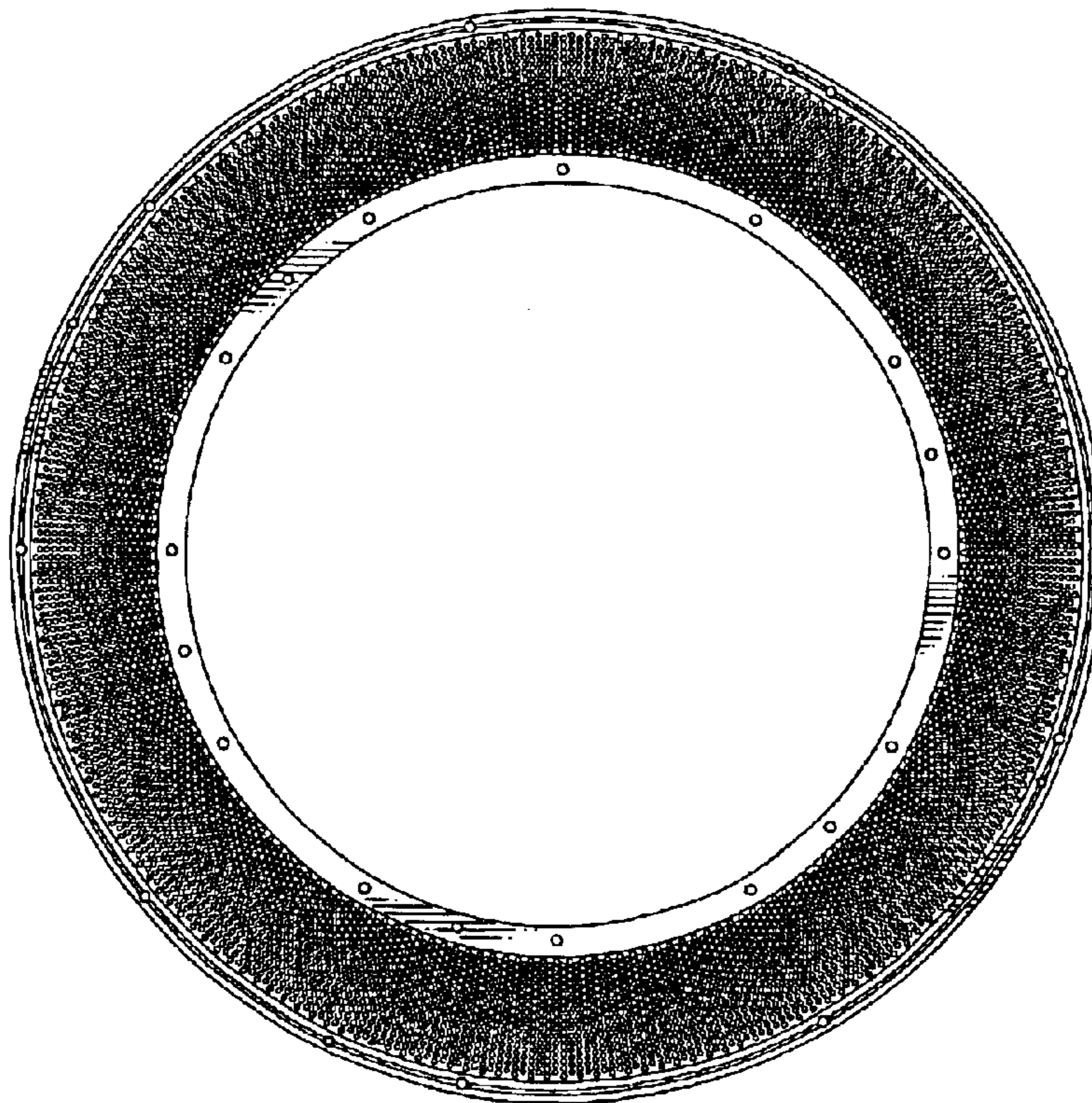


FIG. 4



FIG. 5

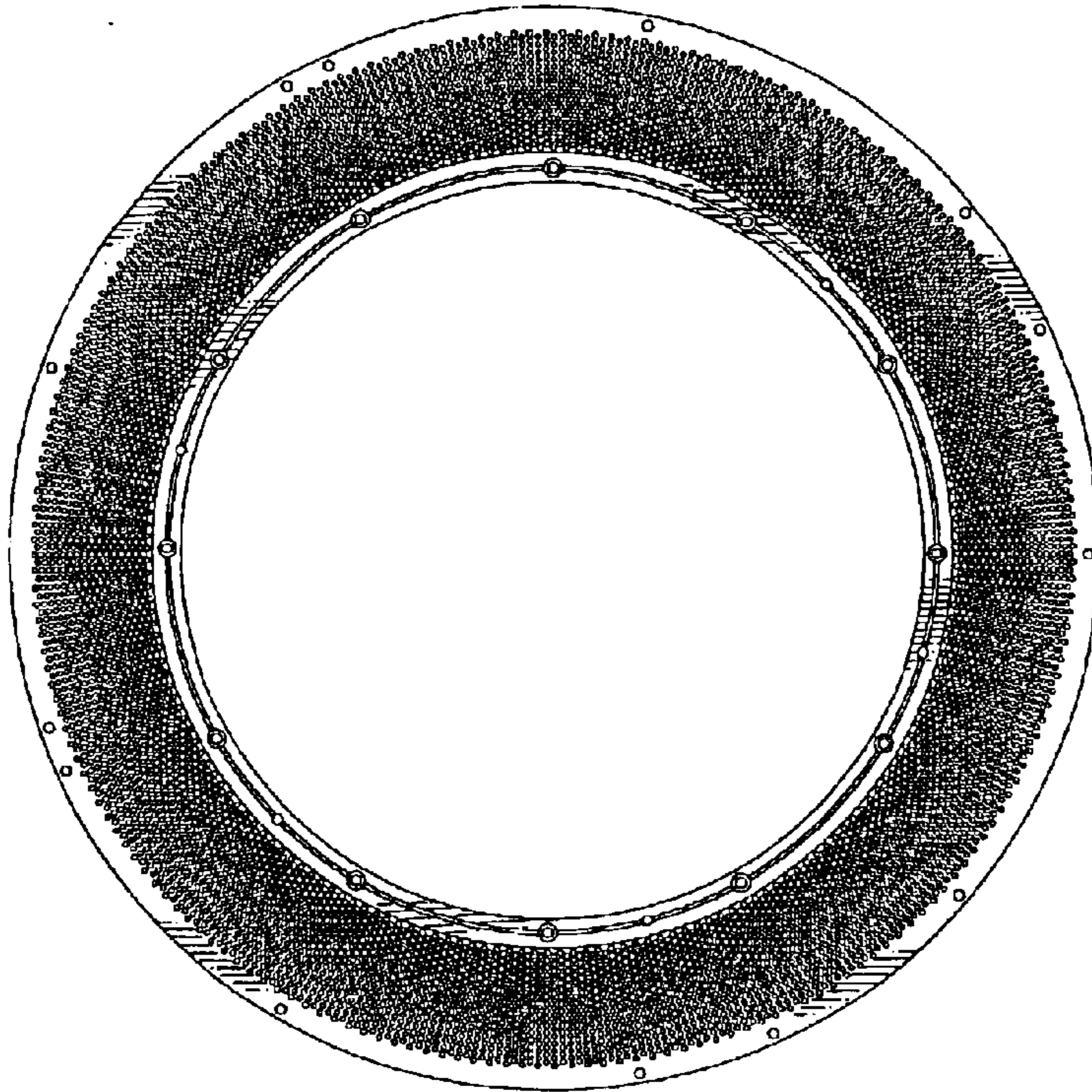


FIG. 8

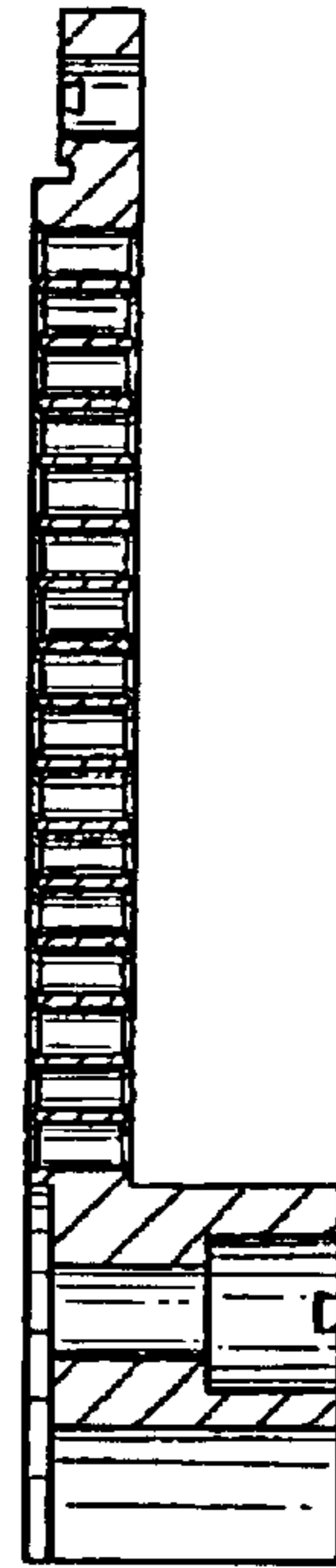


FIG. 6

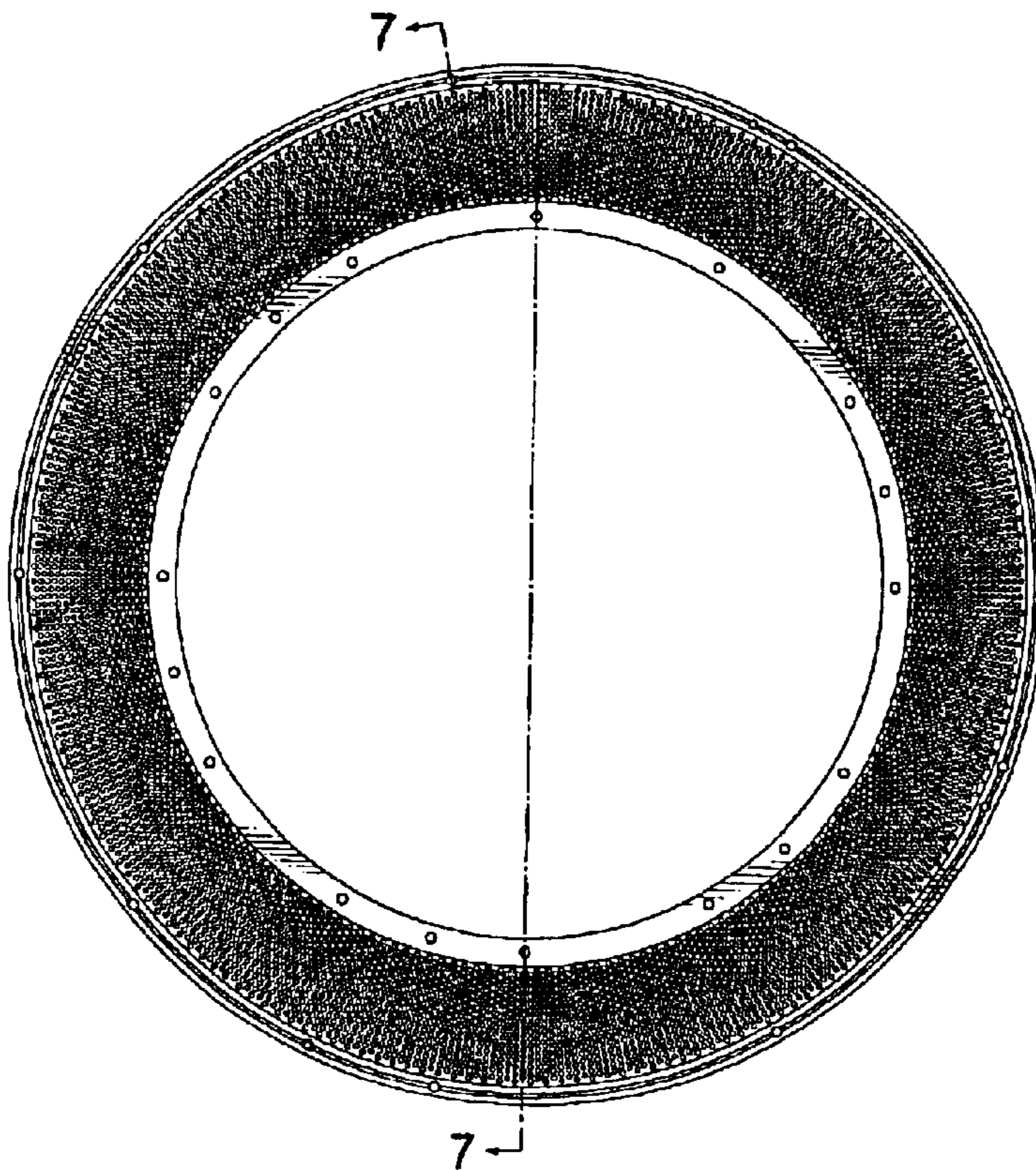


FIG. 7

