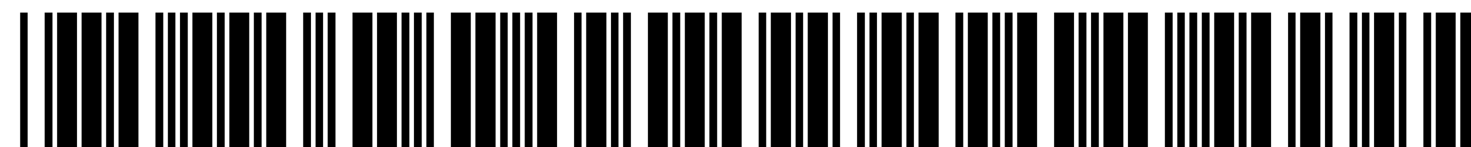

US00D491963S1

(12) **United States Design Patent** (10) **Patent No.: US D491,963 S**
Doba (45) **Date of Patent: ** Jun. 22, 2004**

(54) **INNER WALL SHIELD FOR A PROCESS CHAMBER FOR MANUFACTURING SEMICONDUCTORS**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/182,142**

(22) Filed: **May 20, 2003**

(30) **Foreign Application Priority Data**

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Nov. 20, 2002 (JP) 2002-032005

(51) **LOC (7) Cl.** **15-09**
(52) **U.S. Cl.** **D15/144**
(58) **Field of Search** D15/144; 118/504; 204/298.07, 298.09, 298.11; 427/255.28, 248.1, 250

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,432,203 B1 * 8/2002 Black et al. 118/504
6,630,201 B2 * 10/2003 Chiang et al. 427/255.28

* cited by examiner

Primary Examiner—Antoine D. Davis
(74) *Attorney, Agent, or Firm*—Ladas & Parry

(57) **CLAIM**

I claim the ornamental design for inner wall shield for a process chamber for manufacturing semiconductors, as shown and described.

DESCRIPTION

FIG. **1** atop/left-side/rear perspective view of a first embodiment of an inner wall shield for a process chamber for manufacturing semiconductors;
FIG. **2** a front elevational view thereof;
FIG. **3** a rear elevational view thereof;
FIG. **4** a right side elevational view thereof;
FIG. **5** a left side elevational view thereof;
FIG. **6** a top plan view thereof;
FIG. **7** a bottom plan view thereof;
FIG. **8** a cross-sectional view thereof taken along line **8—8** in FIG. **2**;
FIG. **9** a cross-sectional view there taken along line **9—9** in FIG. **4**
FIG. **10** an enlarged view of a right-end portion of FIG. **9**.
FIG. **11** a top/left-side/rear perspective view of a second embodiment of an inner wall shield for a process chamber for manufacturing semiconductors;
FIG. **12** a front elevational vie thereof;
FIG. **13** a rear elevational view thereof;
FIG. **14** a right side elevational view thereof;
FIG. **15** a left side elevational view thereof;
FIG. **16** a top plan view thereof;
FIG. **17** a bottom plan view thereof;
FIG. **18** a cross-sectional view taken alone line **8—8** in FIG. **2**;
FIG. **19** a cross-sectional view taken along **9—9** in FIG. **4**; and,
FIG. **20** an enlarged view taken along line **10—10** in FIG. **9**.

The inner wall shield for a process chamber for manufacturing semiconductors is typically attached along the inner wall of the process chamber of an etching device. When sufficient high frequency power is connected to upper and lower electrodes of the process chamber, plasma is generated between the electrodes and the inner wall shield prevents the plasma from damaging the inner wall of the process chamber. One or more of the five small circles in one or more of the cross patterns shown in FIGS. **1, 3, 3** and **4** (two patterns), for example, are through holes that are disclaimed in other embodiments (not shown). The outer diameters of the embodiments are preferably about 670 mm, the height of the first embodiment is preferably about 110 mm and the height of the second embodiment is preferably about 150 mm.

1 Claim, 6 Drawing Sheets

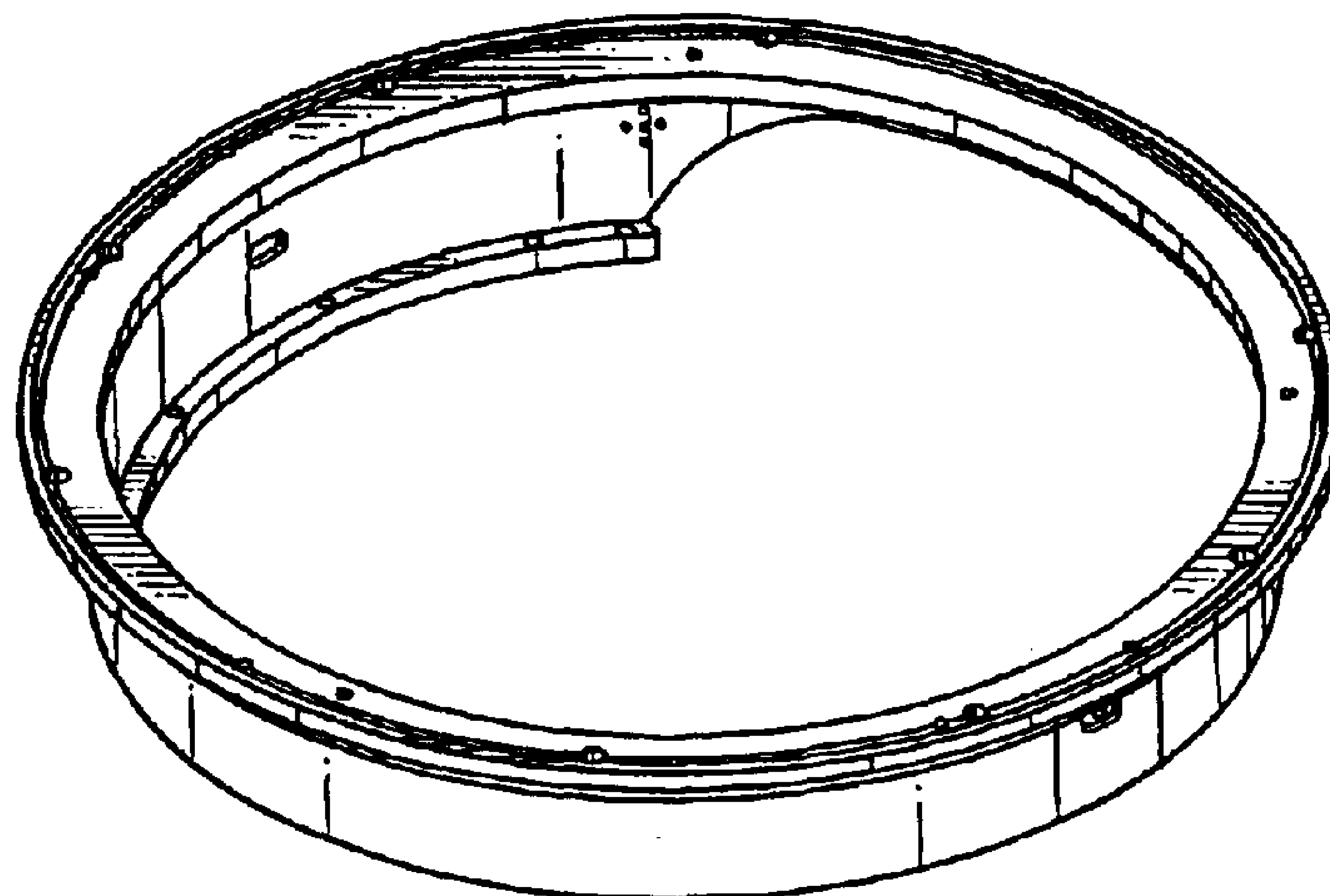


FIG. 1

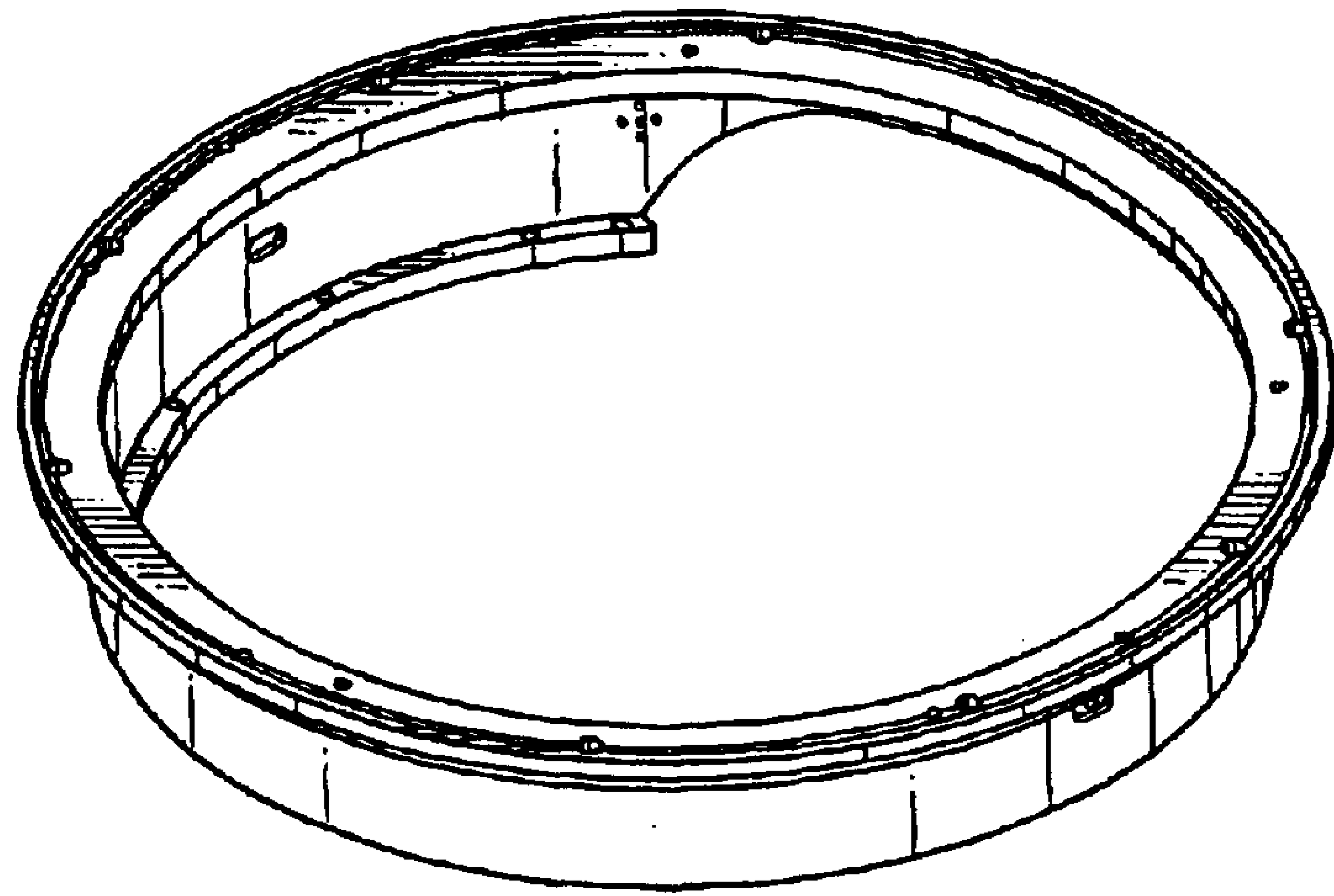


FIG. 2

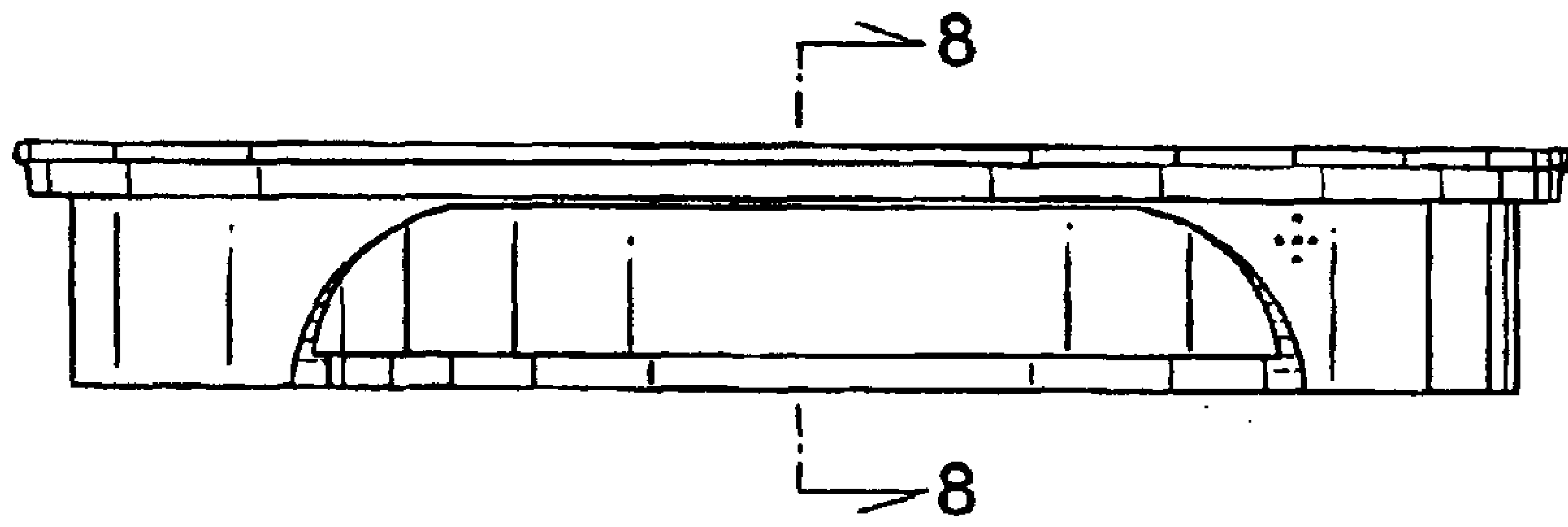


FIG. 3

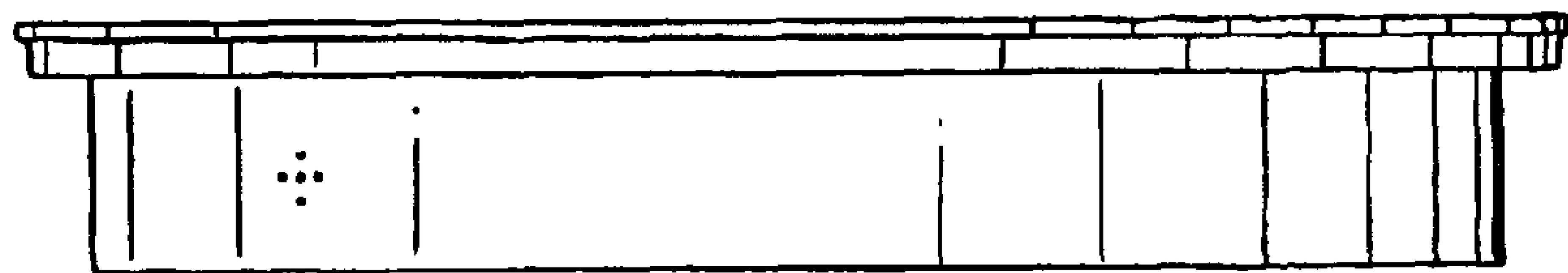


FIG. 4

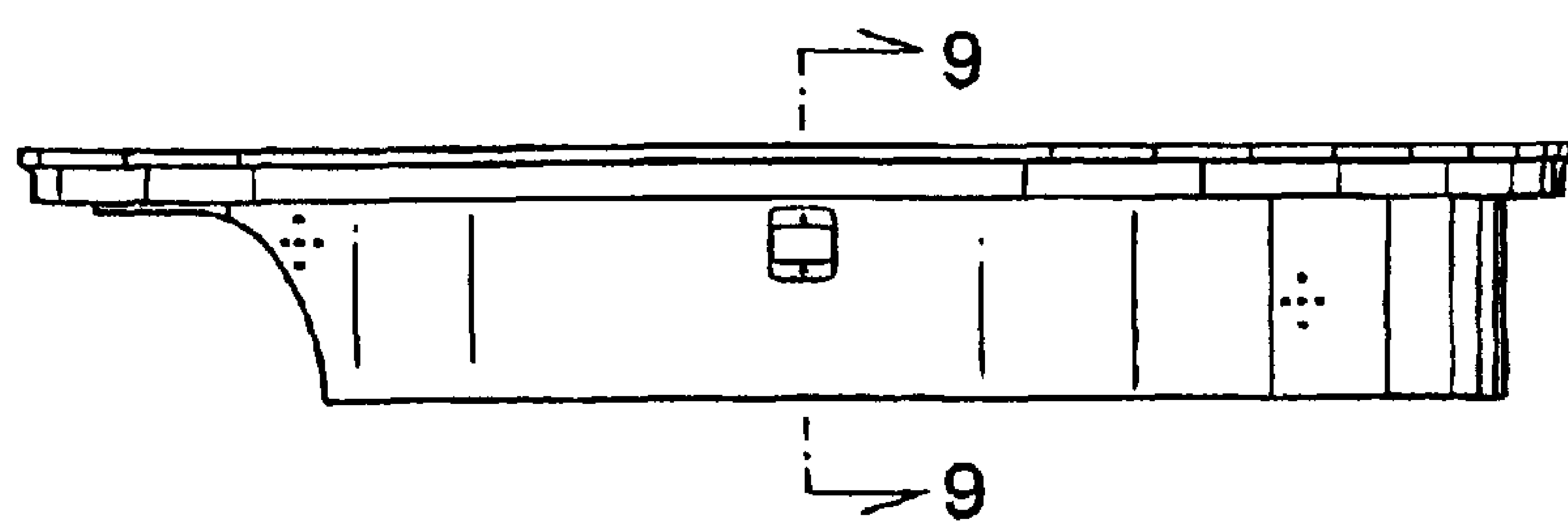


FIG. 5

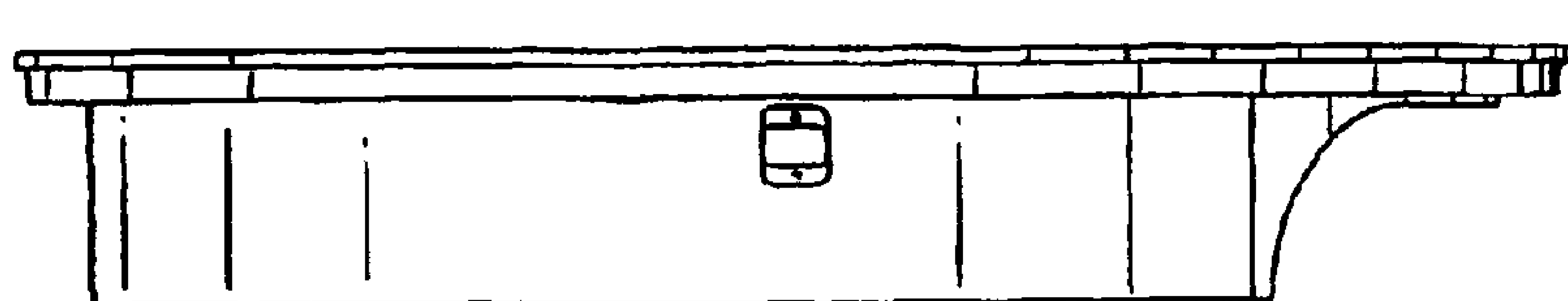


FIG. 6

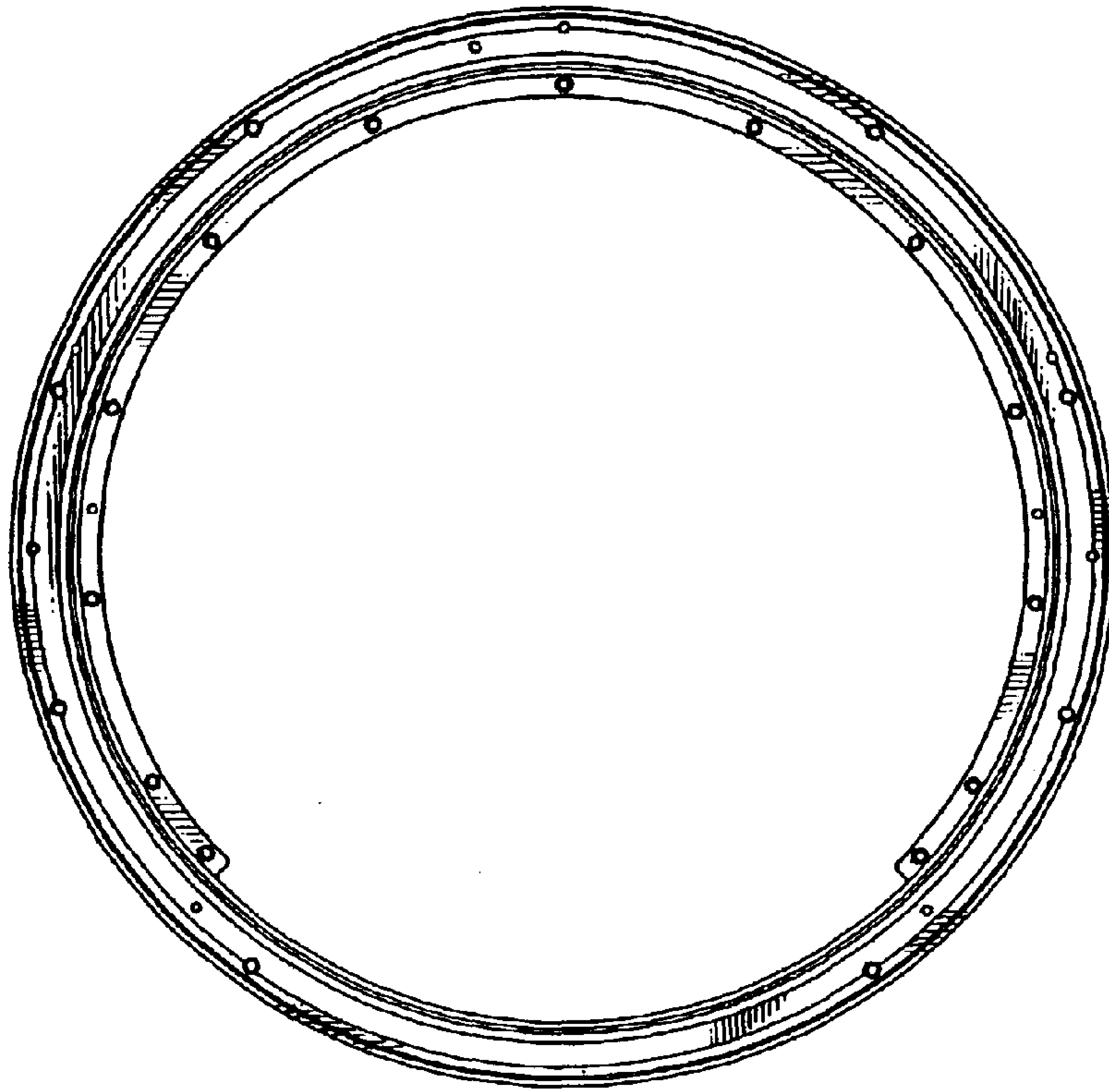


FIG. 7

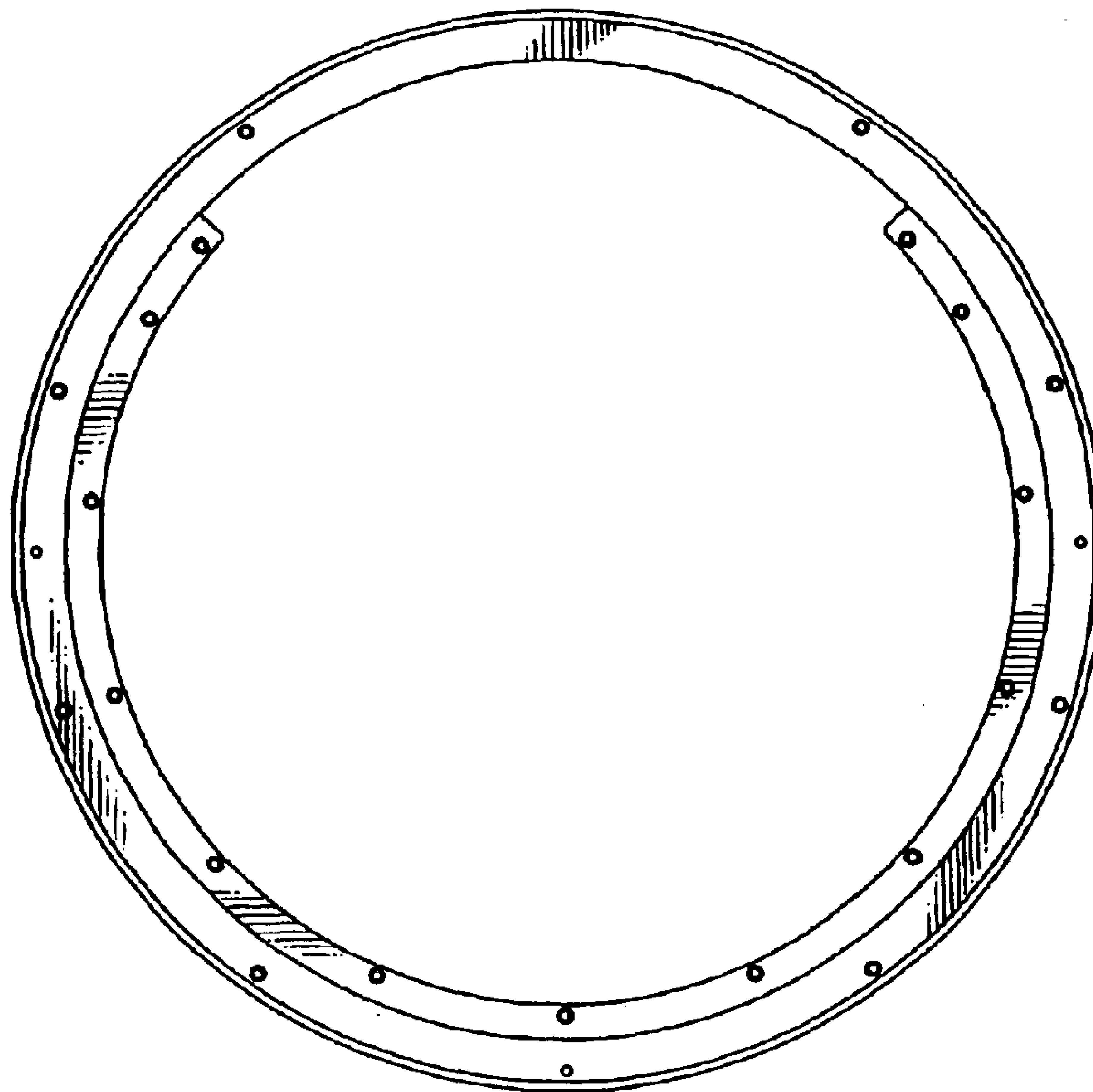


FIG. 8

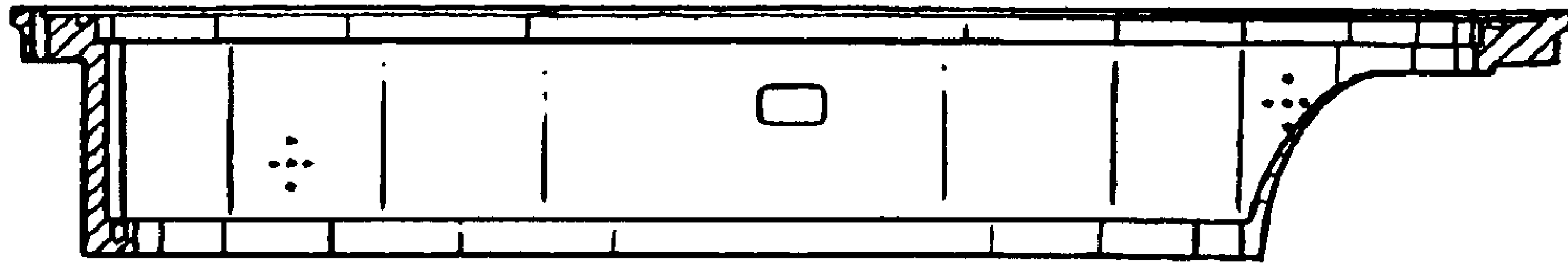


FIG. 9

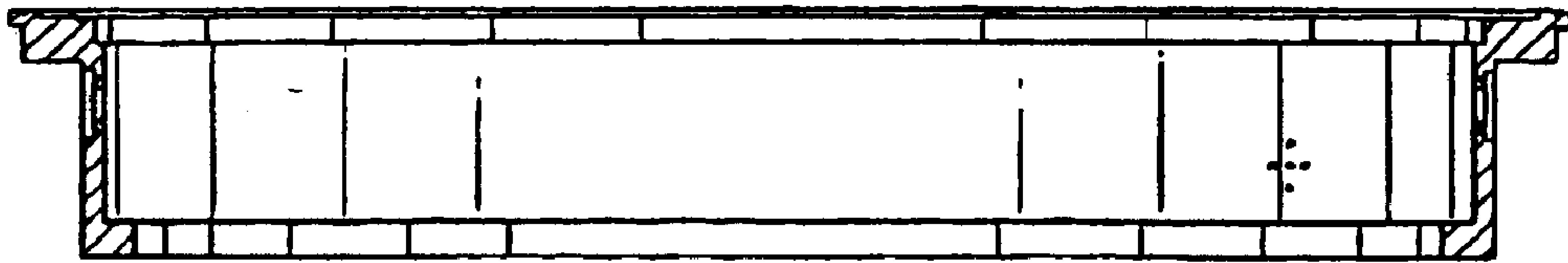
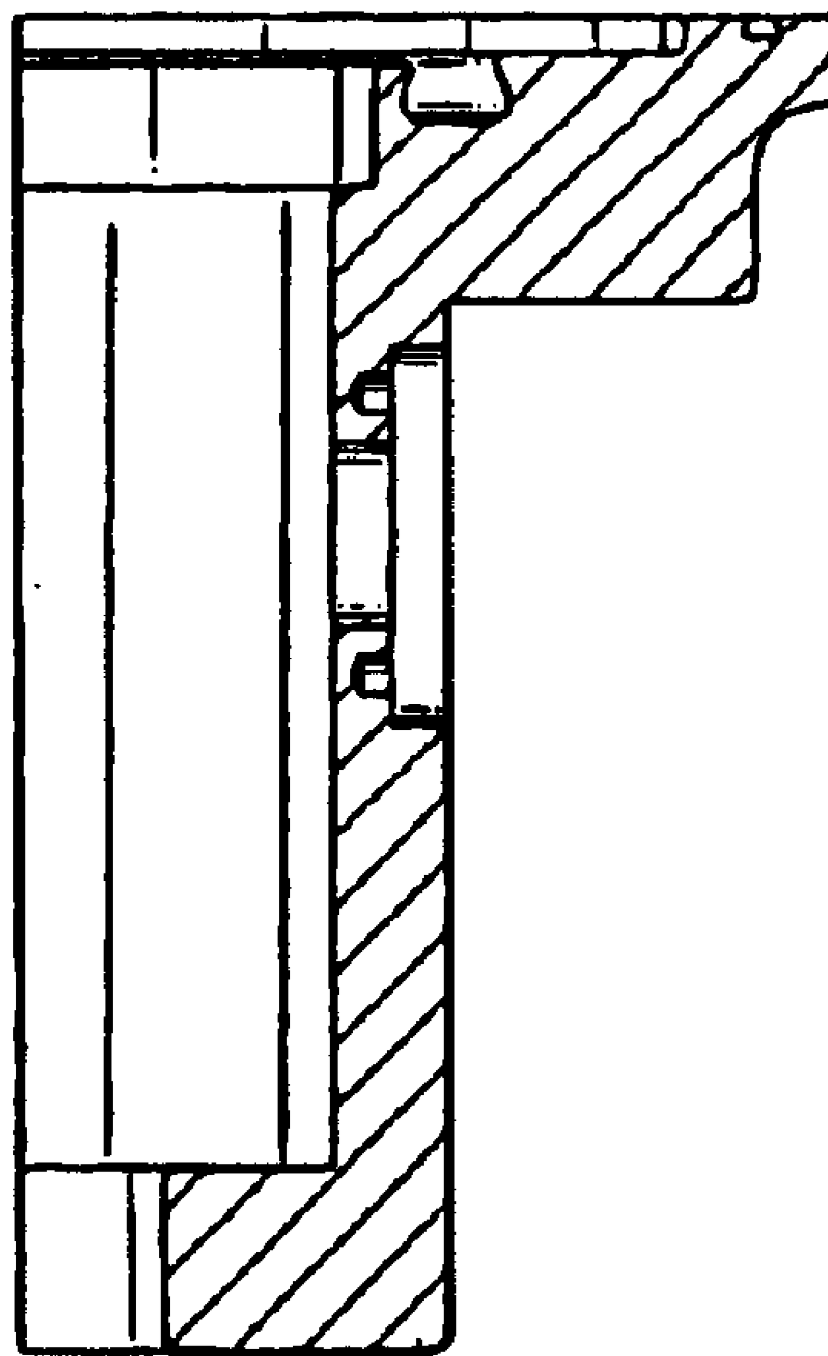


FIG. 10



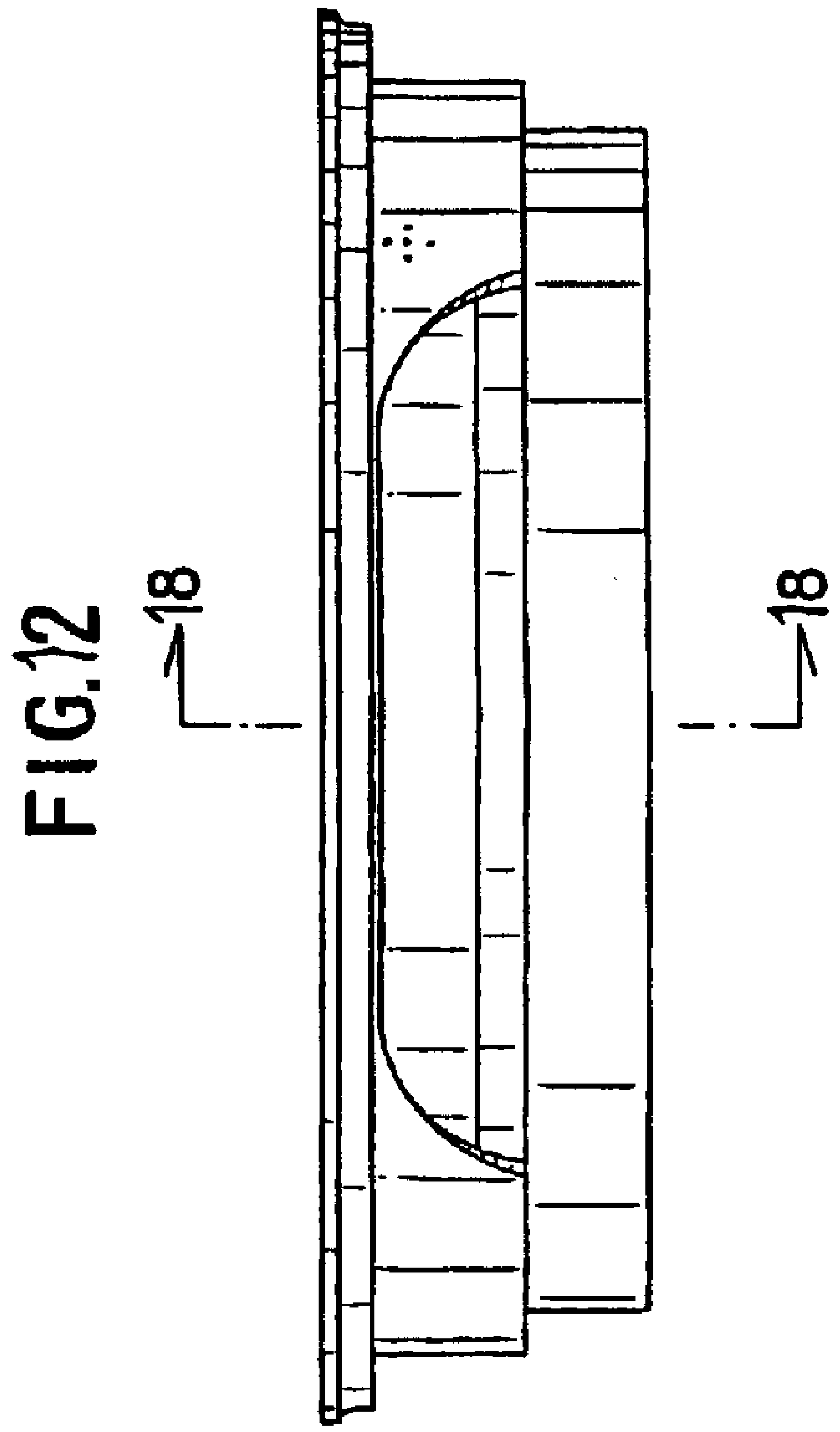


FIG.12

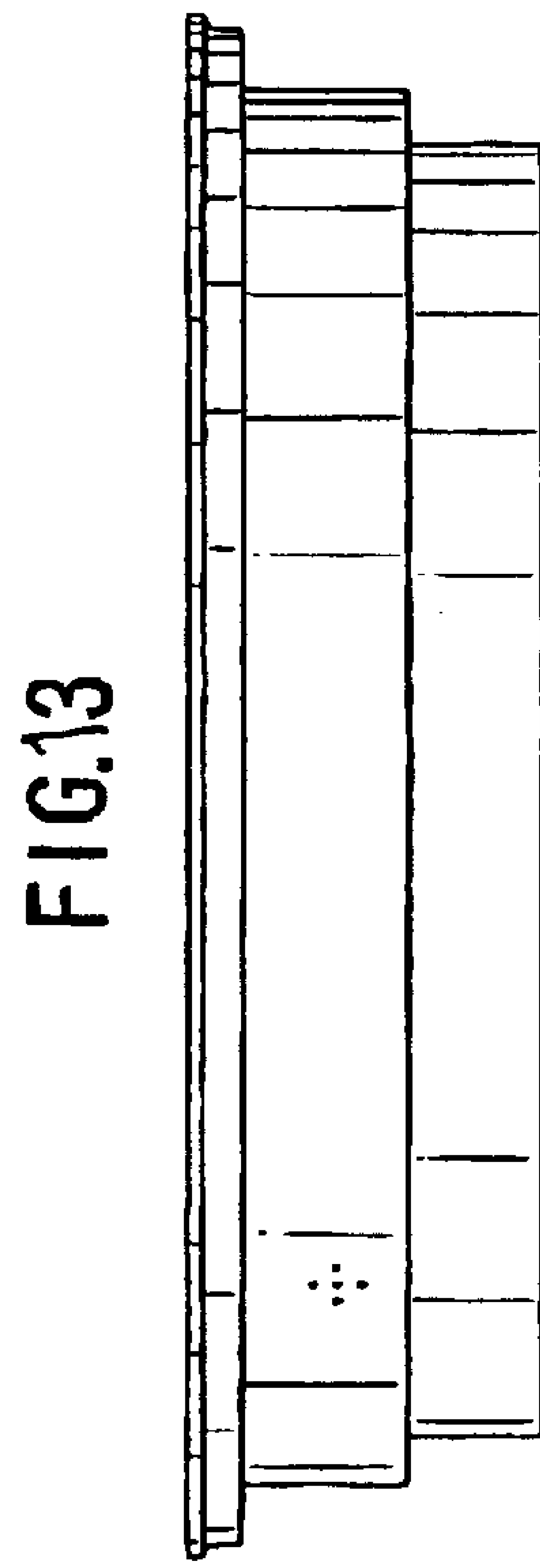


FIG.13

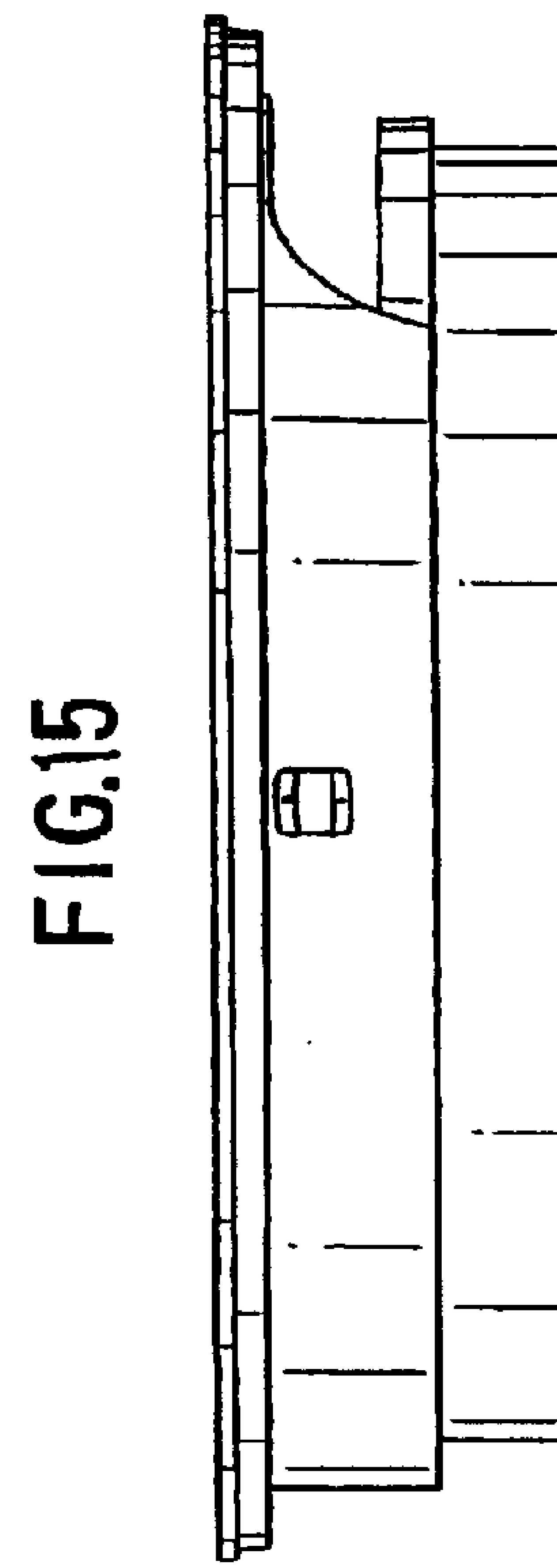


FIG.15

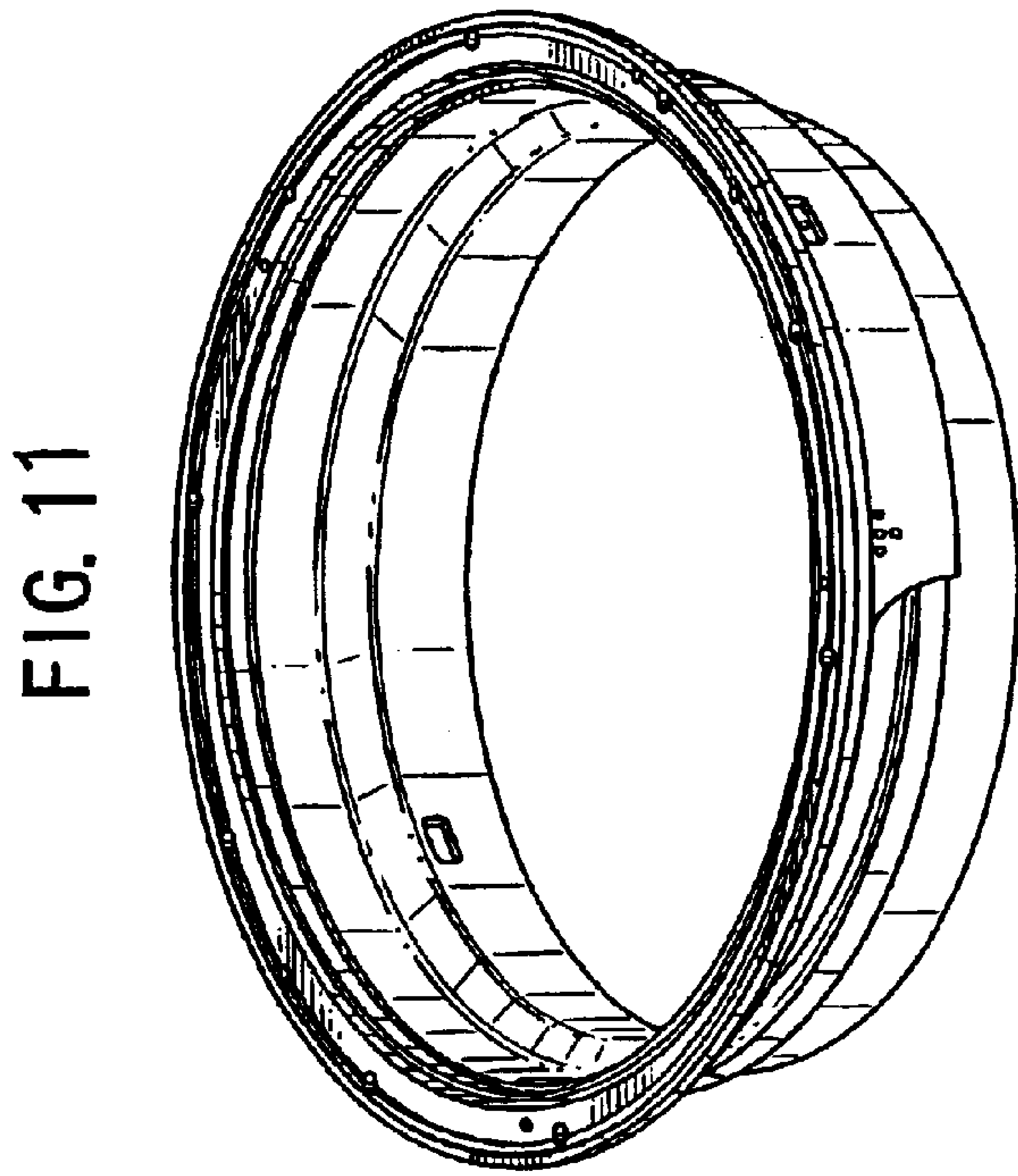


FIG. 11

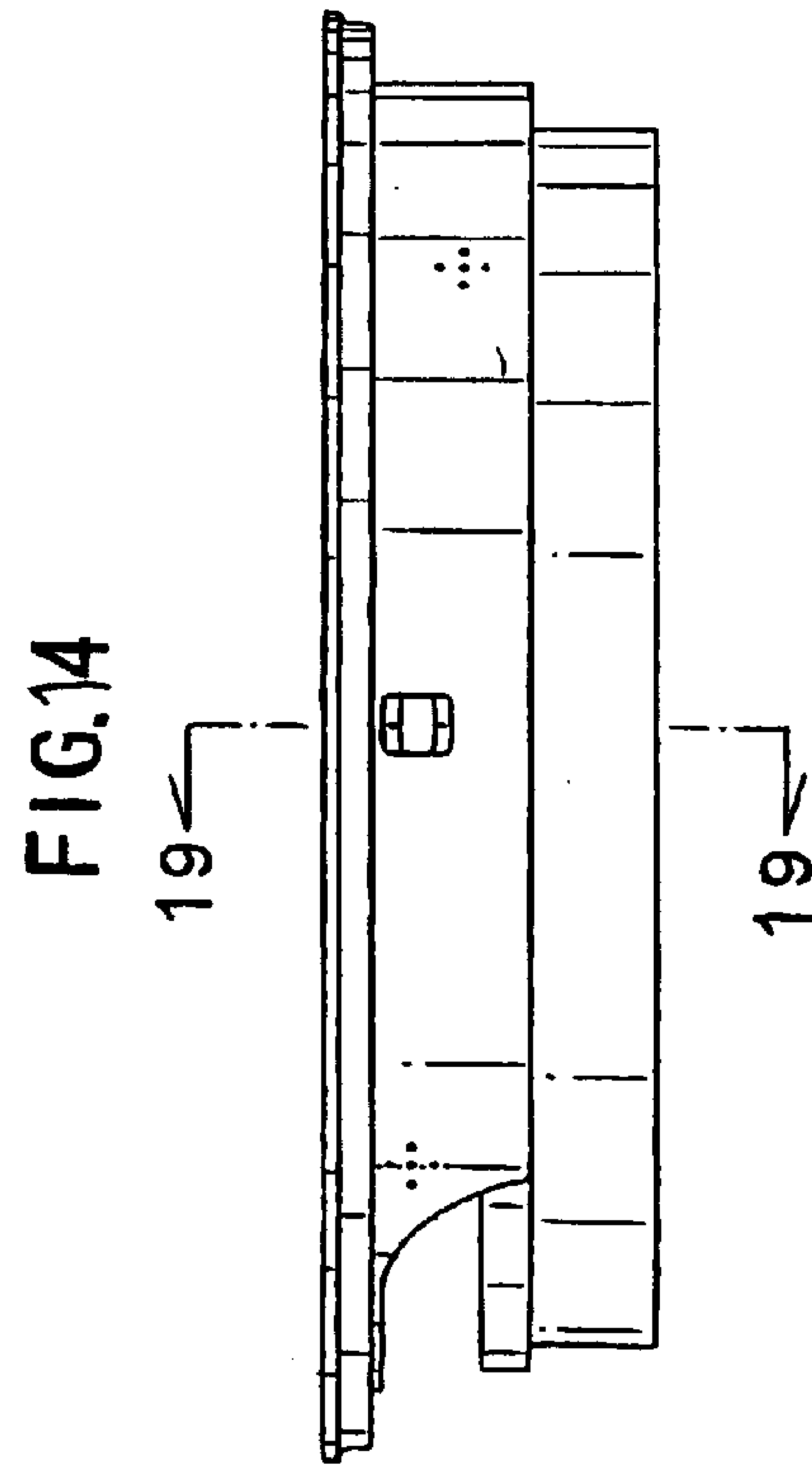


FIG.14

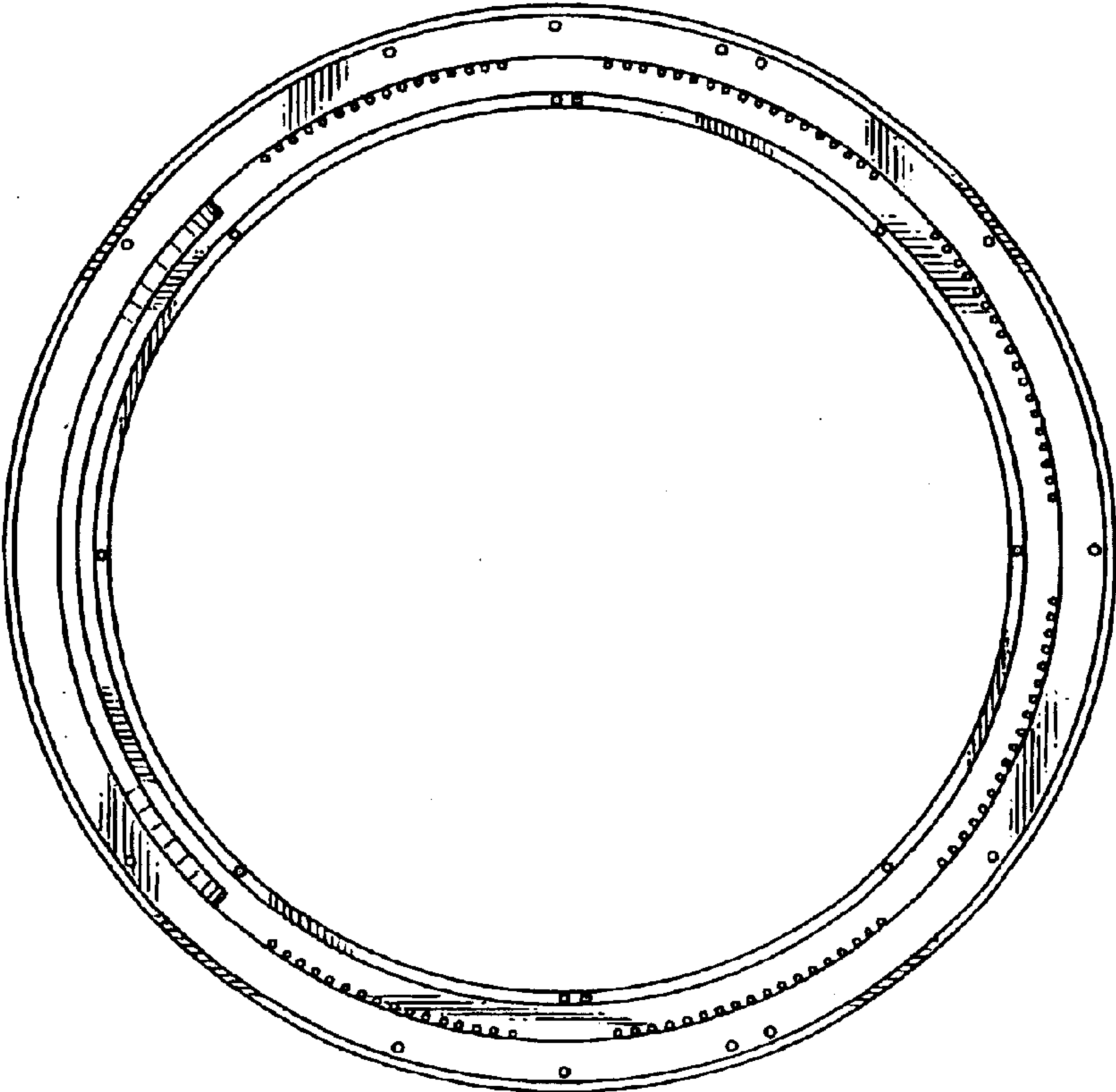


FIG.17

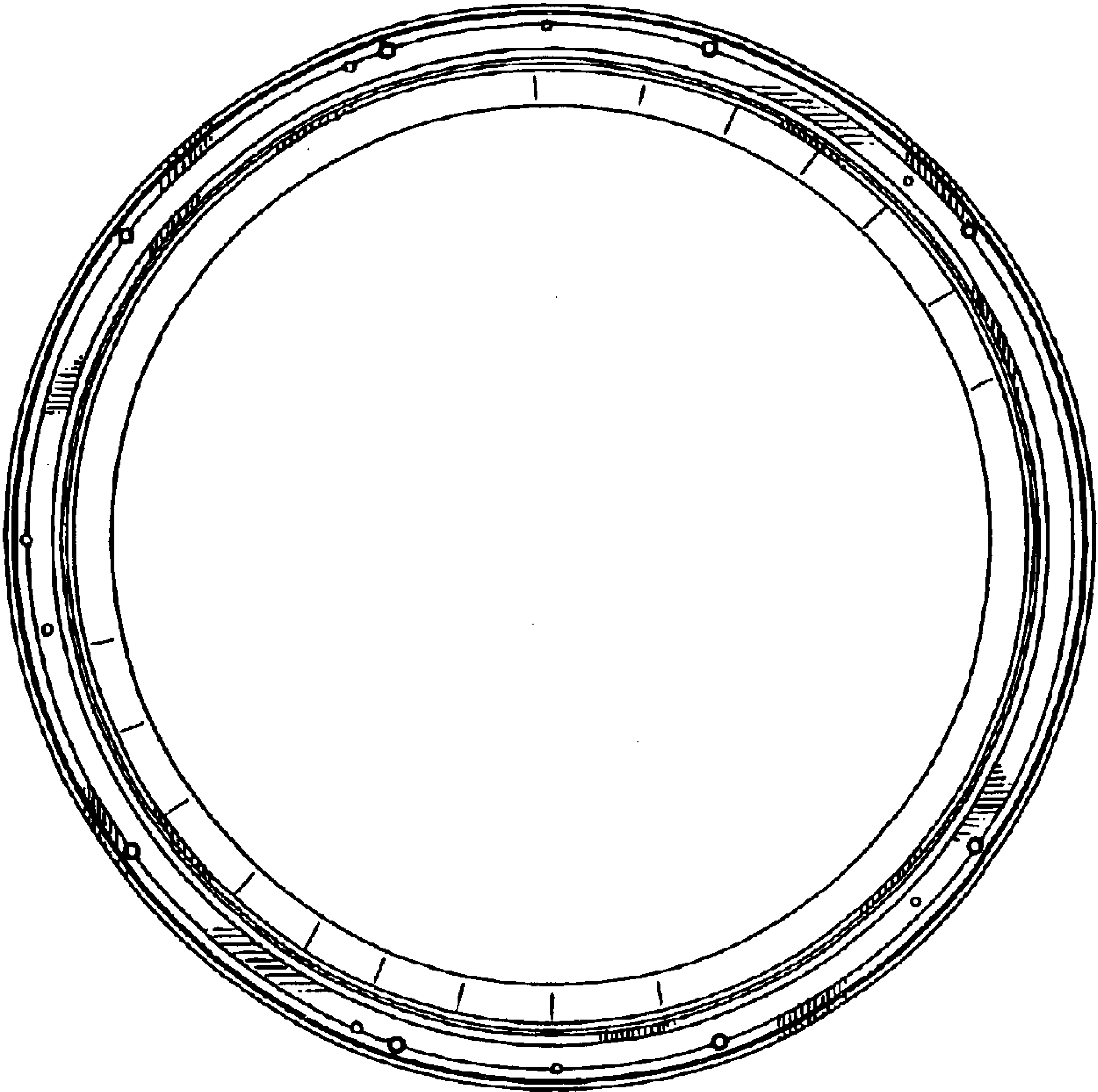


FIG.16

FIG.18

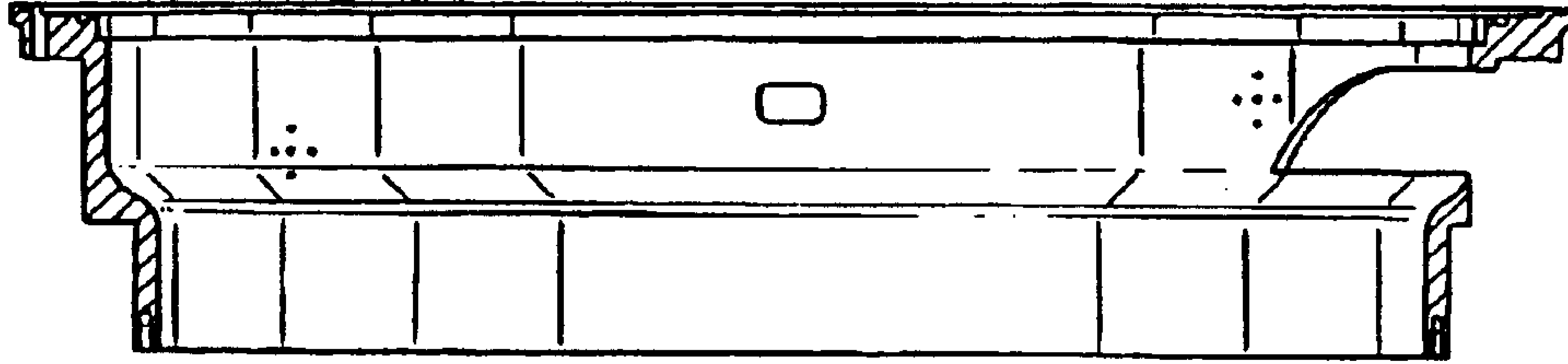


FIG.19

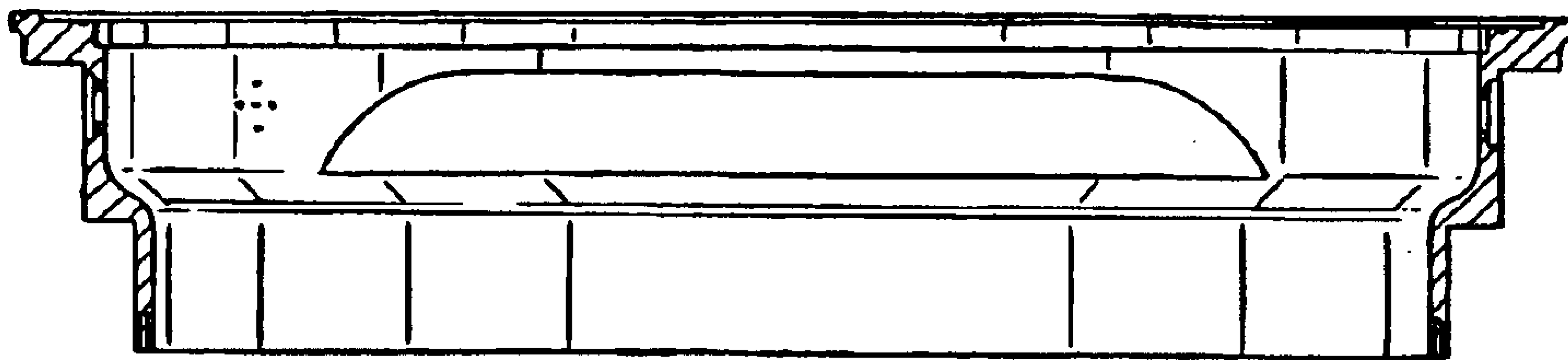


FIG.10