US00D489695S

(12) **United States Design Patent**
Komoto

(10) **Patent No.: US D489,695 S**
(45) **Date of Patent: ** May 11, 2004**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/168,230**

(22) Filed: **Sep. 30, 2002**

(30) **Foreign Application Priority Data**

Mar. 29, 2002 (JP) 2002-008489

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 310/355; 174/52.1, 52.2, 52.4; 257/666, 674, 678, 690, 692, 693, 694, 697; 361/600, 742, 744, 820

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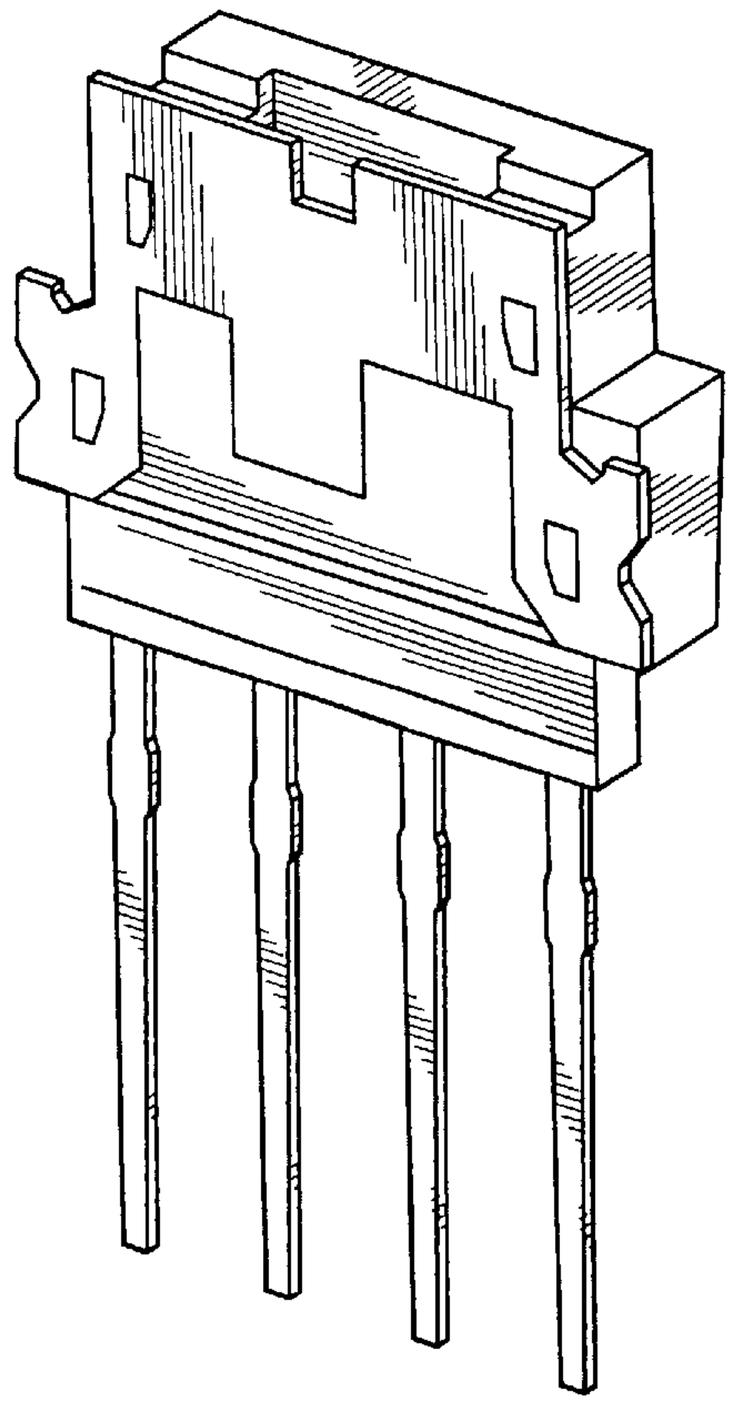
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and right side perspective view of a semiconductor device, showing my new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a top plan view thereof;
FIG. **5** is a bottom plan view thereof;
FIG. **6** is a left side elevational view thereof; and,
FIG. **7** is a right side elevational view thereof.

1 Claim, 2 Drawing Sheets



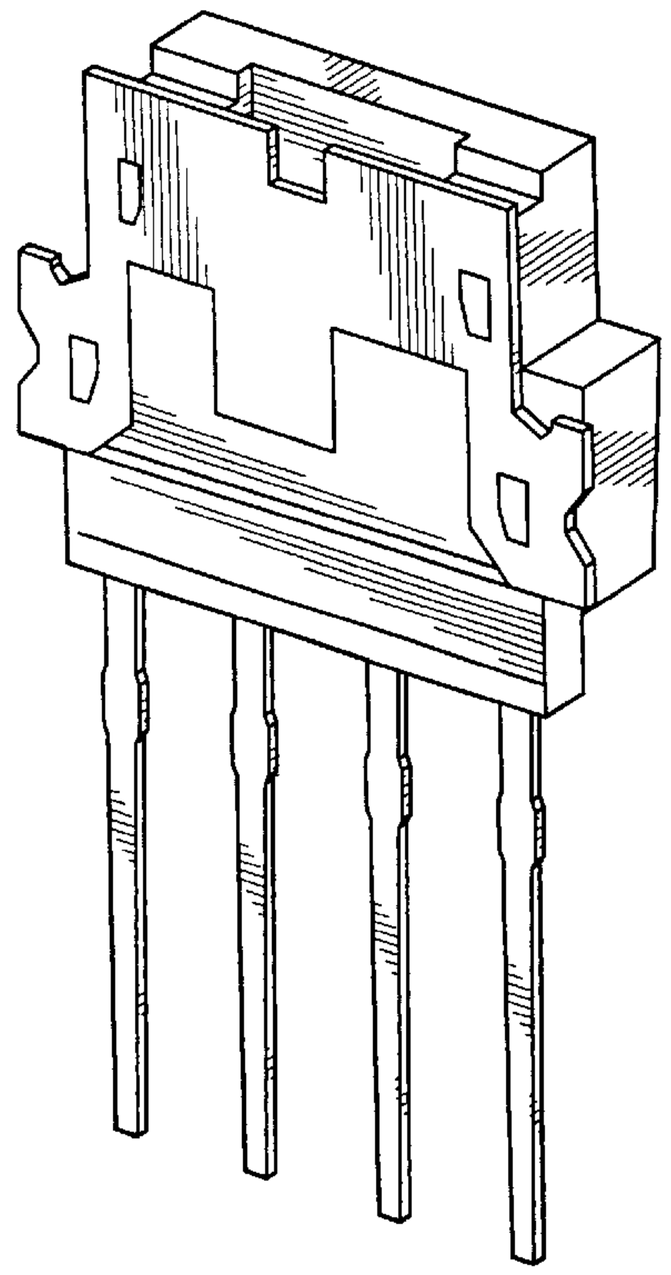


FIG. 1

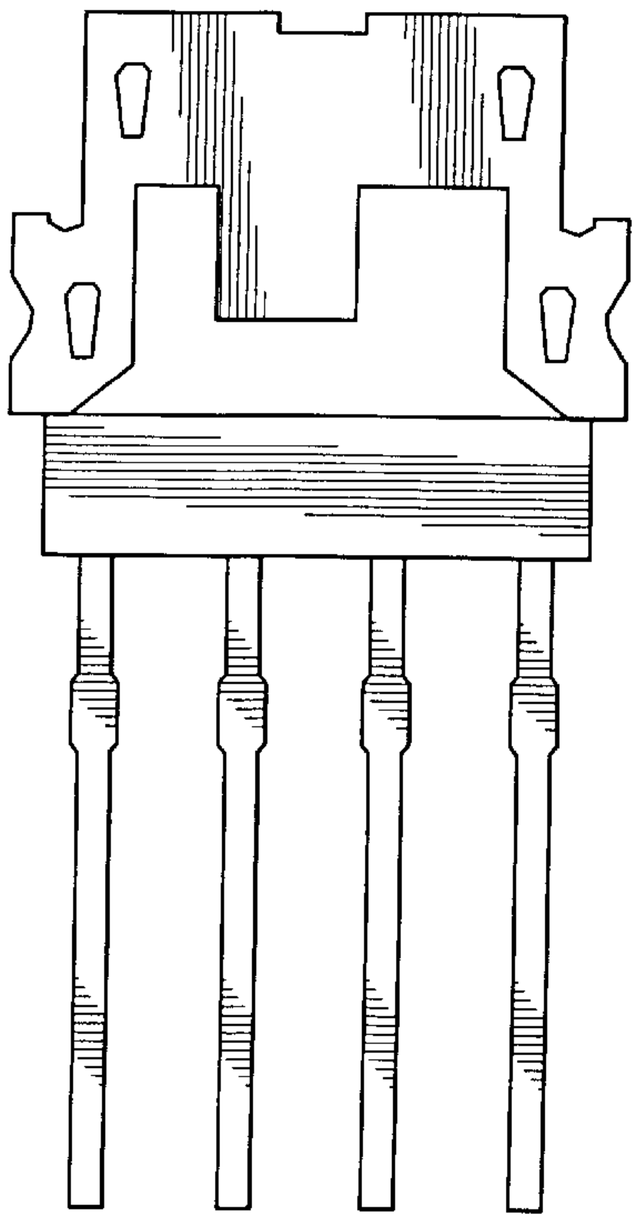


FIG. 2

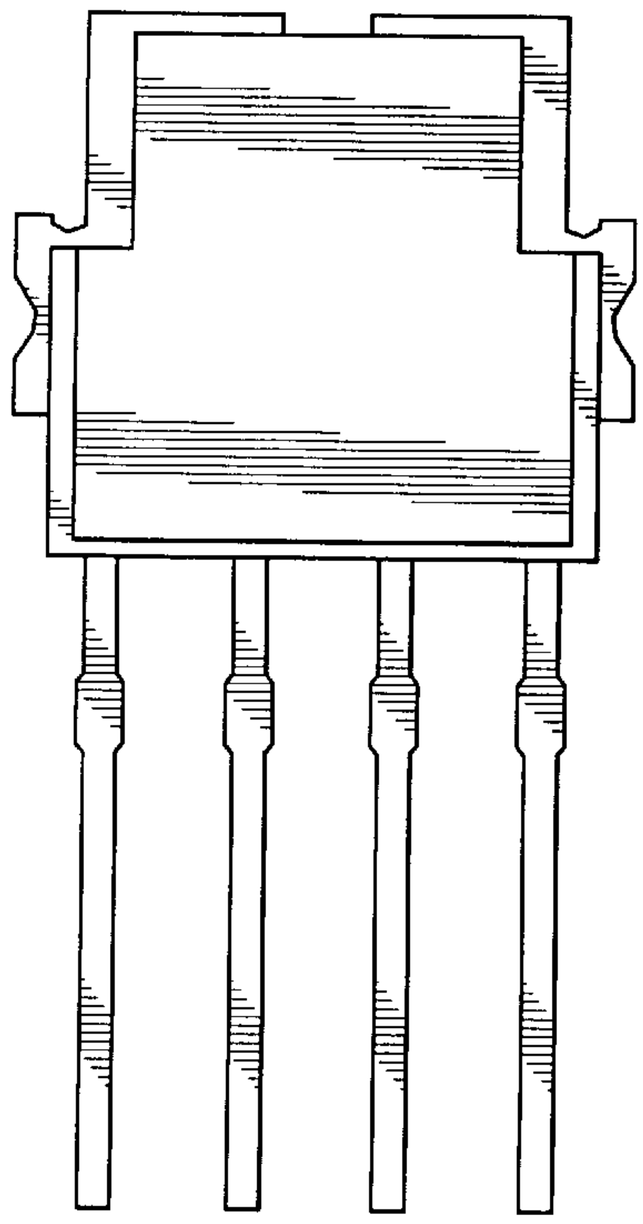


FIG. 3

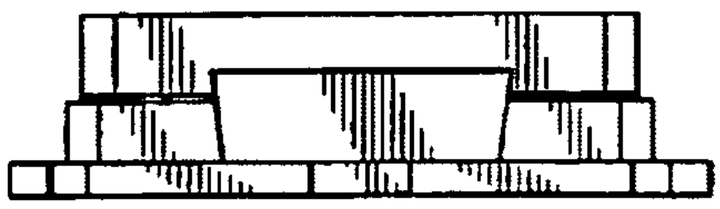


FIG. 4

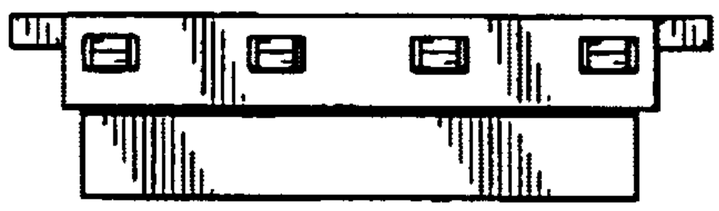


FIG. 5

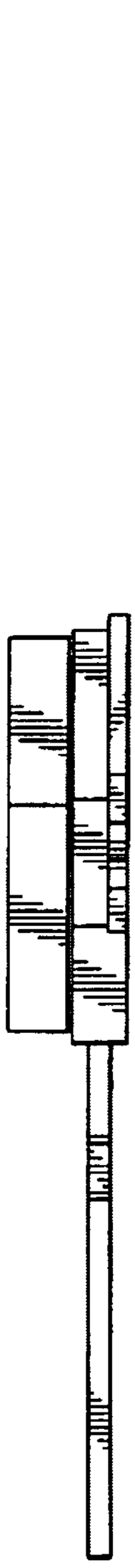


FIG. 6

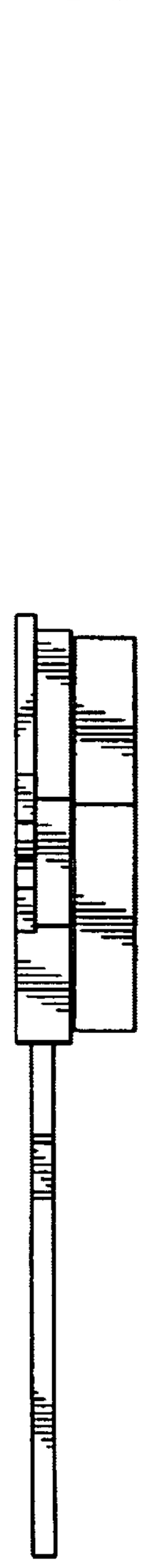


FIG. 7