



US00D487255S

(12) **United States Design Patent**  
**Dang et al.**

(10) **Patent No.:** **US D487,255 S**

(45) **Date of Patent:** **\*\* Mar. 2, 2004**

(54) **ELECTRONICS COMPONENT PACKAGE ELEMENT**

6,549,108 B2 \* 4/2003 Fausch ..... 335/129

**OTHER PUBLICATIONS**

(75) Inventors: **Tung Dang**, San Marcos, CA (US);  
**Glen Alan Cotant**, Ramona, CA (US)

Allied Electronics, 1990,pp. 402 (upper left), 615 (upper right and middle left).\*

(73) Assignee: **Pulse Engineering, Inc.**, San Diego, CA (US)

\* cited by examiner

(\*\*) Term: **14 Years**

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*Assistant Examiner*—Selina Sikder

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(21) Appl. No.: **29/177,596**

(57) **CLAIM**

(22) Filed: **Mar. 10, 2003**

The ornamental design of an electronics components package element, as shown and described herein.

(51) **LOC (7) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Search** ..... D13/182; 29/602.1; 174/17 VA; 200/306; 220/260; 335/78, 80, 122, 132, 151, 199, 202; 361/626, 633, 819; 439/362, 564, 709, 710, 715, 716

**DESCRIPTION**

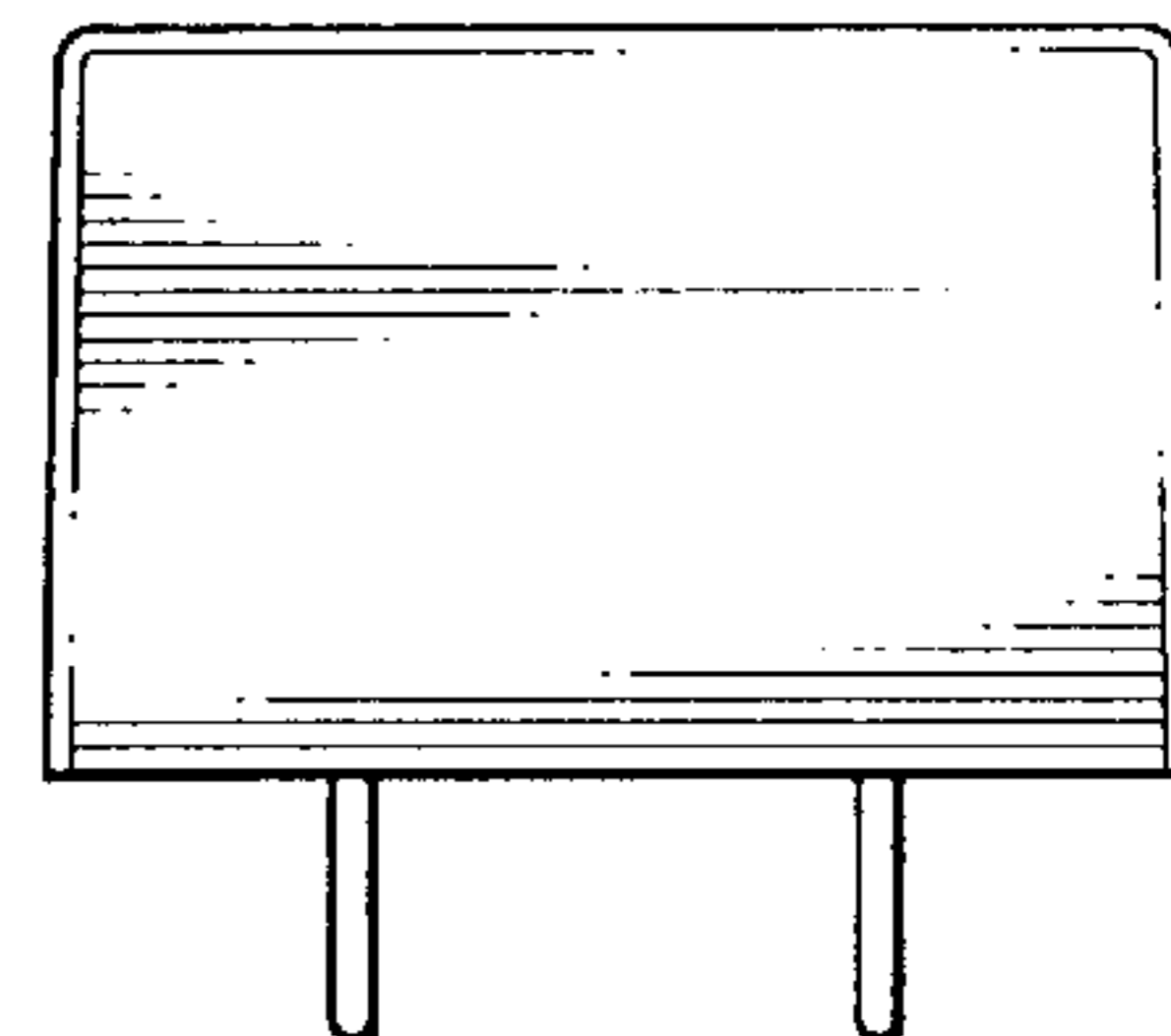
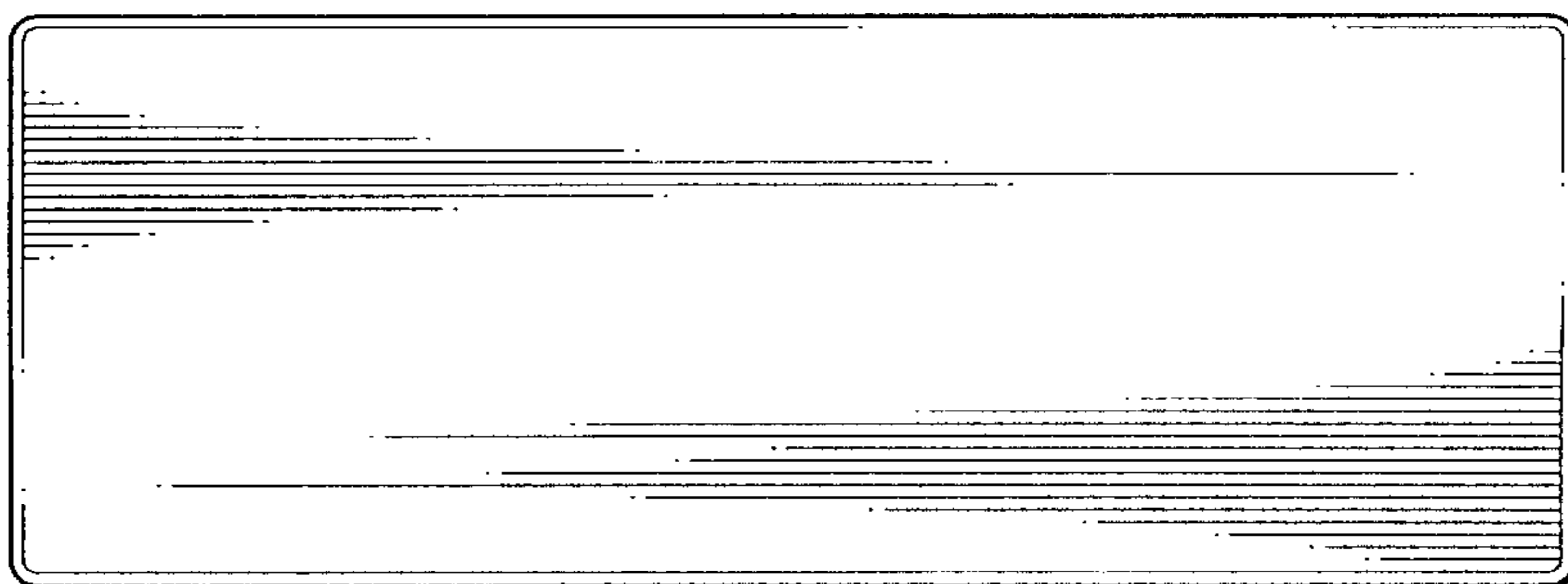
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FIG. 1 is a side elevation view of a first embodiment of an electronics component package, showing our new design; FIG. 2 is a top plan view thereof; FIG. 3 is a bottom plan view thereof; FIG. 4 is a front elevation view thereof; FIG. 5 is a side elevation view of a second embodiment of an electronics component package, showing our new design; FIG. 6 is a top plan view thereof; FIG. 7 is a bottom plan view thereof; and, FIG. 8 is a front plan view thereof.

**1 Claim, 4 Drawing Sheets**



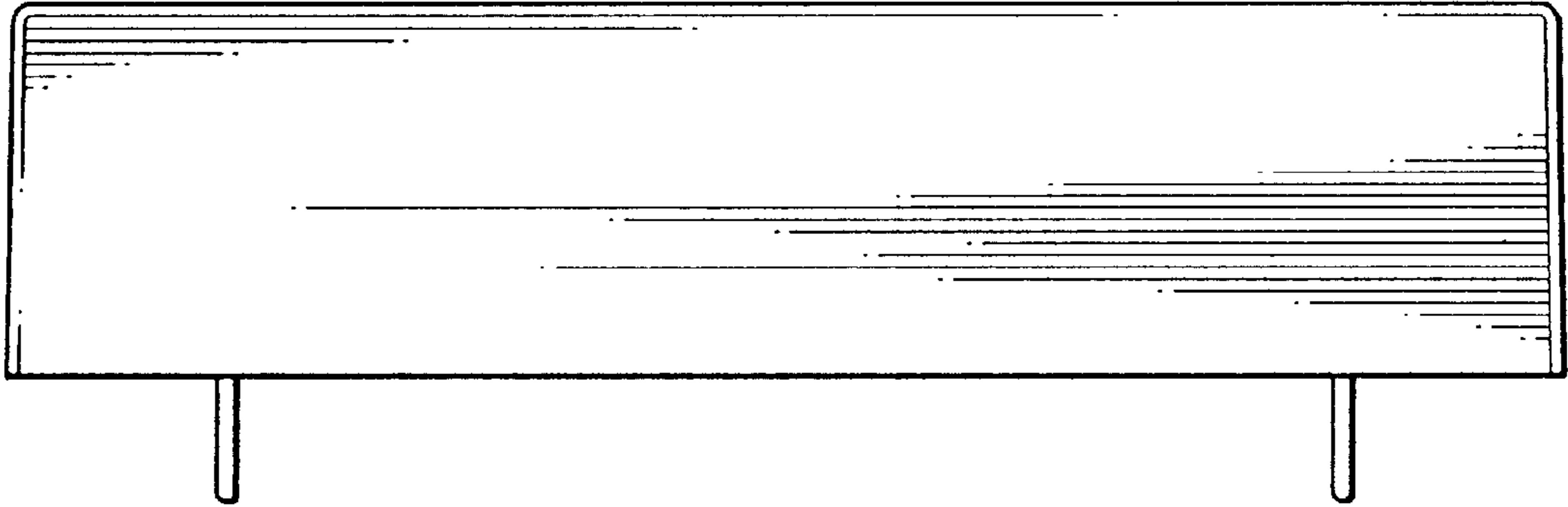


FIG. 1

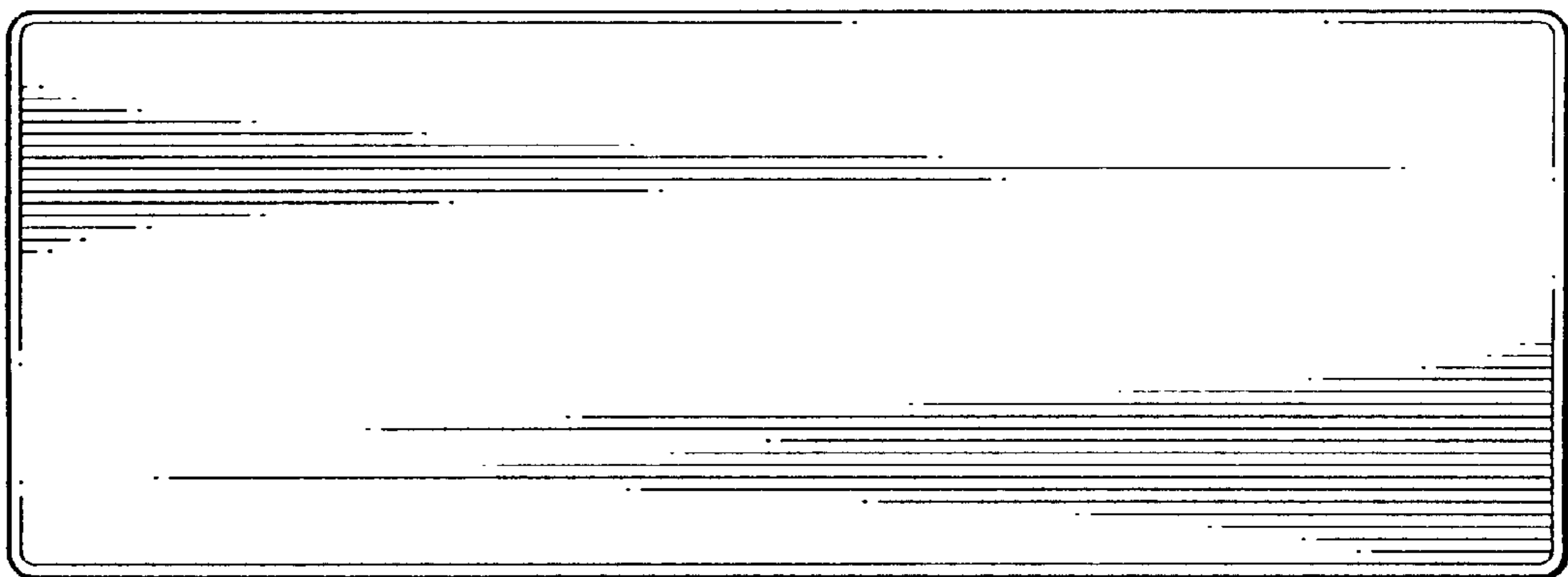


FIG. 2

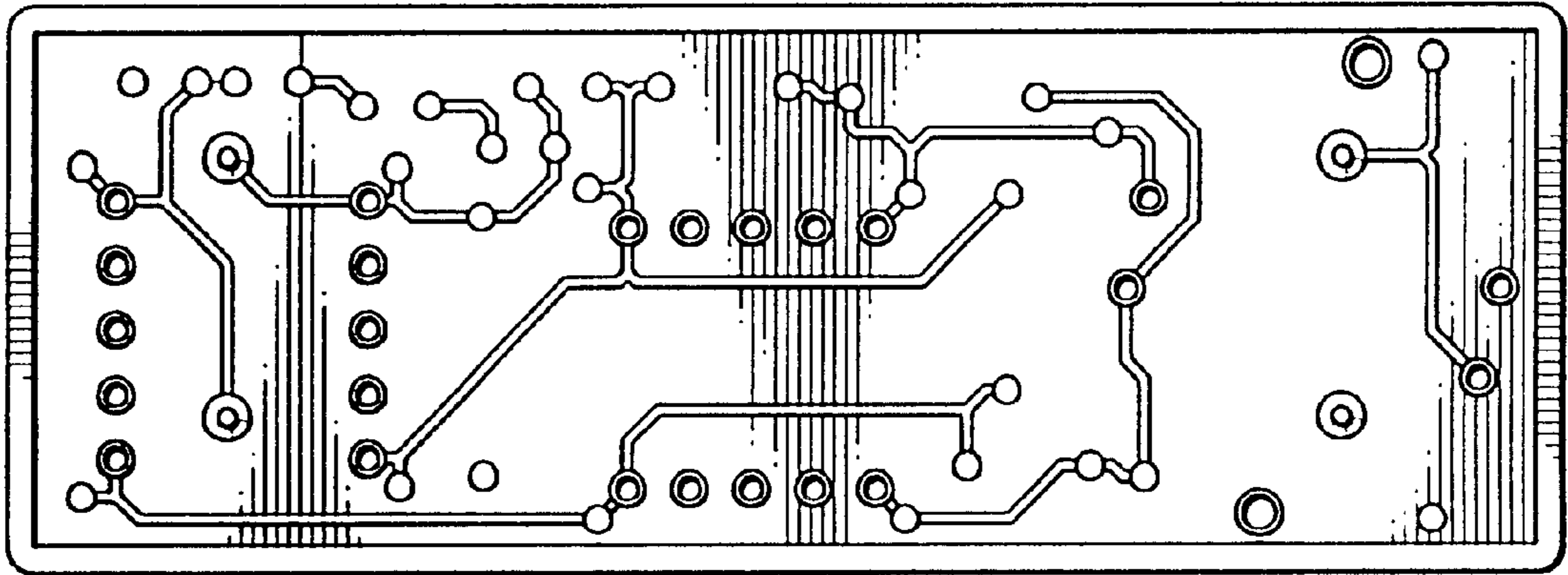


FIG. 3

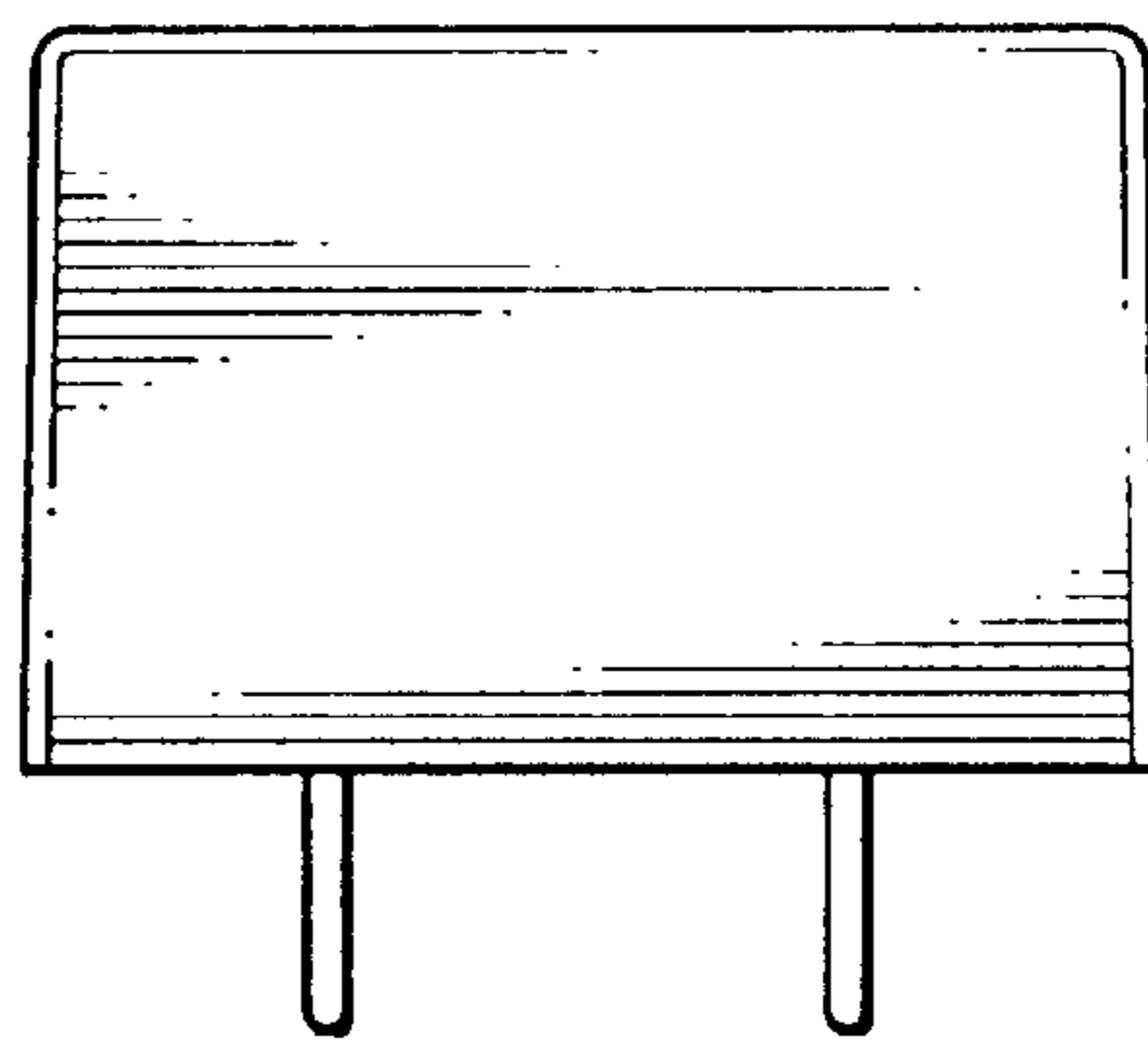


FIG. 4

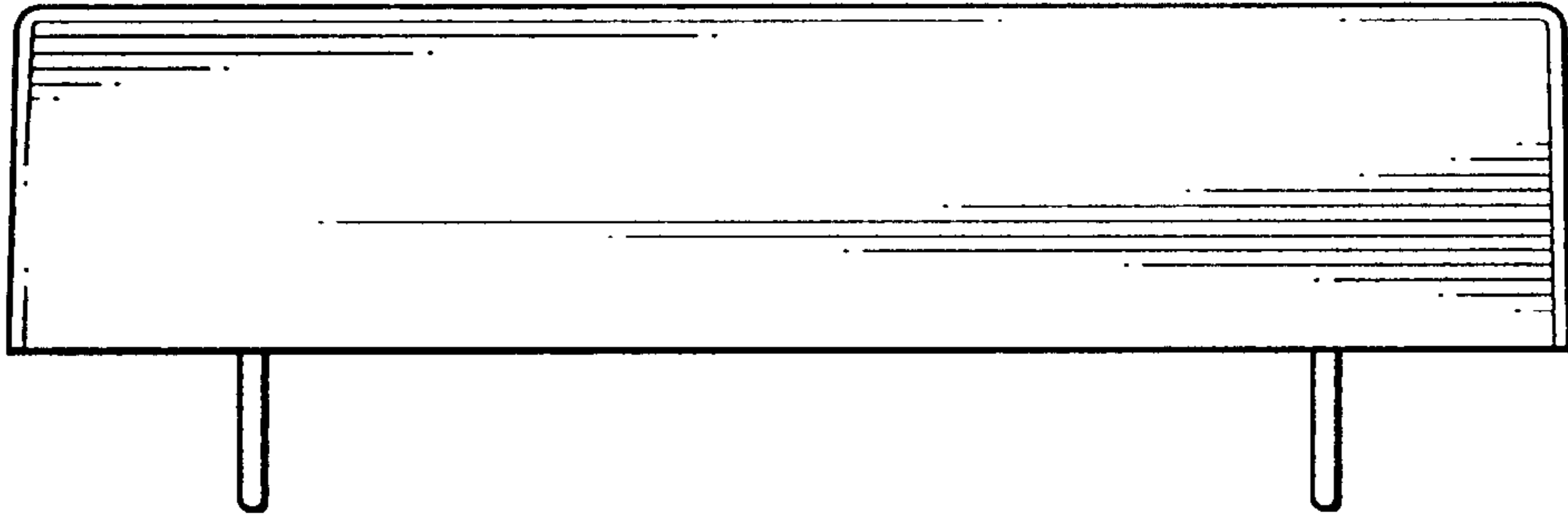


FIG. 5

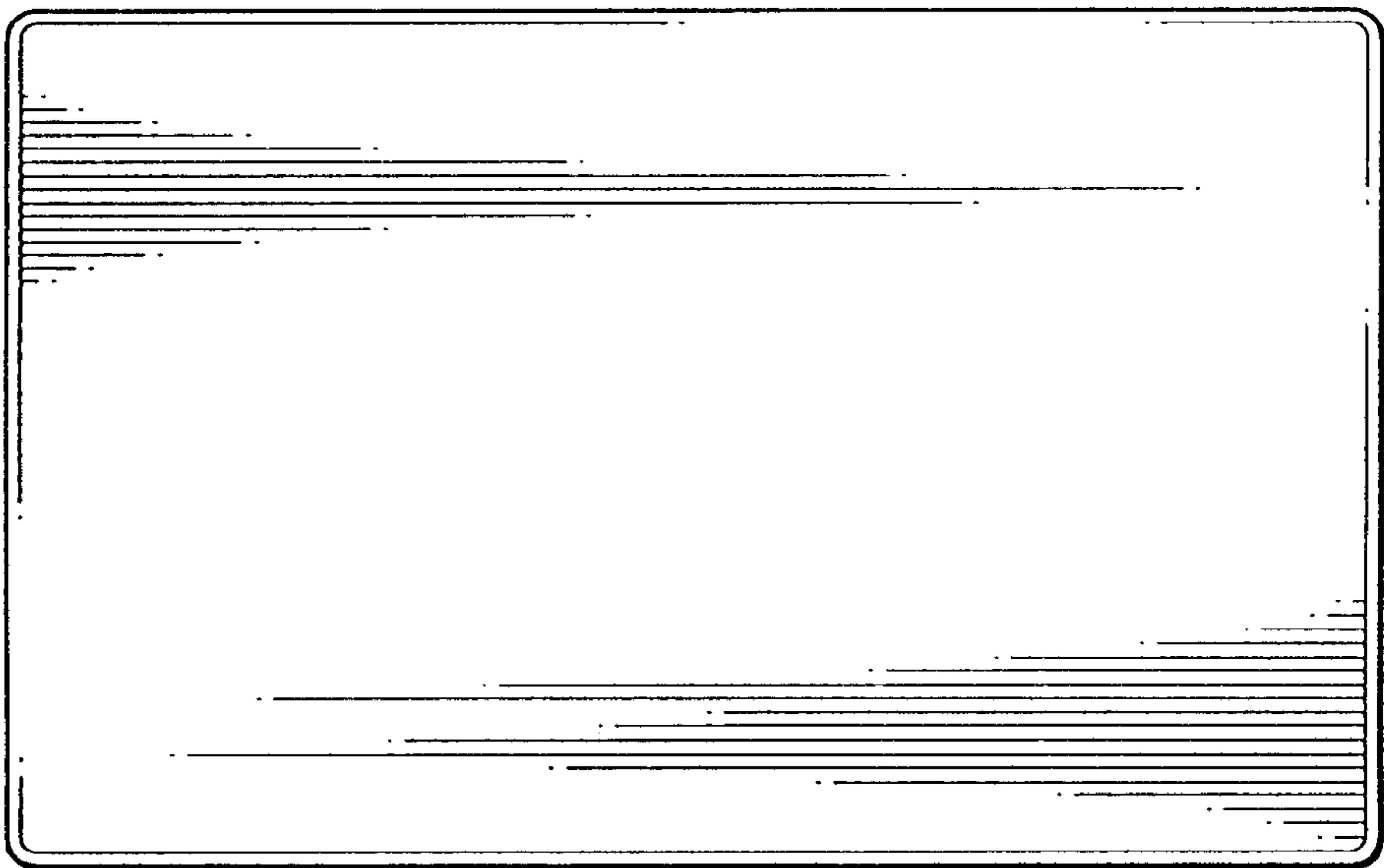


FIG. 6

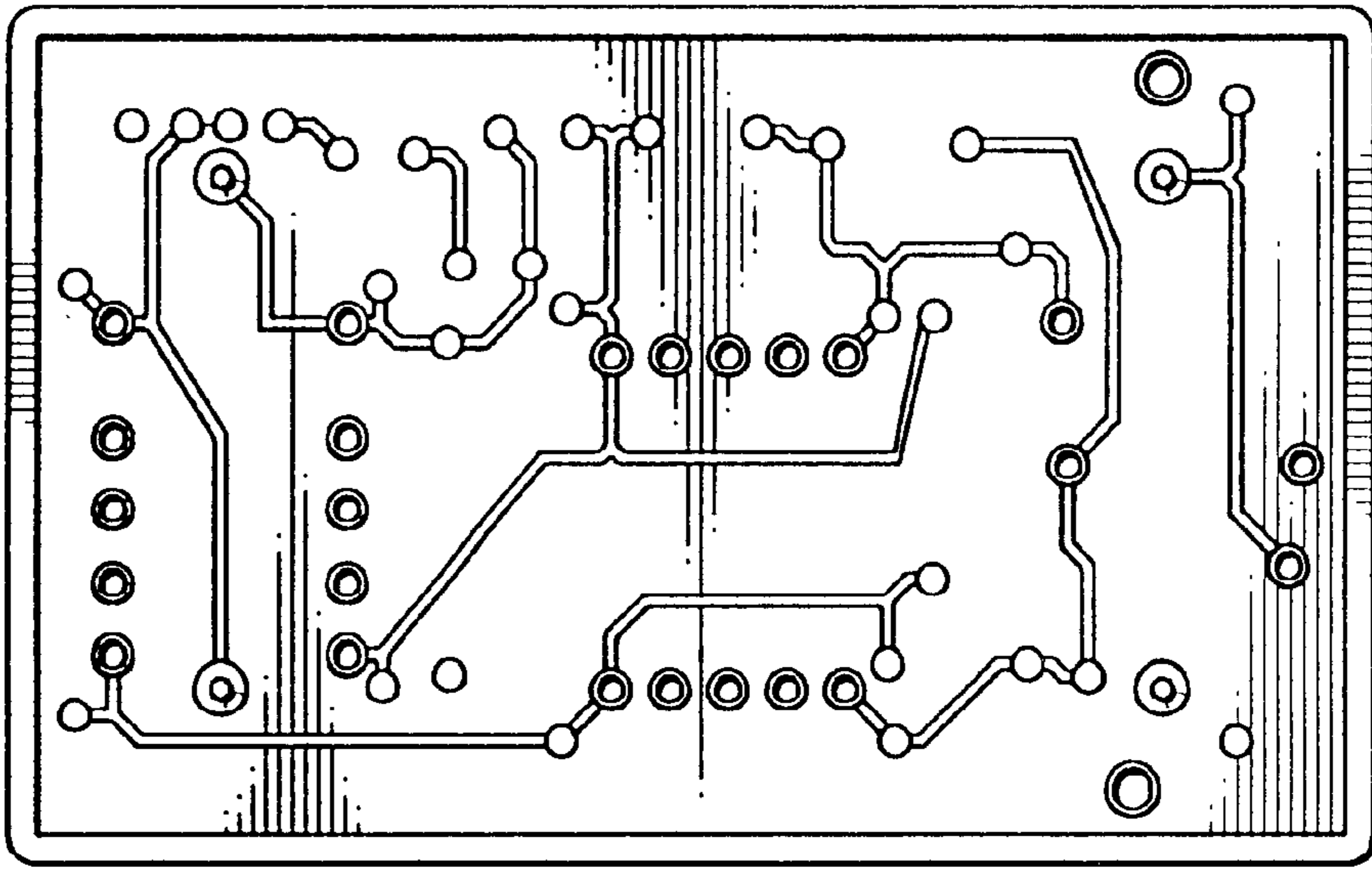


FIG. 7

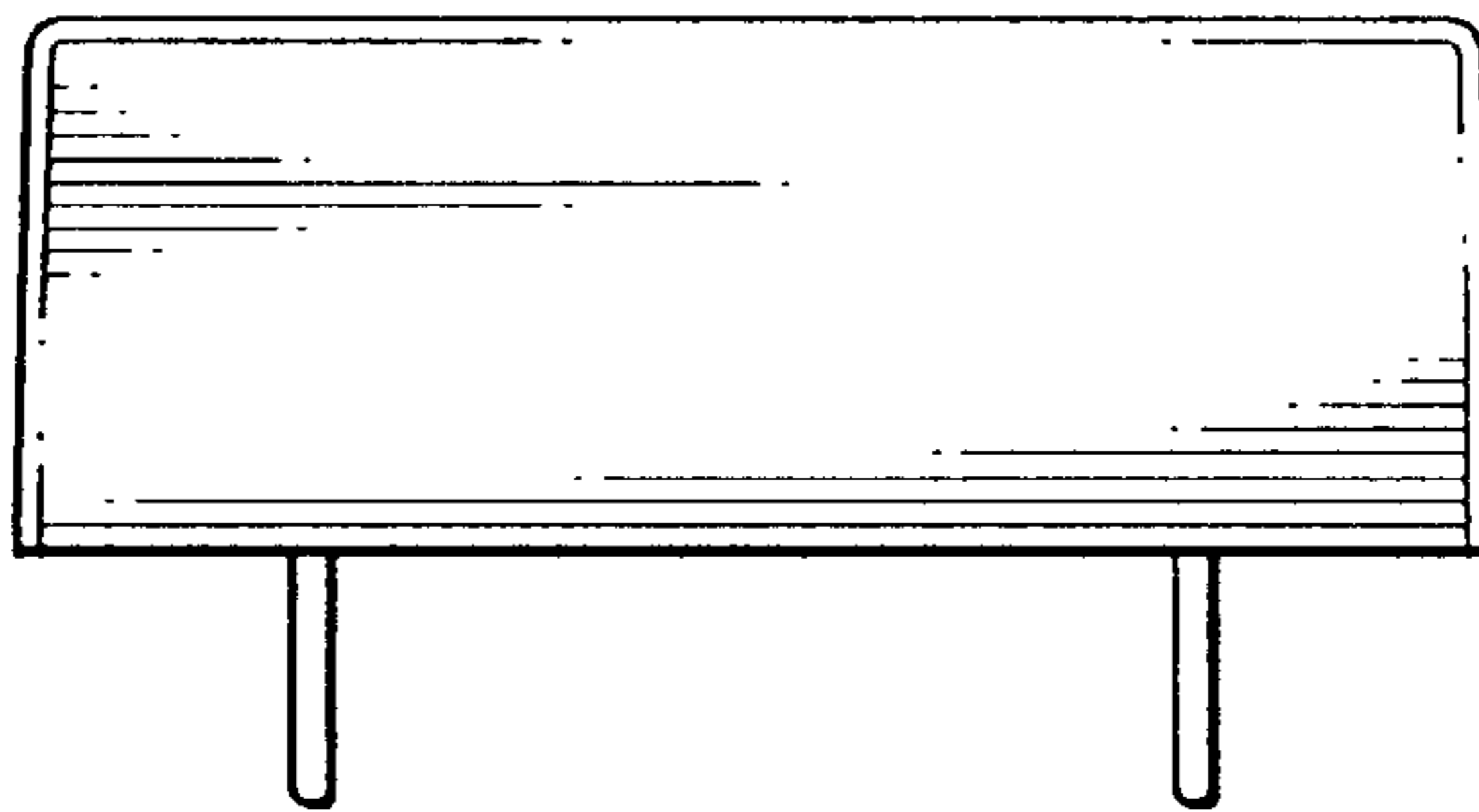


FIG. 8

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : Des. 487,255 S  
DATED : March 2, 2004  
INVENTOR(S) : Dang et al.

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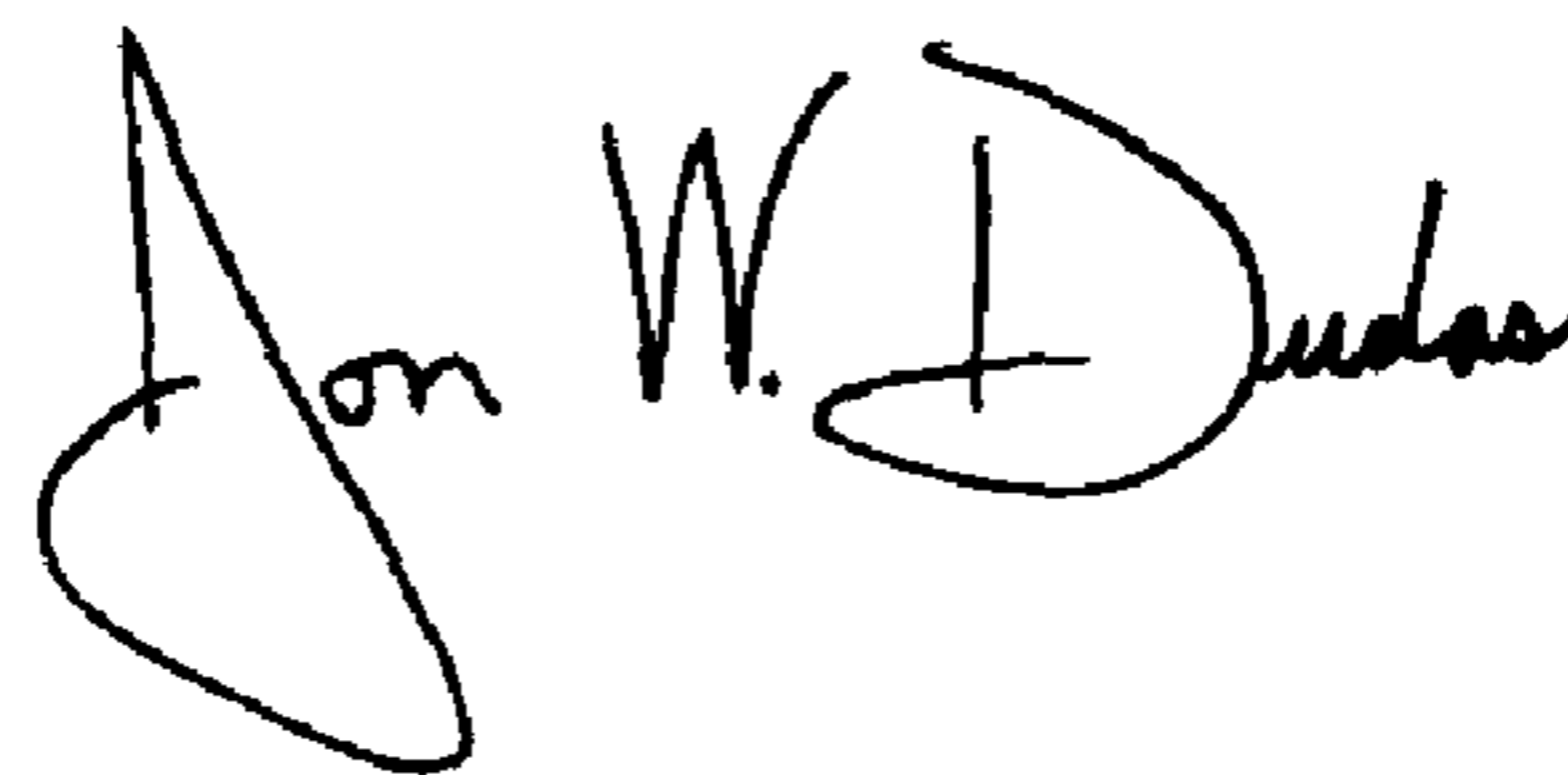
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, Item [54] and Column 1, line 1,  
Title, “**ELECTRONICS COMPONENT PACKAGE ELEMENT**” should read  
-- **ELECTRONICS COMPONENT PACKAGE** --

Title page,  
**DESCRIPTION**, “**FIG. 8** is a front plan view thereof.” should read -- **FIG. 8** is a front elevation view thereof. --

Signed and Sealed this

Twenty-ninth Day of June, 2004



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JON W. DUDAS  
*Acting Director of the United States Patent and Trademark Office*