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(12) **United States Design Patent**
Koizumi

(10) **Patent No.:** **US D481,689 S**

(45) **Date of Patent:** **** Nov. 4, 2003**

(54) **SEMICONDUCTOR DEVICE**
(75) Inventor: **Hideshi Koizumi**, Nara-ken (JP)
(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka (JP)
(**) Term: **14 Years**

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(21) Appl. No.: **29/177,395**
(22) Filed: **Mar. 11, 2003**

(57) **CLAIM**

The ornamental design for a “semiconductor device”, as shown and described.

Related U.S. Application Data

(62) Division of application No. 29/156,639, filed on Mar. 6, 2002, now Pat. No. Des. 476,296.

DESCRIPTION

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 257/666,
257/674, 678, 690, 692, 693, 694, 697,
417; 174/52.1, 52.2, 52.4; 361/600, 742,
744, 820; 372/43

FIG. 1 is a top, front, and right perspective of a semiconductor device showing my new design;
FIG. 2 is a front elevational view thereof;
FIG. 3 is a rear elevational view thereof;
FIG. 4 is a top plan view thereof;
FIG. 5 is a bottom plan view; and,
FIG. 6 is a right side elevational view, the left side elevational view being a mirror image thereof.

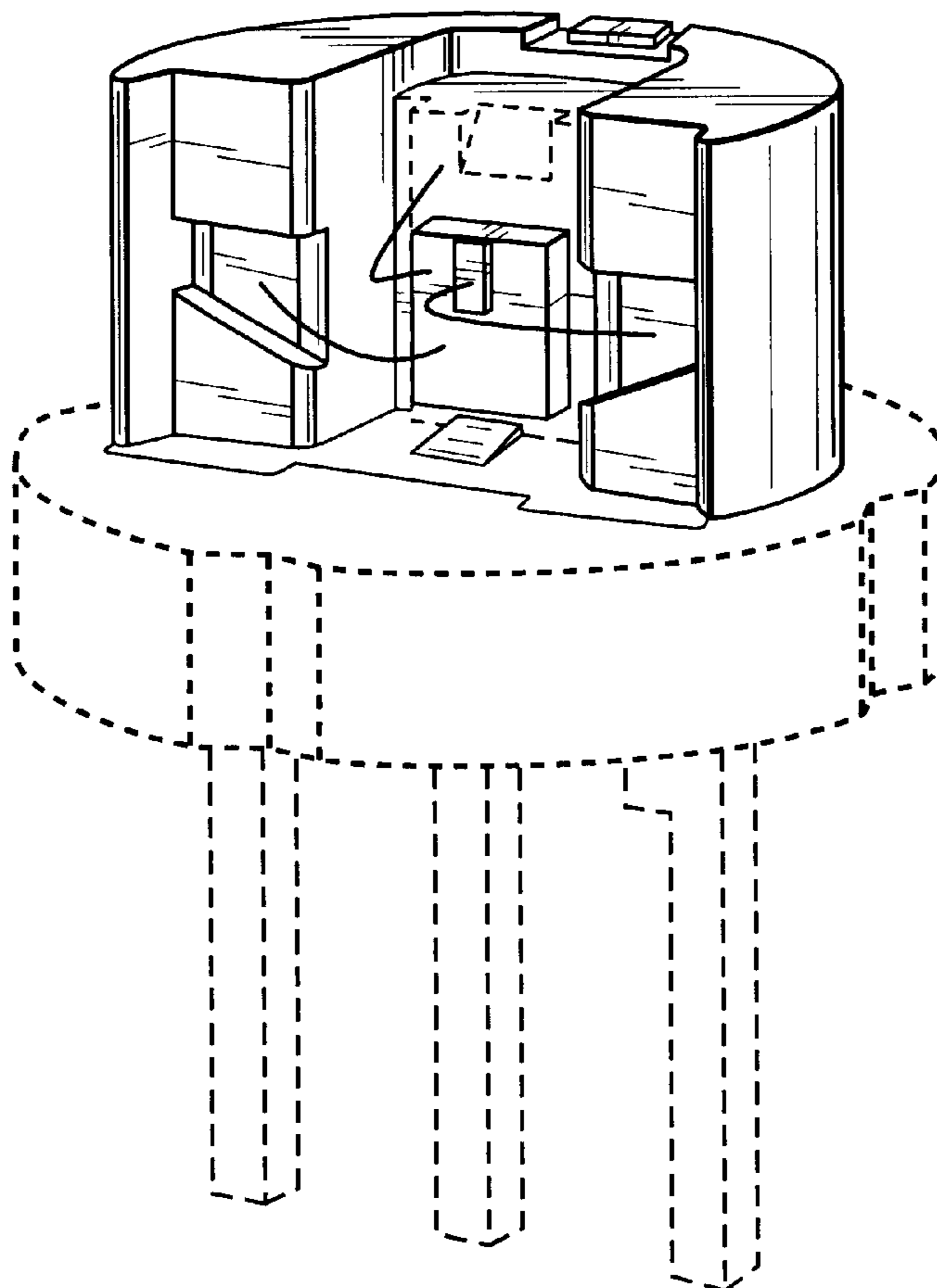
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The broken line showing of the environment is for illustrative purpose only and forms no part of the claimed design.

U.S. PATENT DOCUMENTS

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1 Claim, 5 Drawing Sheets



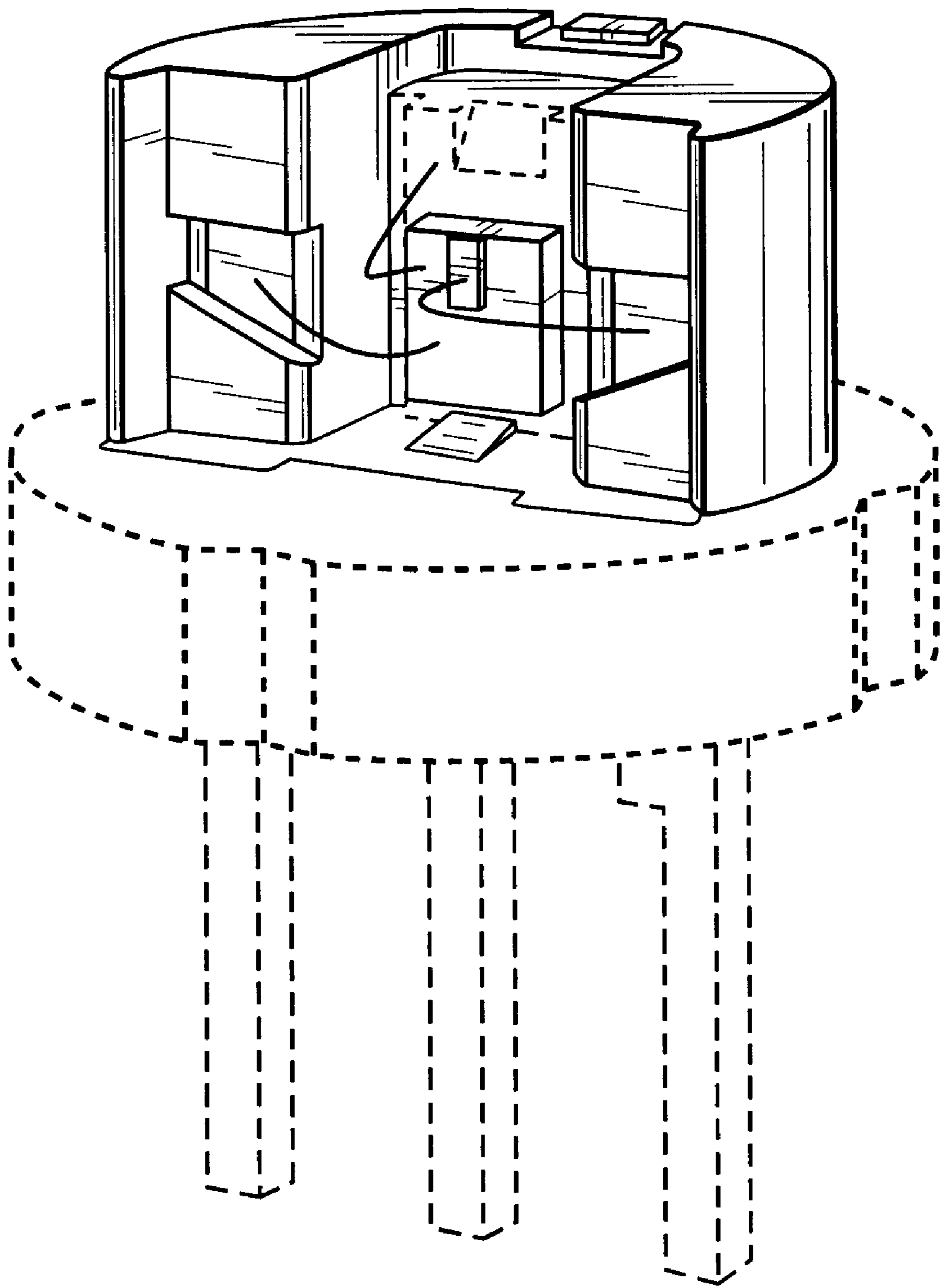


Fig. 1

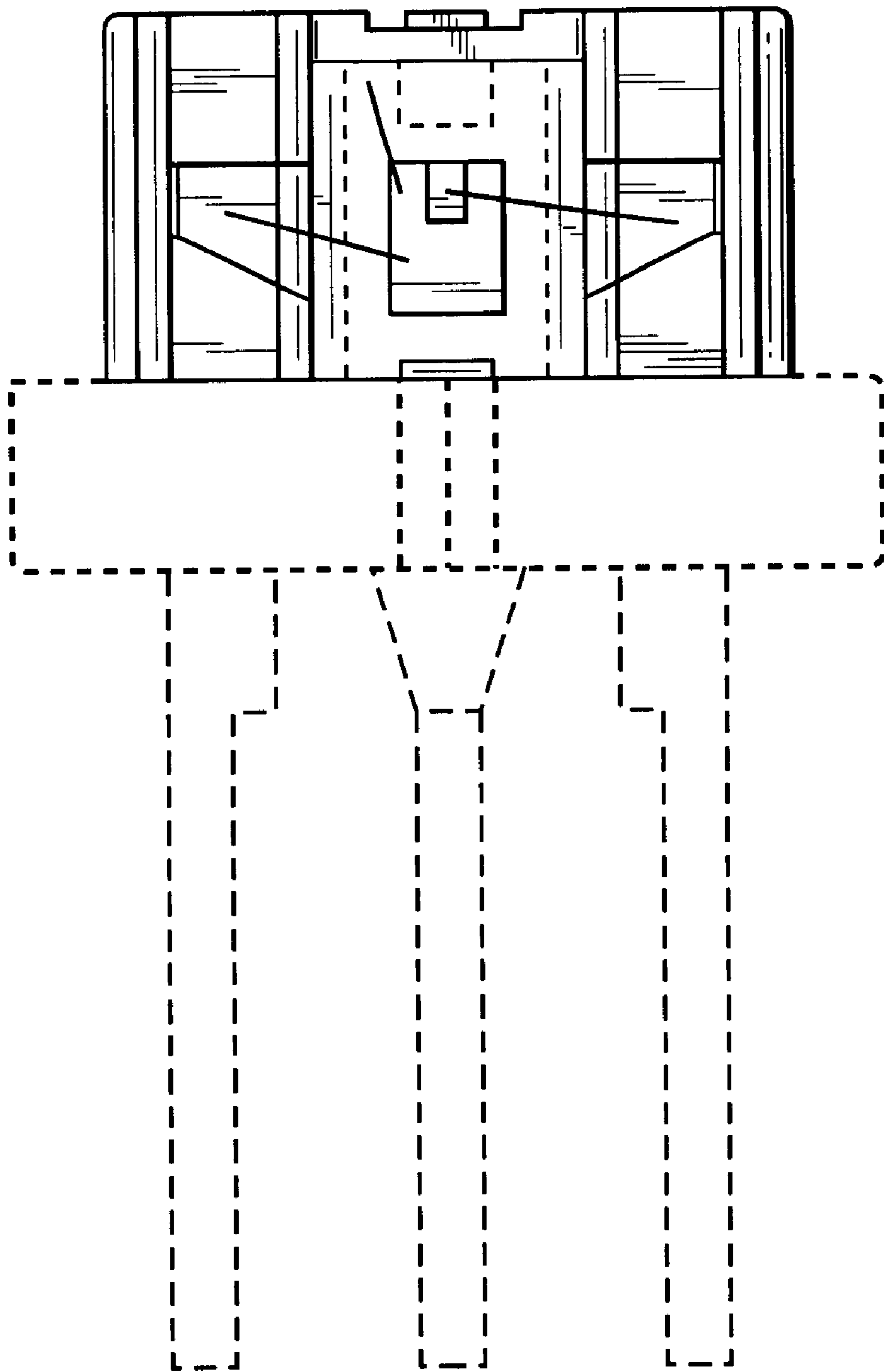


Fig. 2

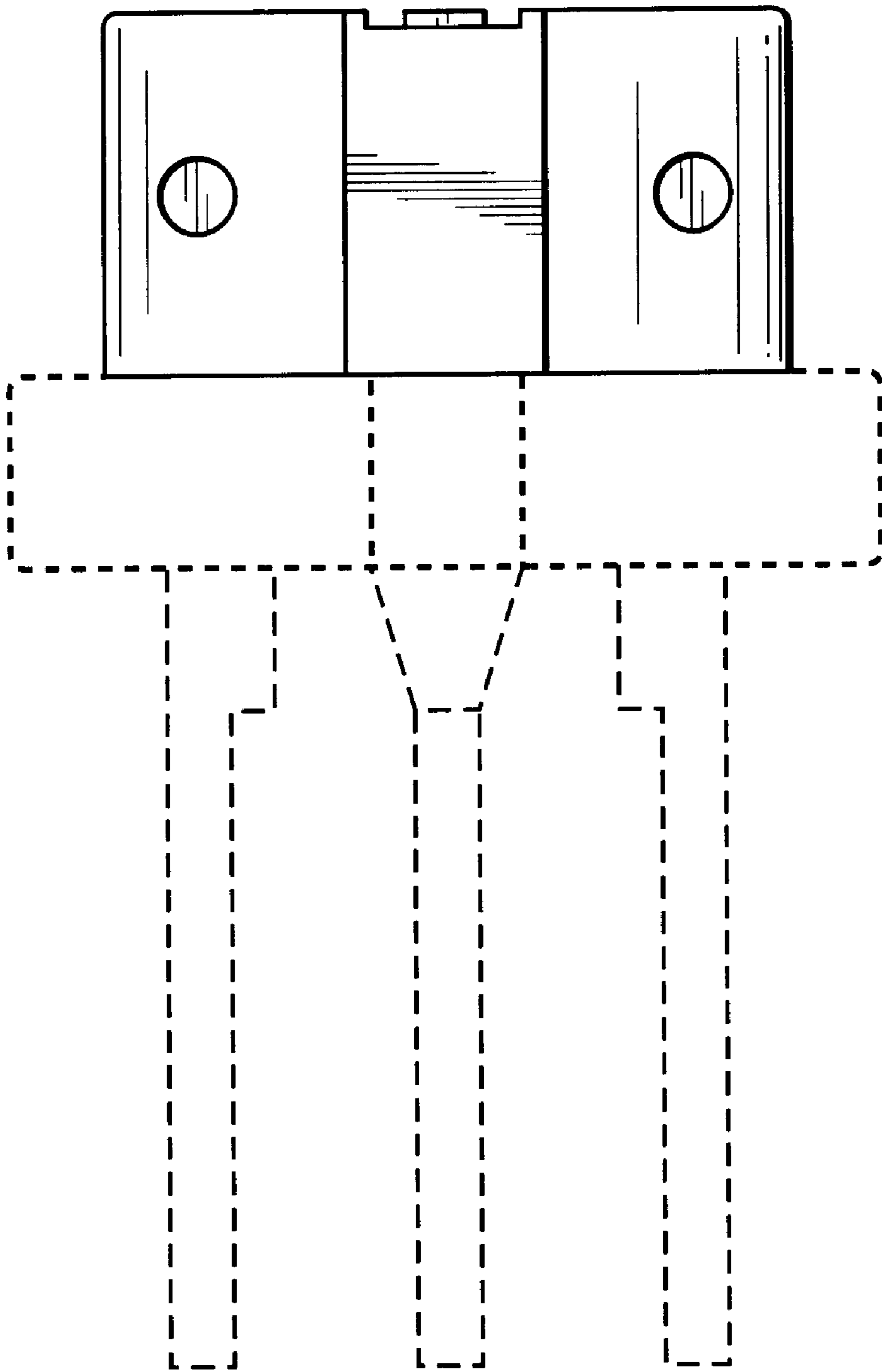


Fig. 3

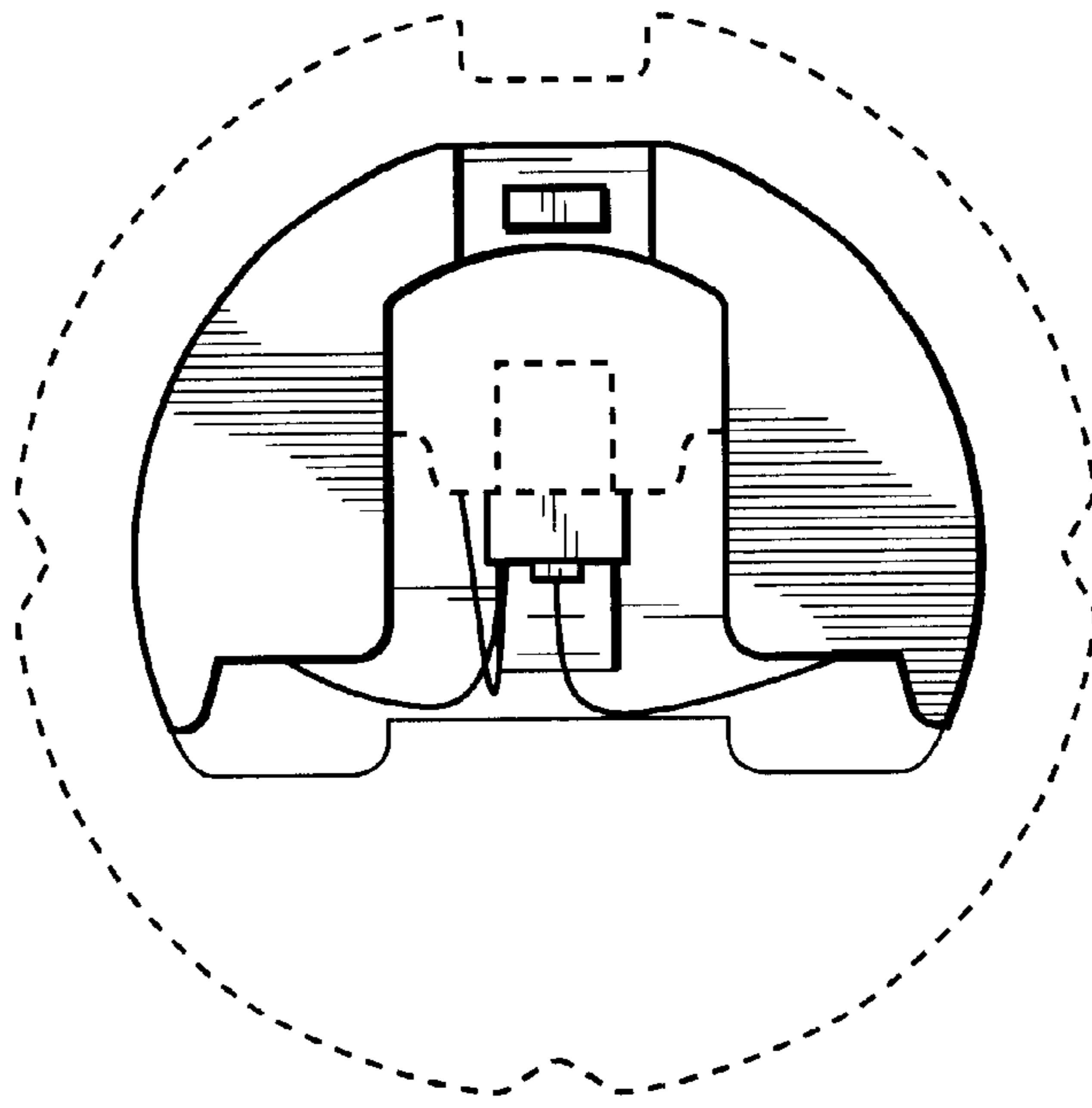


Fig. 4

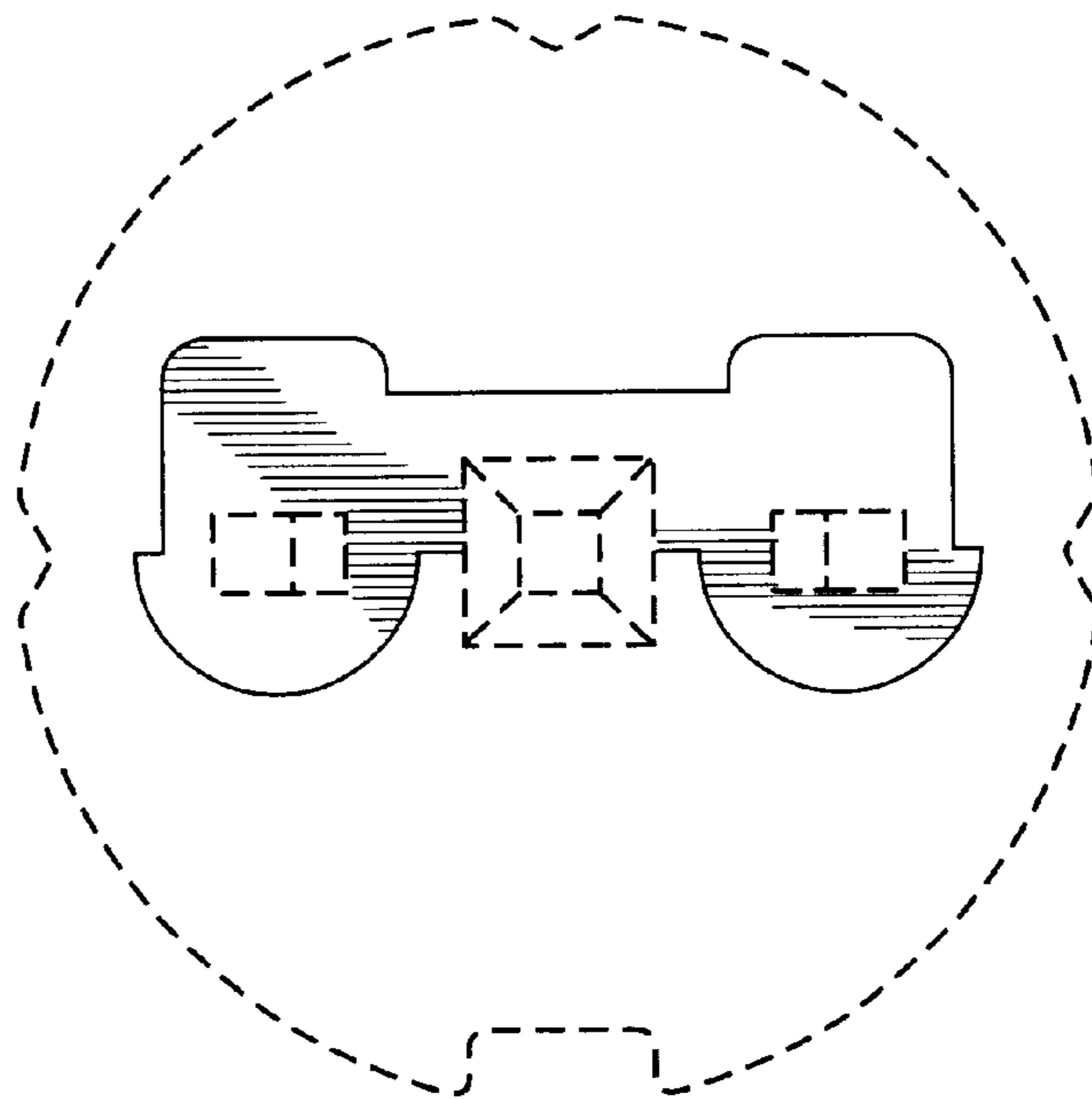


Fig. 5

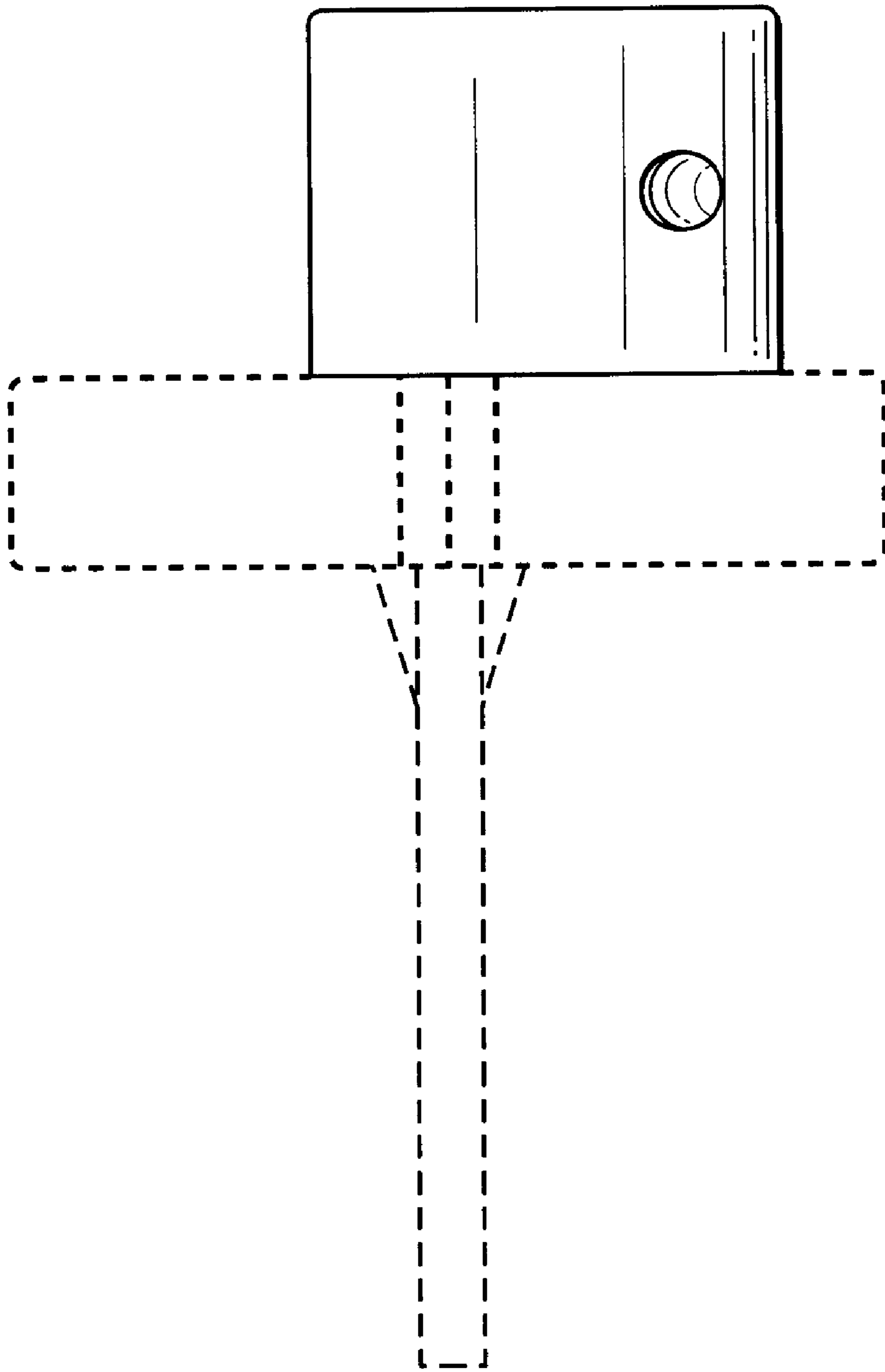


Fig. 6