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(12) United States Design Patent

Hori et al.

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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **14 Years**

(21) Appl. No.: **29/167,095**

(22) Filed: **Sep. 10, 2002**

(30) **Foreign Application Priority Data**

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Mar. 11, 2002	(JP)	2002-006216

(51) **LOC (7) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Search** D13/110, 123, D13/125, 179, 182; 174/16.3, 52.1, 52.2, 52.4; 211/261, 4.17, 162; 361/718, 728, 747, 748, 760, 774, 784, 785, 813, 820

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Catalog of a chip size package (VMN4).
Extract of Nihon Kogyo Shimbun (Newspaper) showing a chip–type Transistor package (E–CSP).

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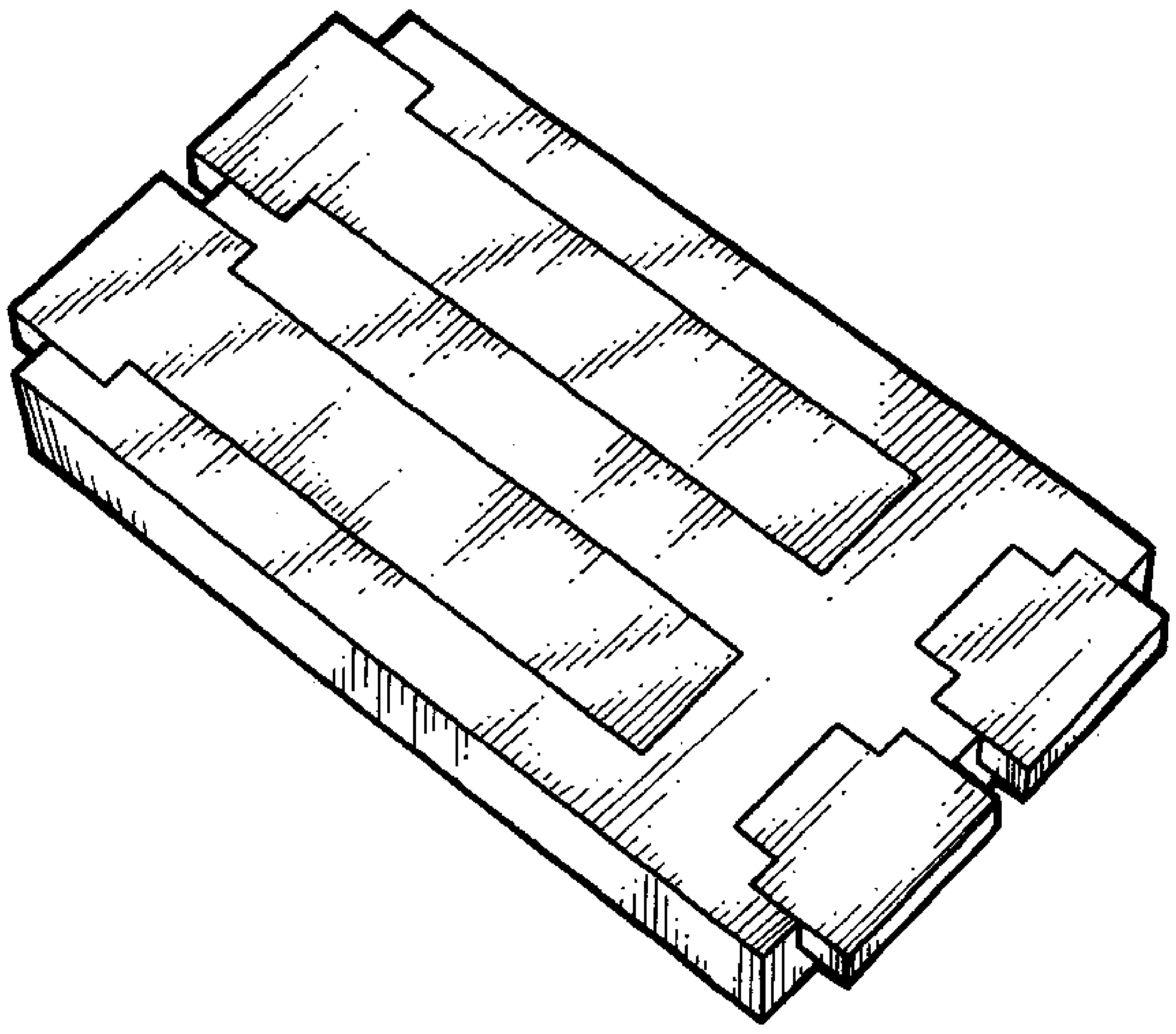
(57) **CLAIM**

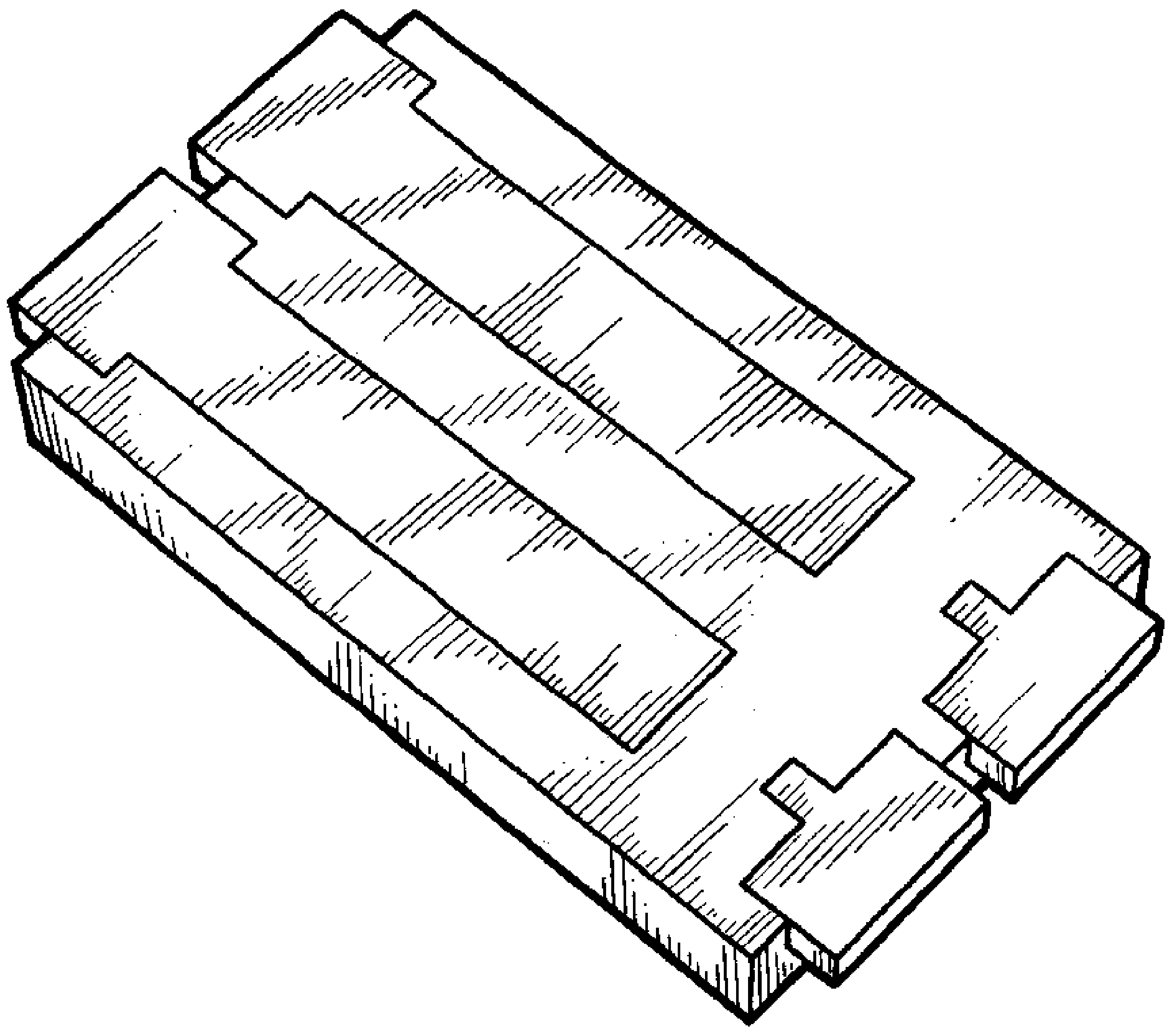
The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front perspective view of a semiconductor device, showing our new design;
FIG. **2** is a rear perspective view thereof;
FIG. **3** is a top plan view thereof; a bottom plan view being a mirror image thereof;
FIG. **4** is a right side elevational view thereof; a left side elevational view being a mirror image thereof;
FIG. **5** is a front elevational view thereof;
FIG. **6** is a rear elevational view thereof;
FIG. **7** is a front perspective view of a second embodiment of a semiconductor device, showing our new design;
FIG. **8** is a rear perspective view thereof;
FIG. **9** is a top plan view thereof; a bottom plan view being a mirror image thereof;
FIG. **10** is a right side elevational view thereof; a left side elevational view being a mirror image thereof;
FIG. **11** is a front elevational view thereof; and,
FIG. **12** is a rear elevational view thereof.

1 Claim, 4 Drawing Sheets





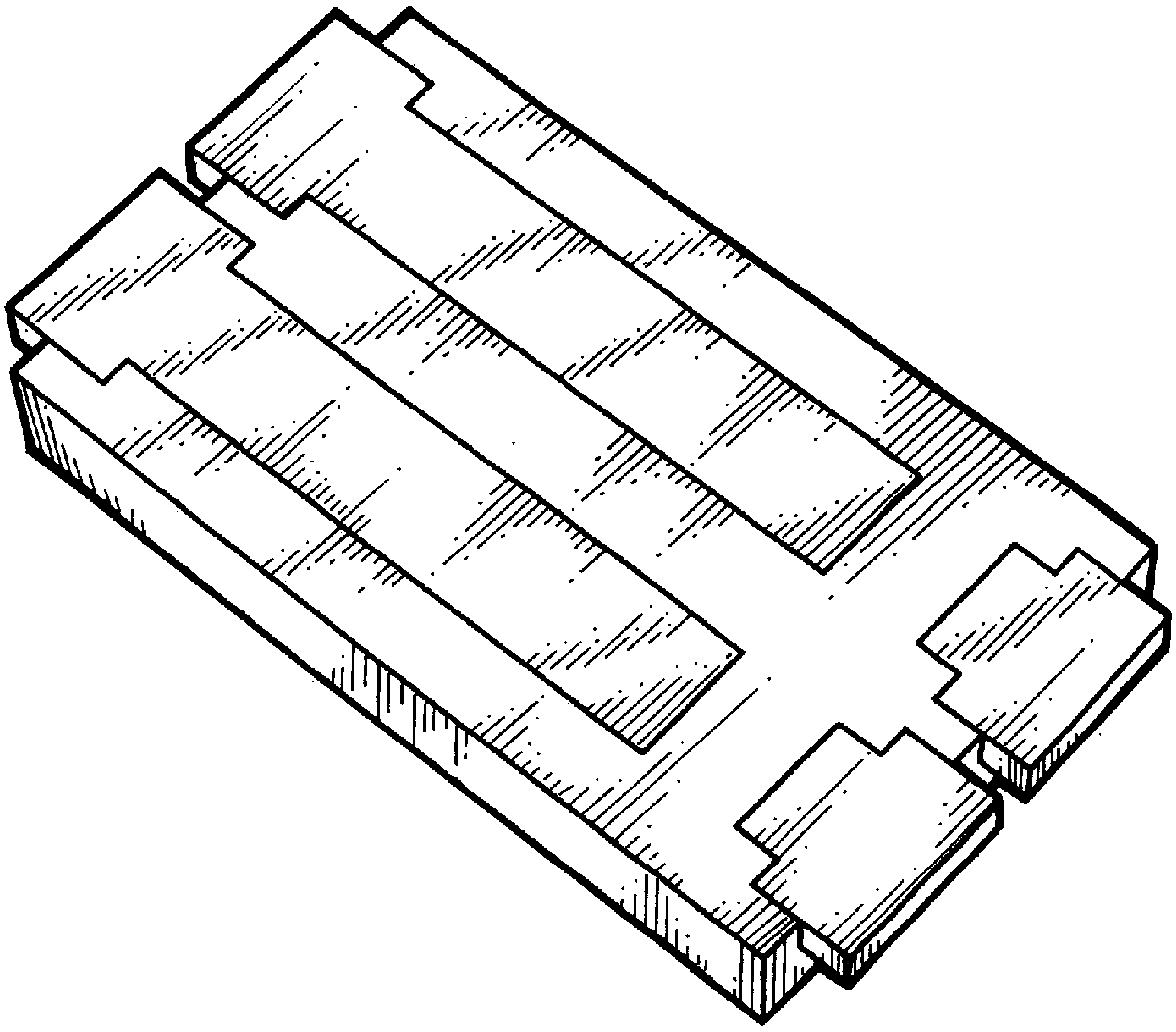


Fig.1

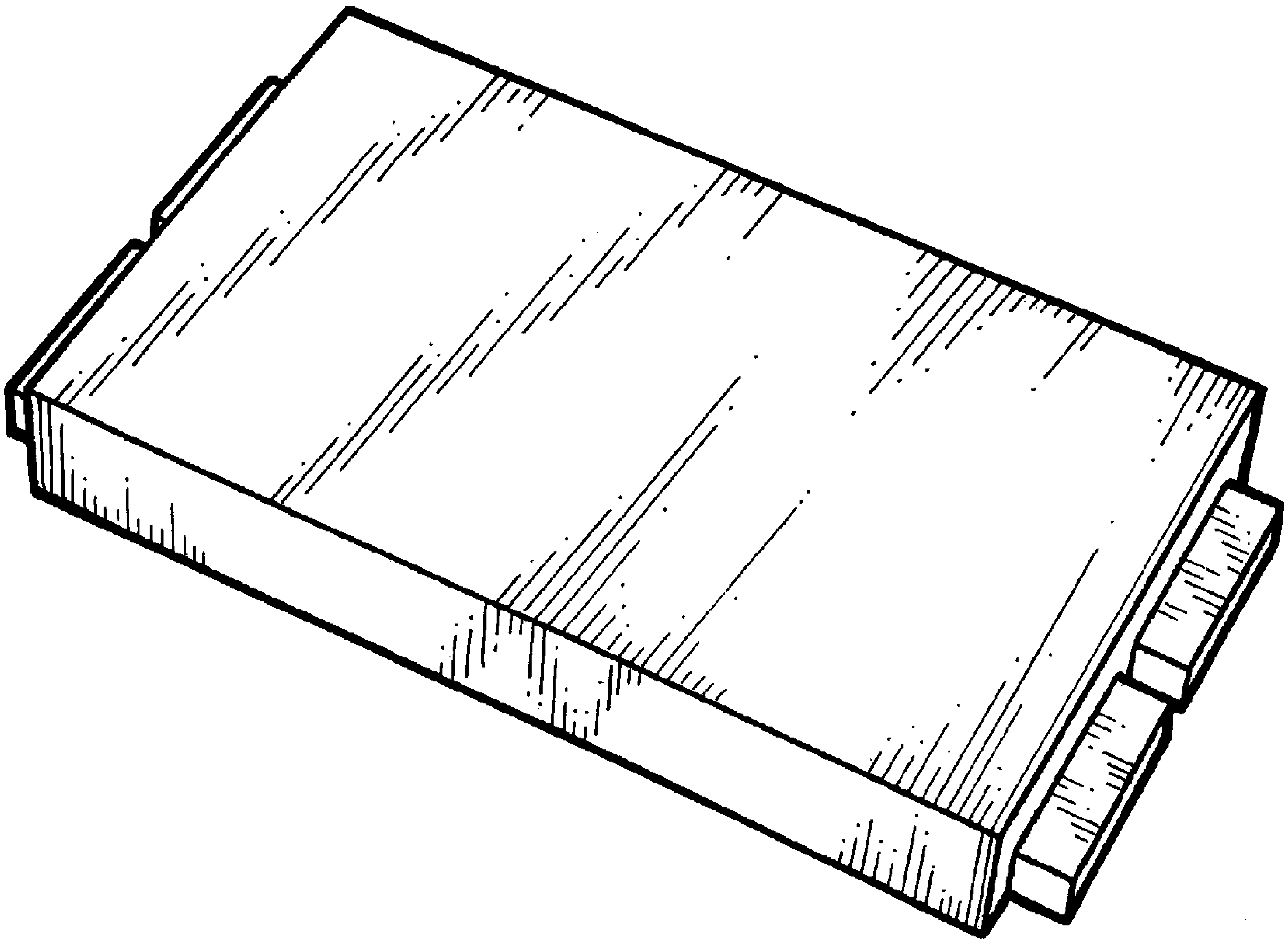


Fig.2

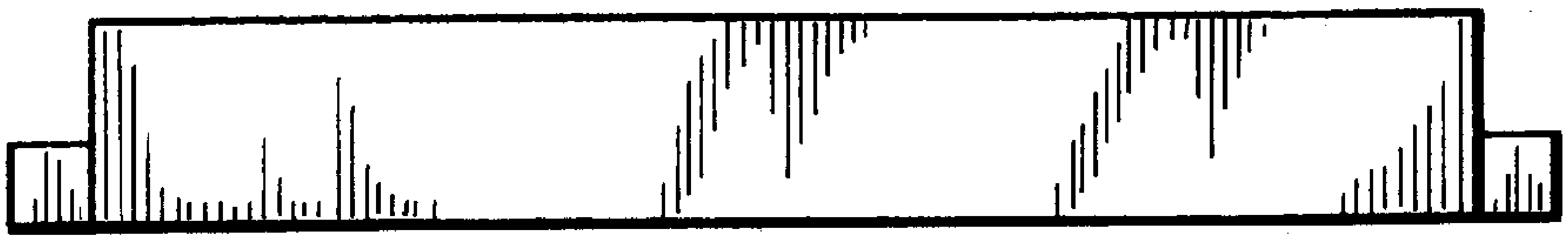


Fig.3

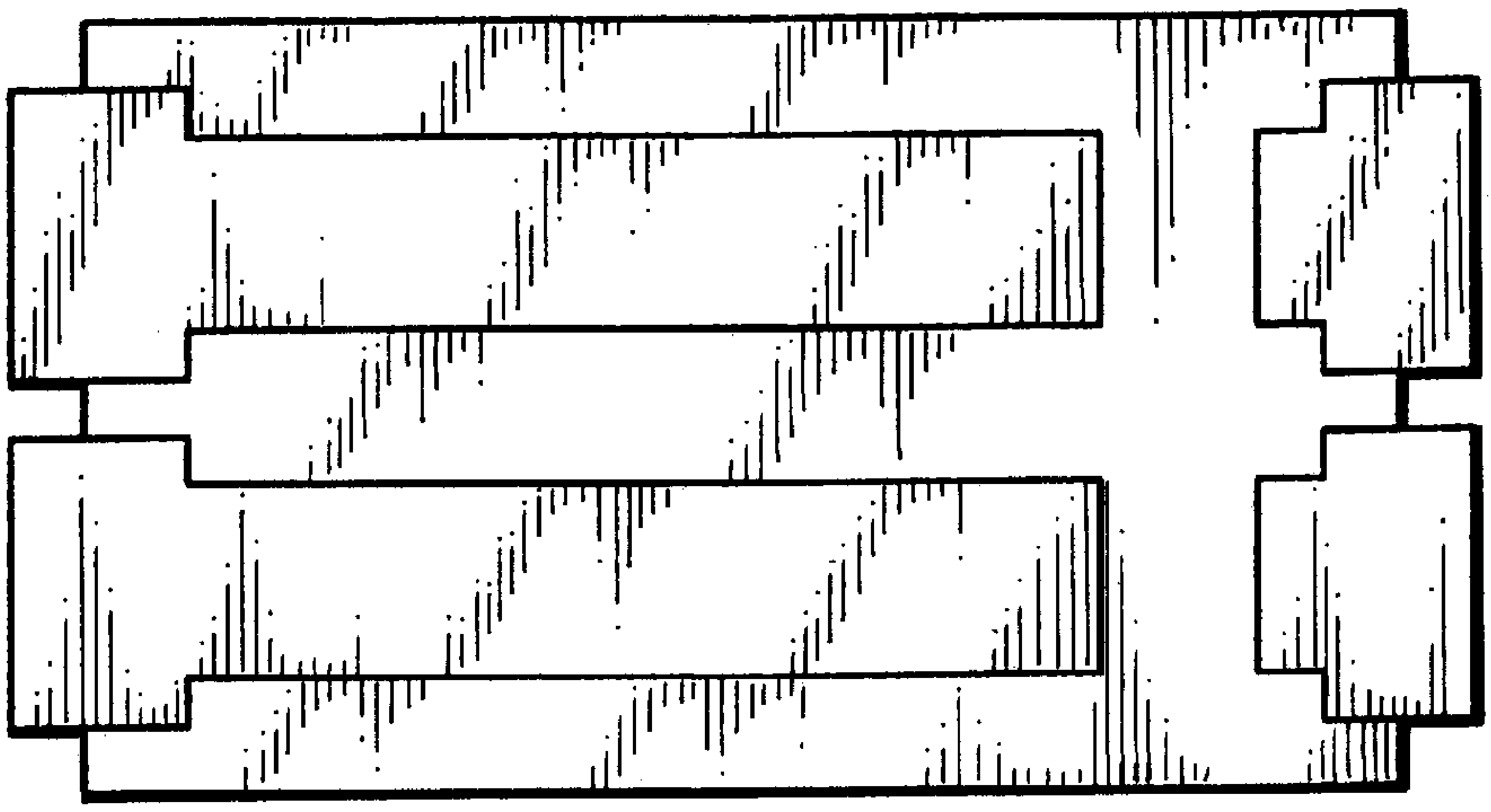


Fig.5

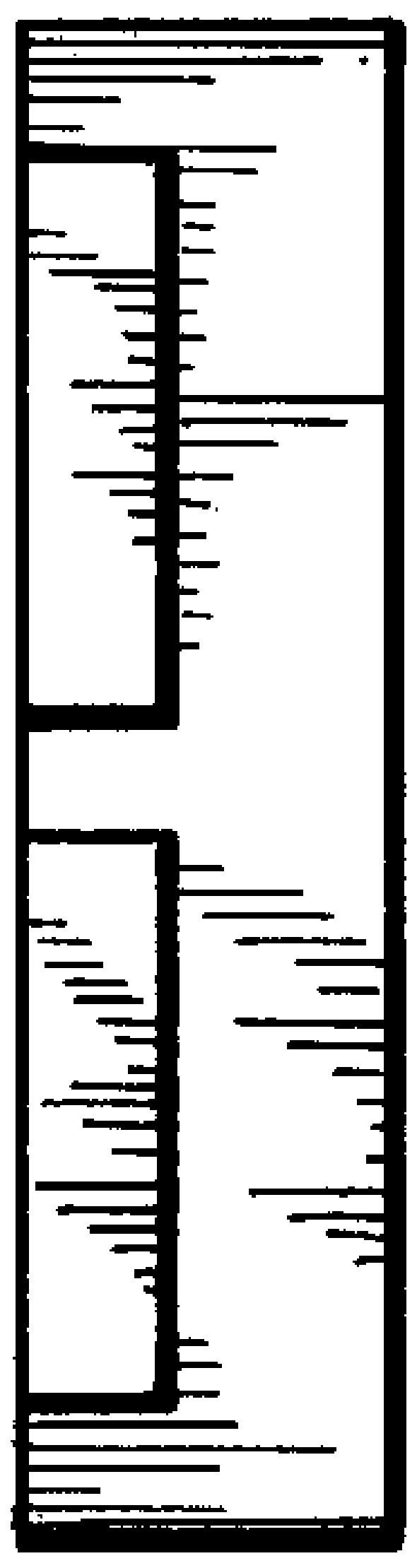


Fig.4

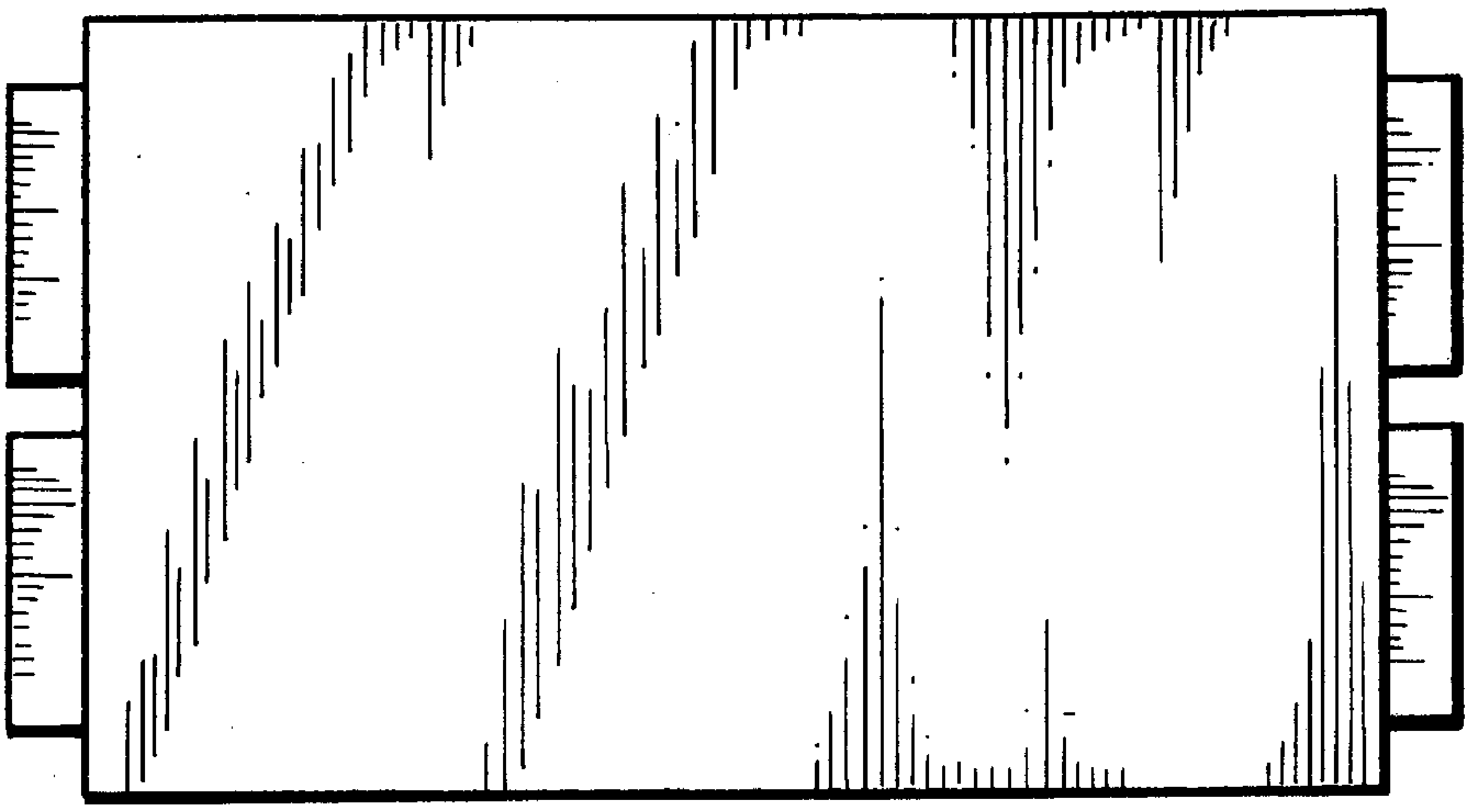


Fig.6

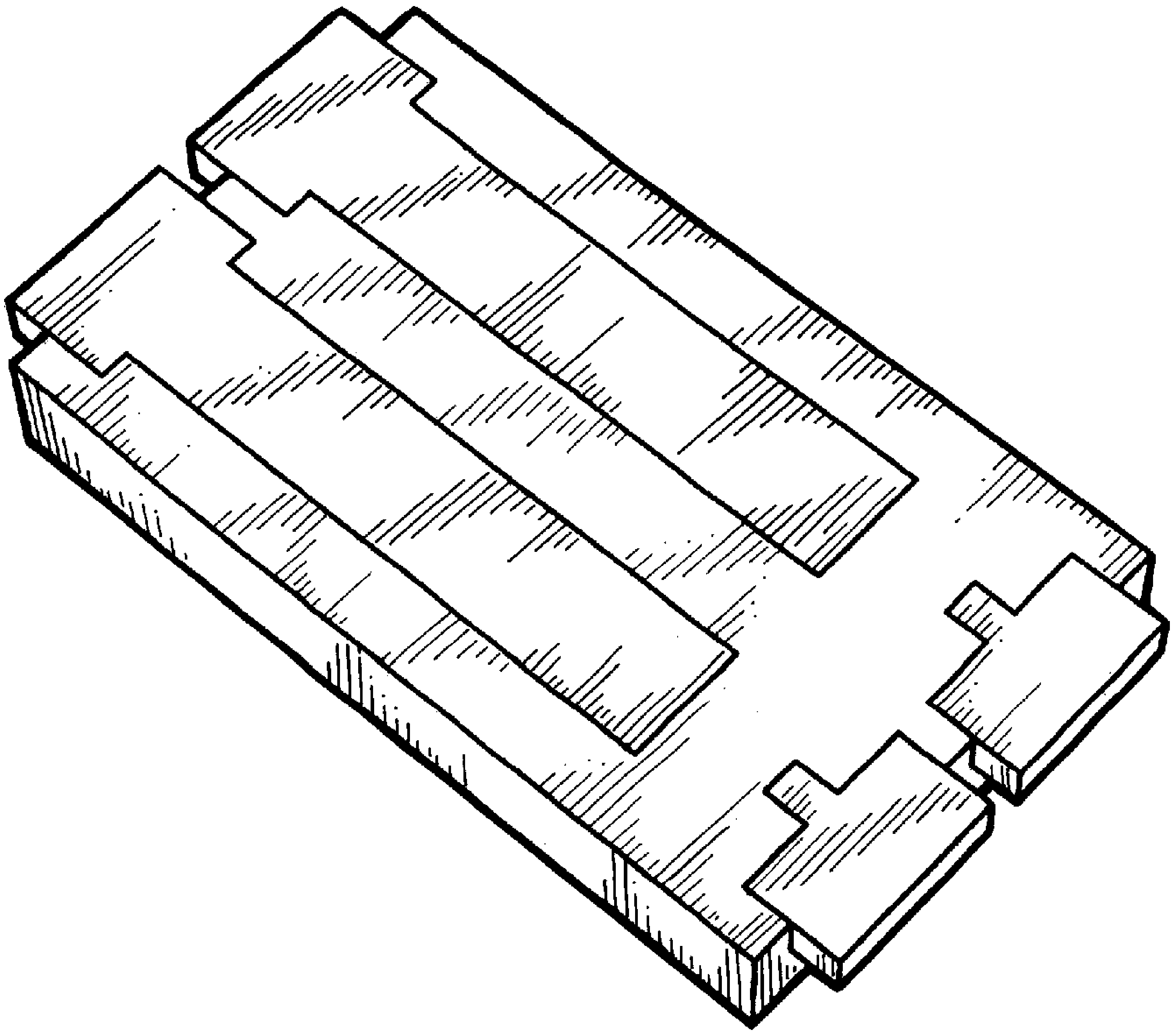


Fig.7

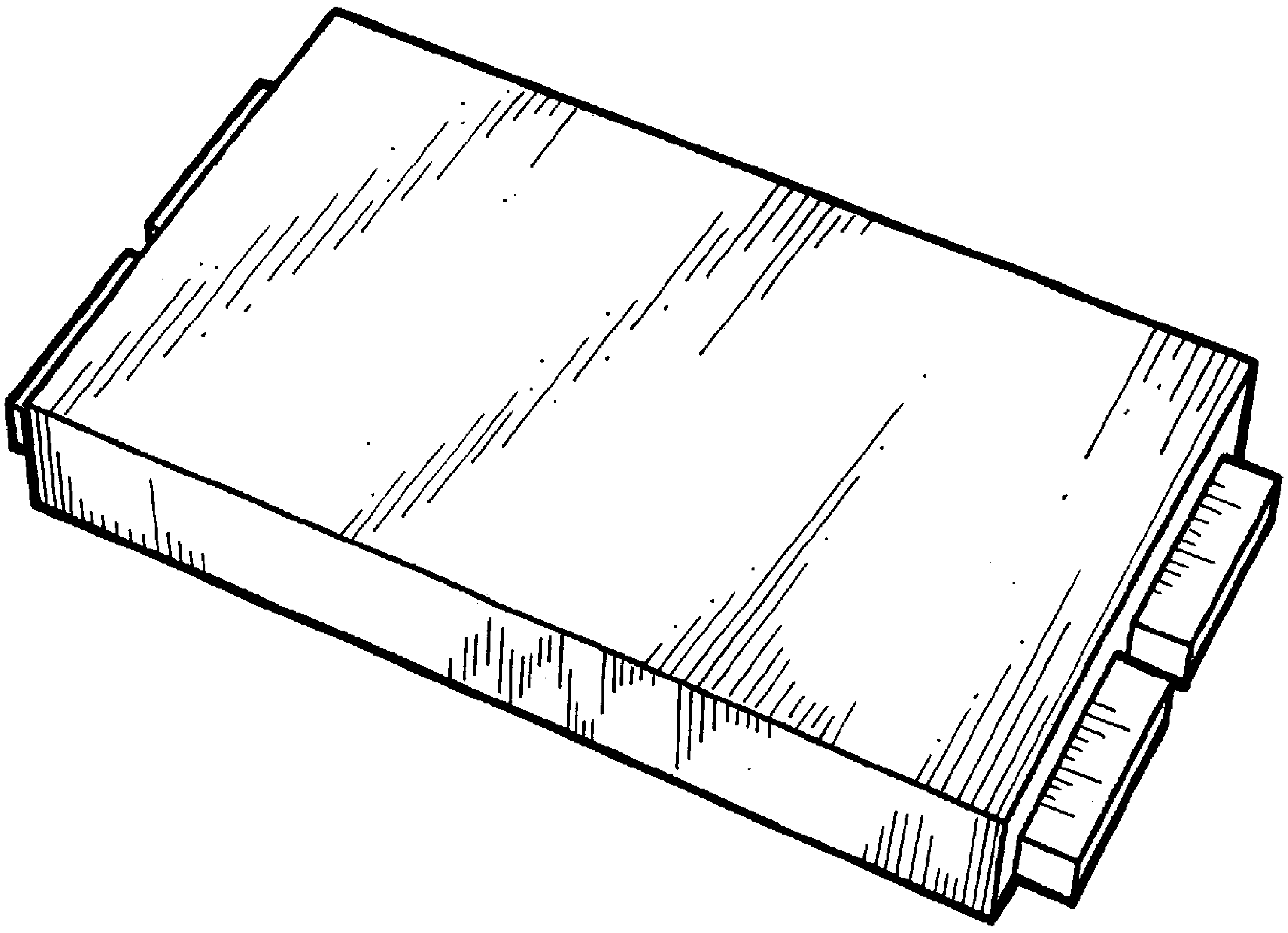


Fig.8

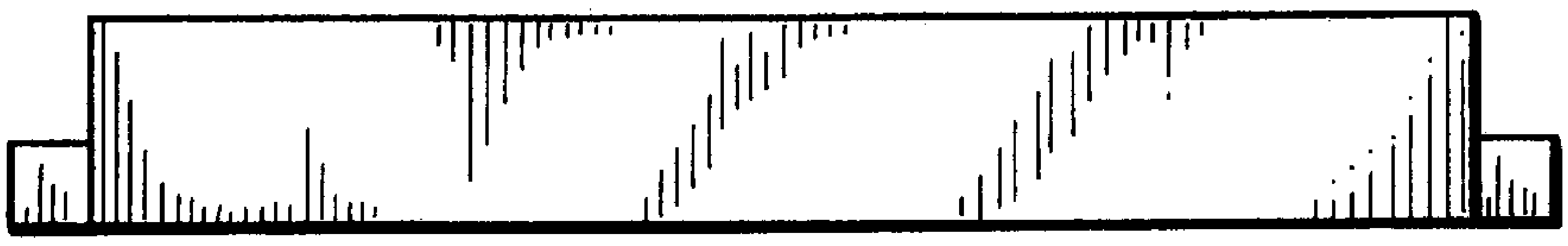
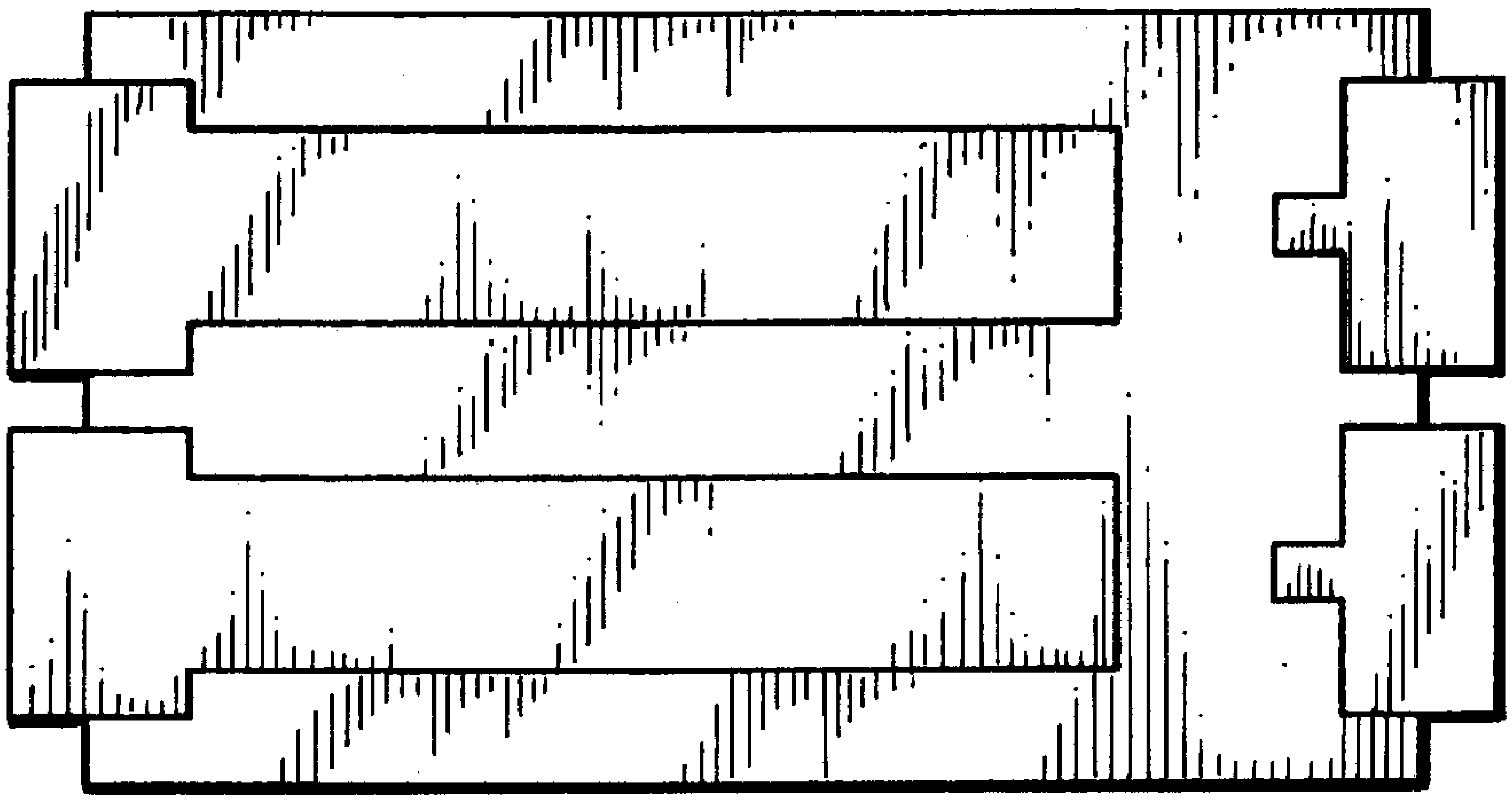


Fig.9



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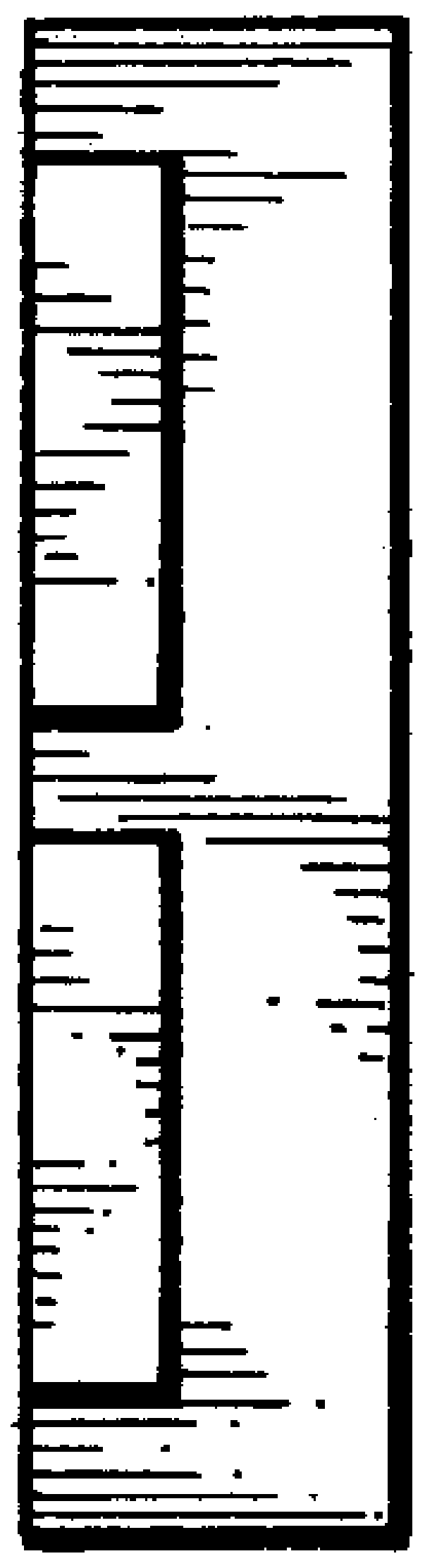

Fig.10

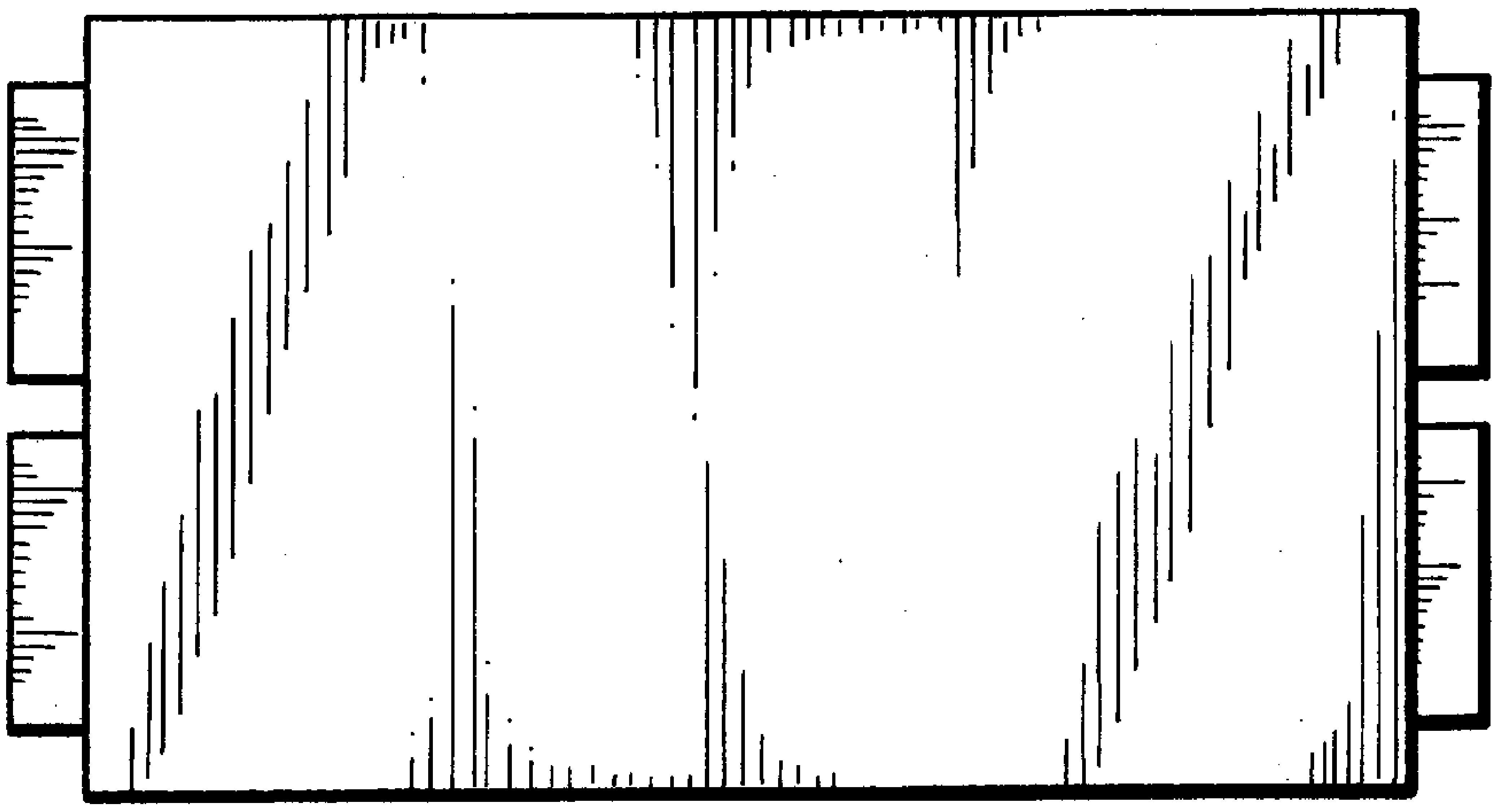

Fig.12