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(12) **United States Design Patent**
Michii

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(45) **Date of Patent:** **** Jun. 17, 2003**

(54) **INTEGRATED CIRCUITS SUBSTRATE**

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JP 11-40745 2/1999

(**) Term: **14 Years**

* cited by examiner

(21) Appl. No.: **29/165,700**

Primary Examiner—Ted Shooman

(22) Filed: **Aug. 16, 2002**

Assistant Examiner—Selina Sikder

(30) **Foreign Application Priority Data**

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(57) **CLAIM**

(51) **LOC (7) Cl.** **13-03**

The ornamental design for an integrated circuits substrate, as
shown and described.

(52) **U.S. Cl.** **D13/182**

DESCRIPTION

(58) **Field of Search** D13/182; 174/52.2,
174/52.4; 257/666, 667, 676, 686, 690,
692, 696, 705, 712, 735; 361/742, 777,
813

FIG. 1 is a front, top and right side perspective view of an
integrated circuits substrate, showing my new design;
FIG. 2 is a front elevational view thereof, the rear elevational
view is omitted as that is symmetrical to the front elevational
view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a right side elevational view thereof;
FIG. 6 is a left side elevational view thereof; and,
FIG. 7 is an enlarged cross-sectional view thereof, taken
along line 7—7 of FIG. 2, with the internal system omitted.
The broken lines in all views are shown for illustrative
purposes only and form no part of the claimed design.

(56) **References Cited**

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1 Claim, 3 Drawing Sheets

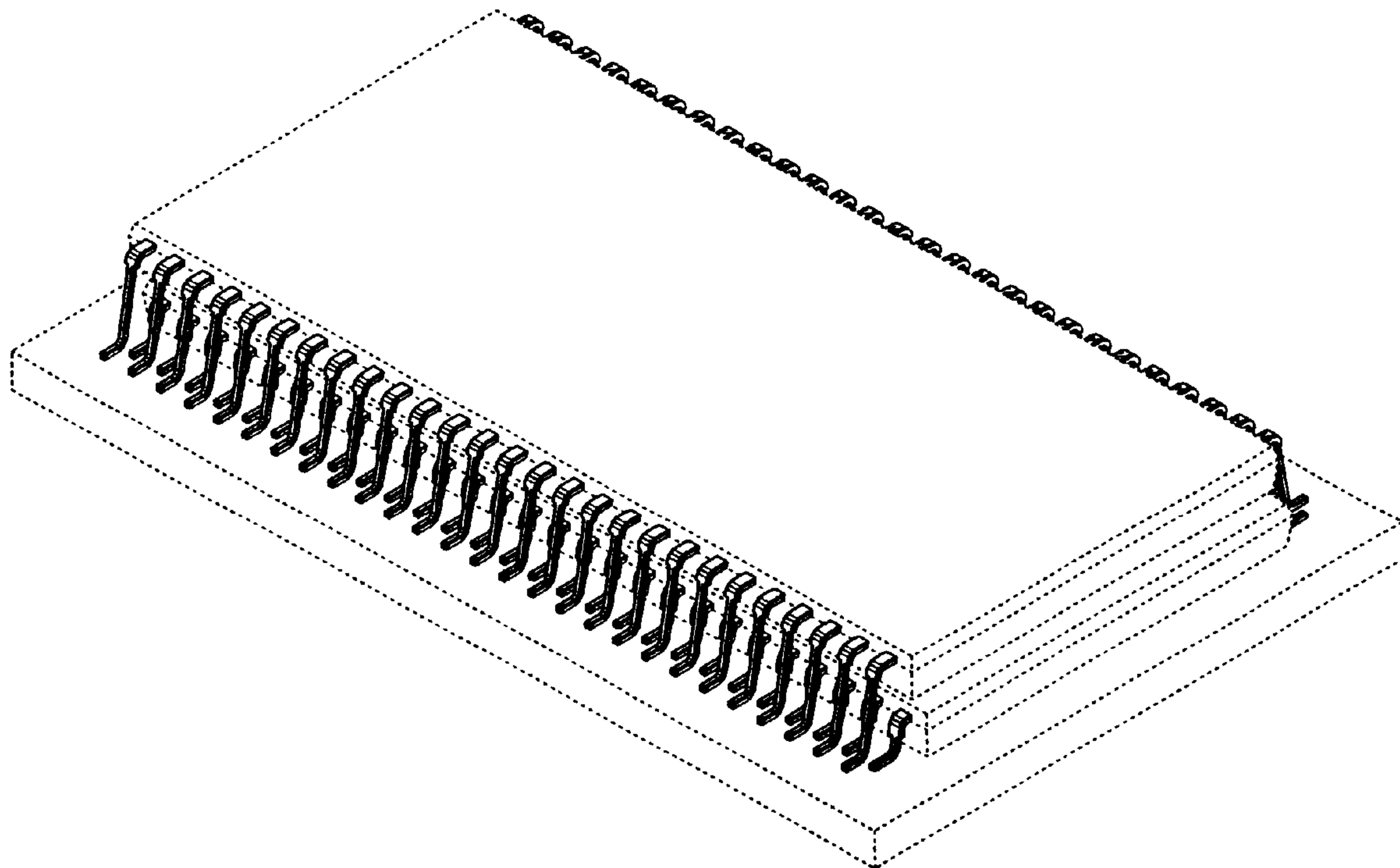


FIG. 1

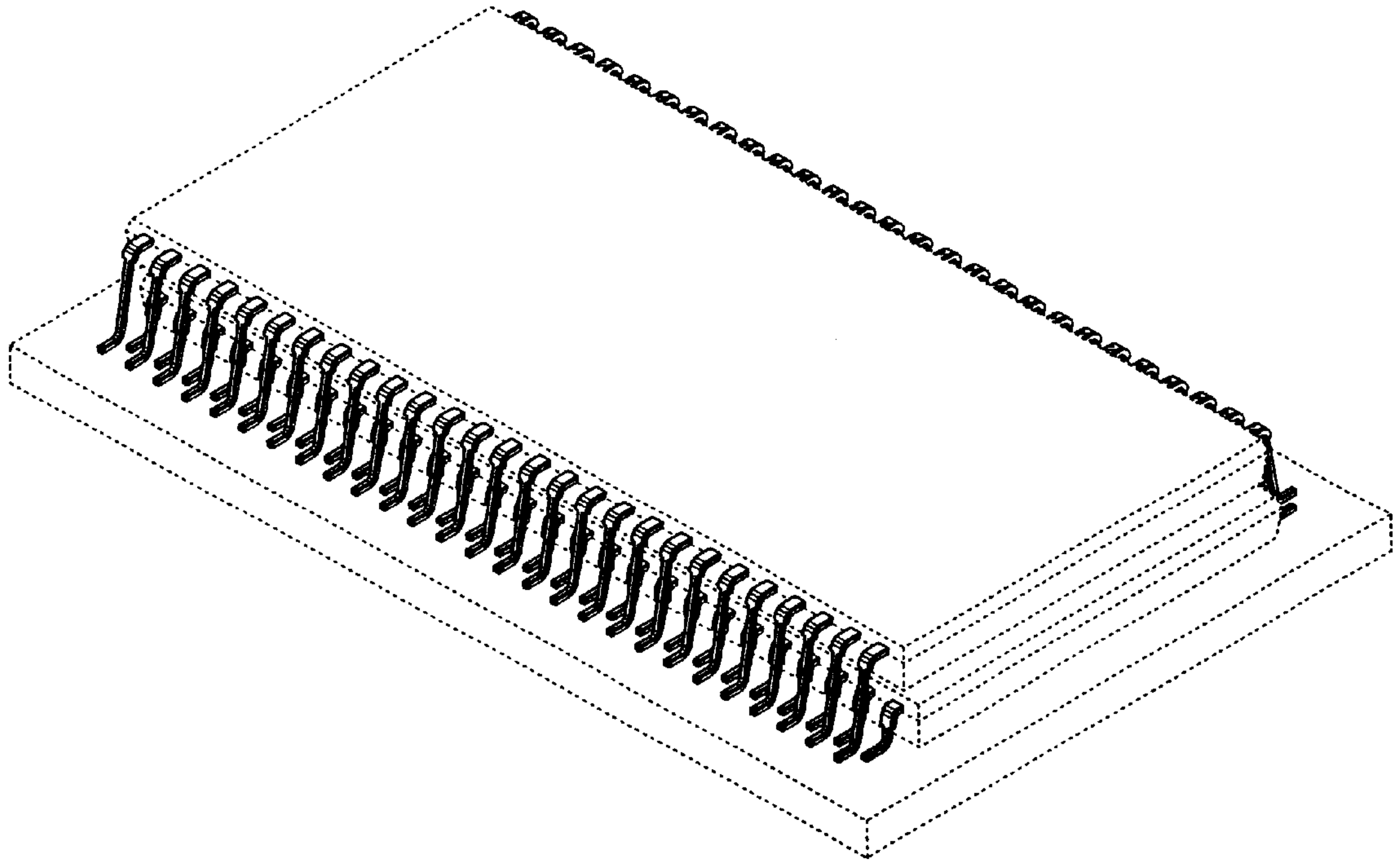


FIG. 2

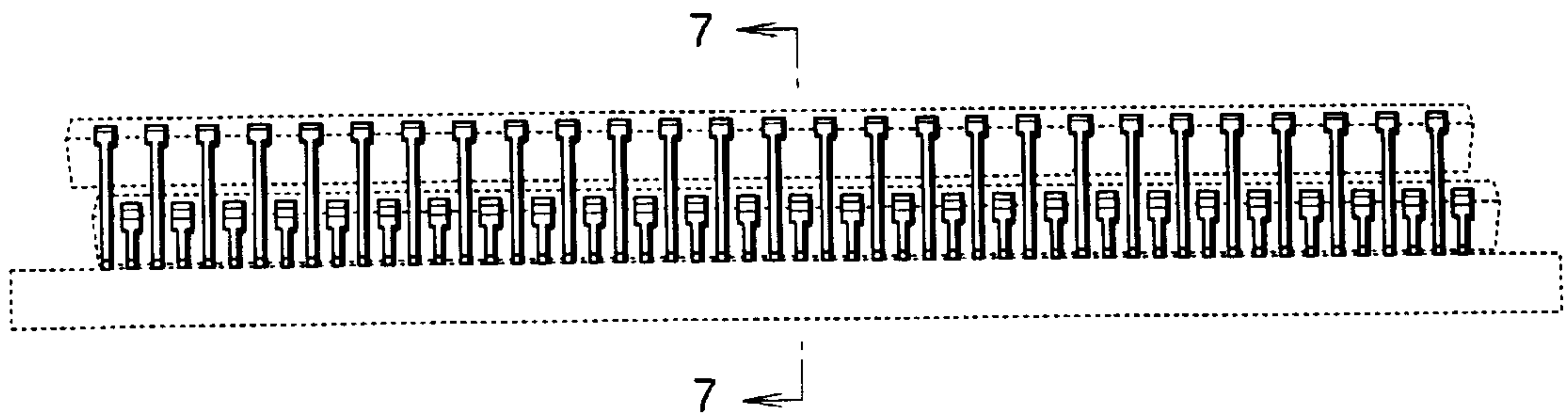


FIG.3

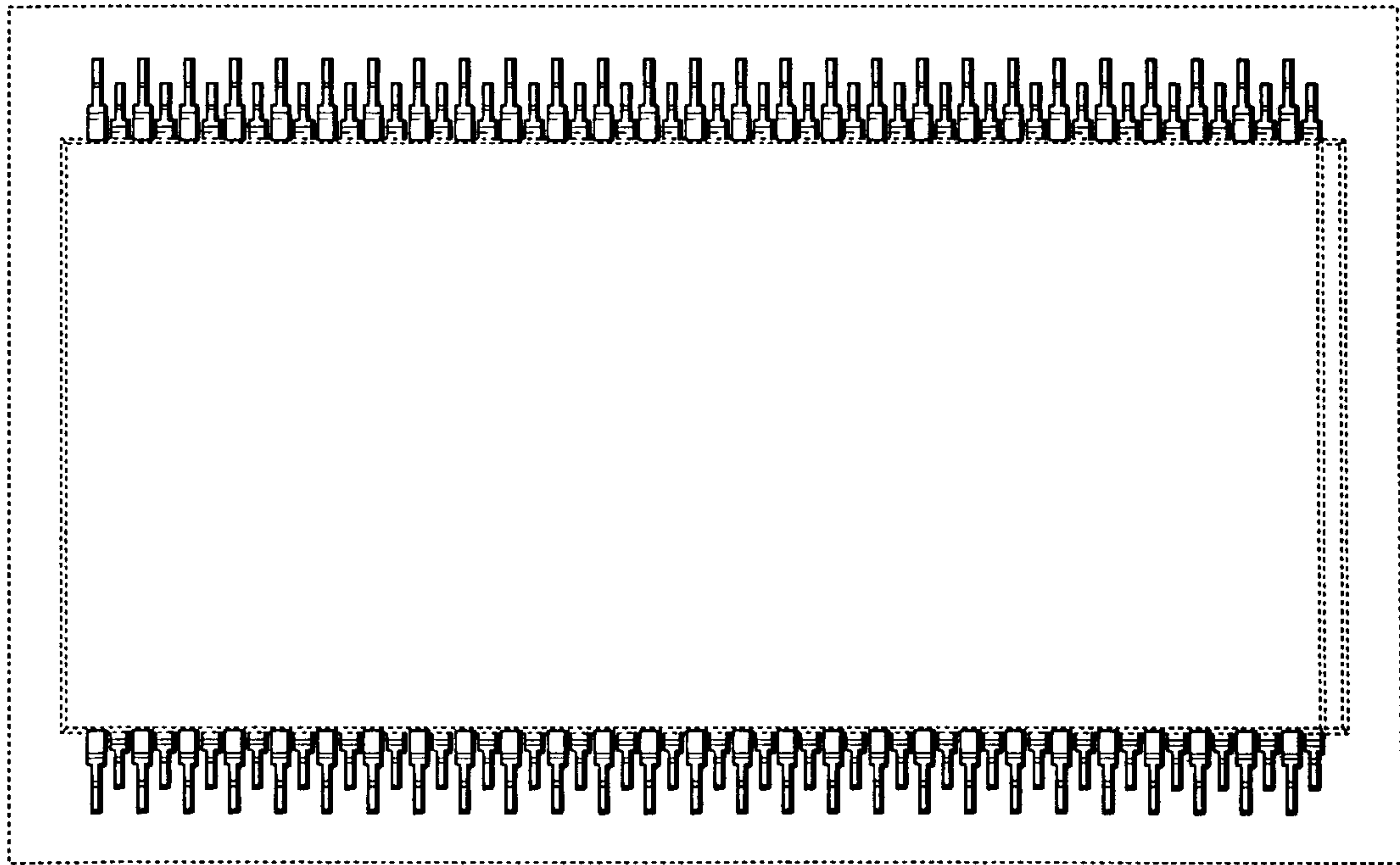


FIG.4



FIG. 5

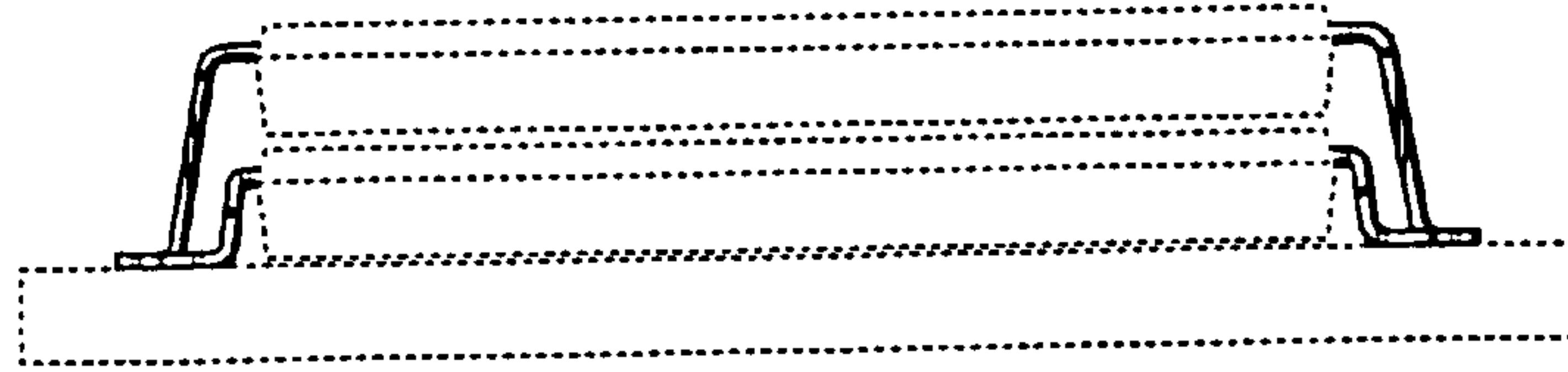


FIG. 6

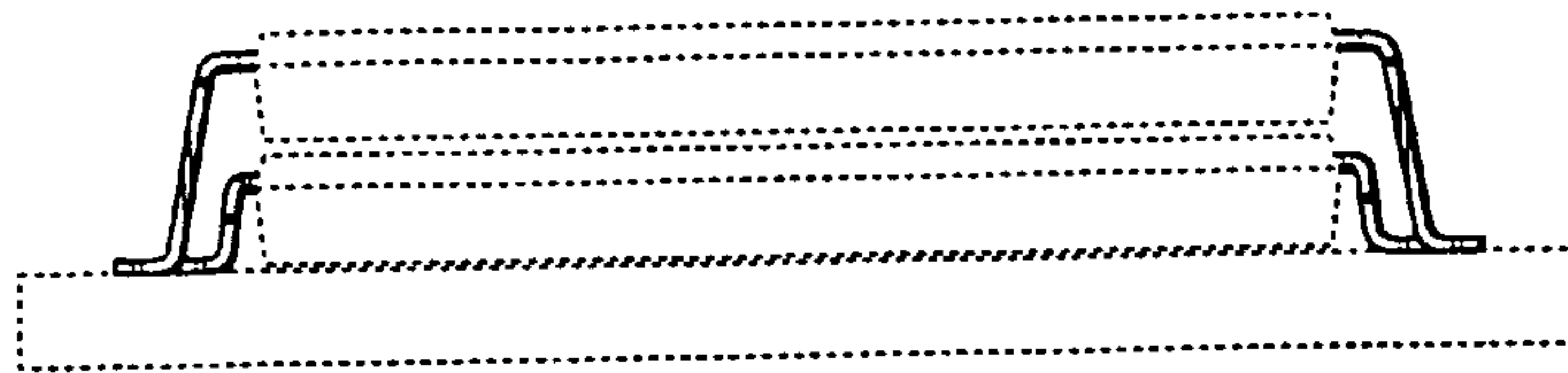


FIG. 7

