US00D473198S

(12) United States Design Patent

Ozawa et al.

(10) Patent No.: US D473,198 S
(45) Date of Patent: ** Apr. 15, 2003

(54) **SEMICONDUCTOR DEVICE**

(75) Inventors: **Isao Ozawa**, Chigasaki (JP); **Toshitsune Iijima**, Tama (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/159,669**

(22) Filed: **Apr. 26, 2002**

(30) **Foreign Application Priority Data**

Oct. 26, 2001 (JP) 2001-031432

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 174/52.1, 174/52.4; 257/666, 678, 688, 690, 691, 692, 696, 697, 703, 777, 778, 779, 780; 361/679, 728, 748, 761

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,602,271	A	*	7/1986	Dougherty, Jr. et al.	257/700
D319,045	S	*	8/1991	Hasegawa et al.	D13/182
D319,629	S	*	9/1991	Hasegawa et al.	D13/182
D319,814	S	*	9/1991	Hasegawa et al.	D13/182
D442,150	S	*	5/2001	Kang	D13/182
6,300,685	B1	*	10/2001	Hasegawa et al.	257/780
6,307,269	B1	*	10/2001	Akiyama et al.	257/778
D457,146	S	*	5/2002	Yamamoto et al.	D13/182

FOREIGN PATENT DOCUMENTS

JP	900345-5	8/1996

OTHER PUBLICATIONS

Extract of Denpa Shimbun (newspaper) showing a flash memory (LE8BU166) of Sanyo Denki Jul. 8, 1999.*

* cited by examiner

Primary Examiner—Ted Shooman
Assistant Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a top plan view of a semiconductor device, showing our new design; a bottom plan view being a mirror image thereof;
FIG. **2** is a right side elevational view thereof; a left side elevational view being a mirror image thereof;
FIG. **3** is a front elevational view thereof; and,
FIG. **4** is a rear elevational view thereof.

1 Claim, 2 Drawing Sheets

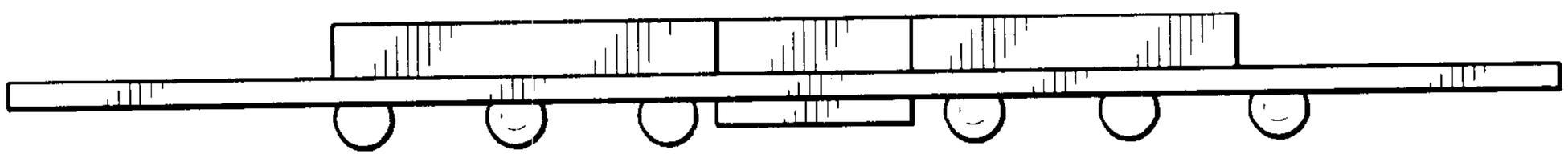

FIG. 1

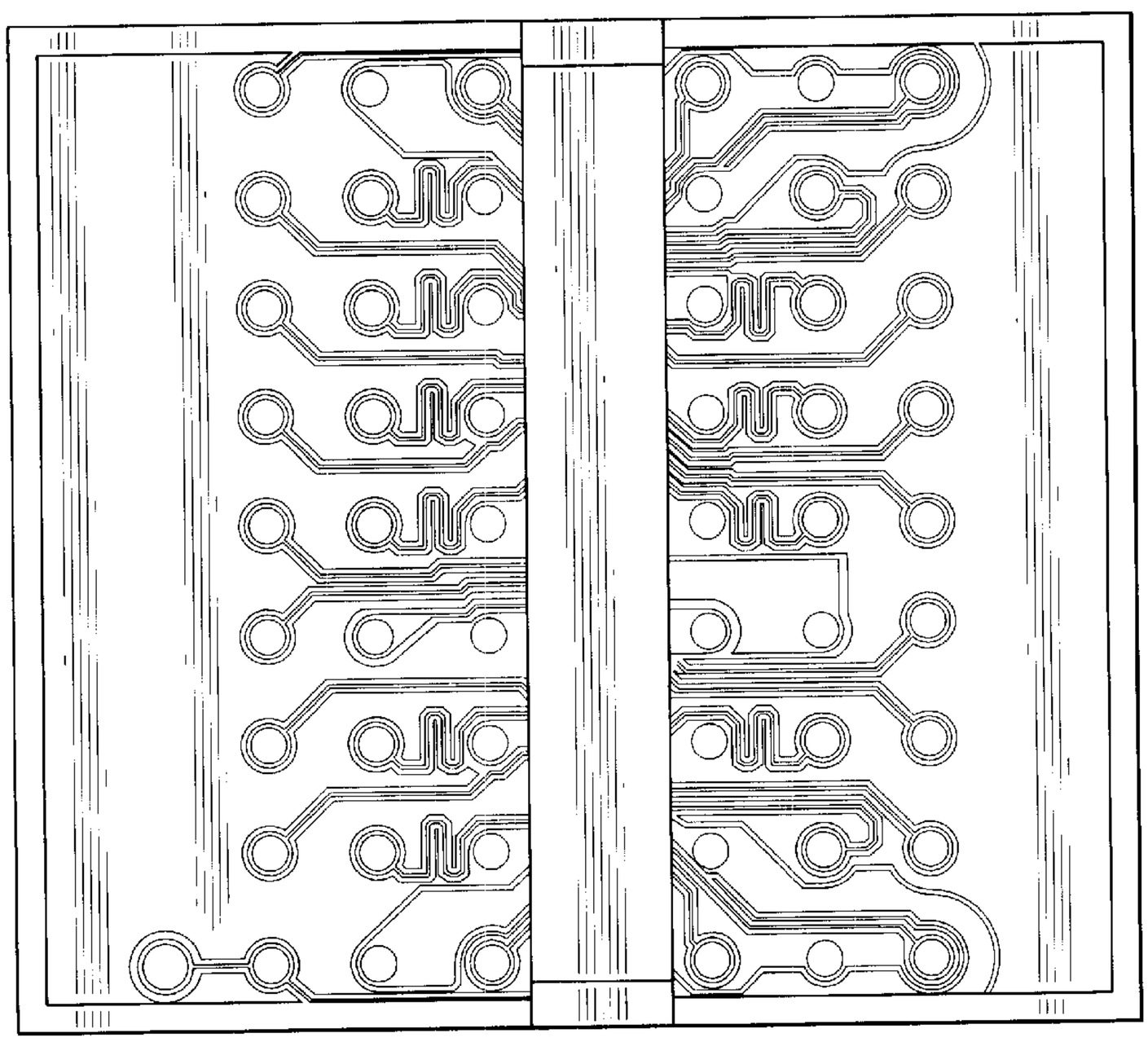

FIG. 3

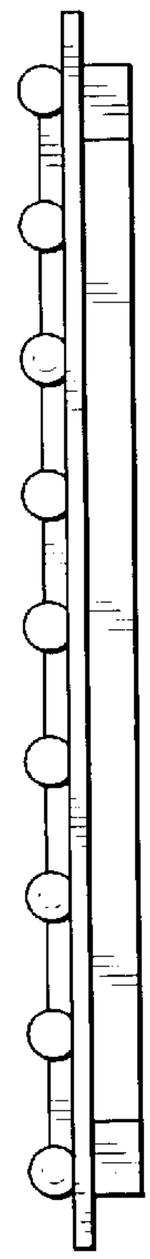

FIG. 2

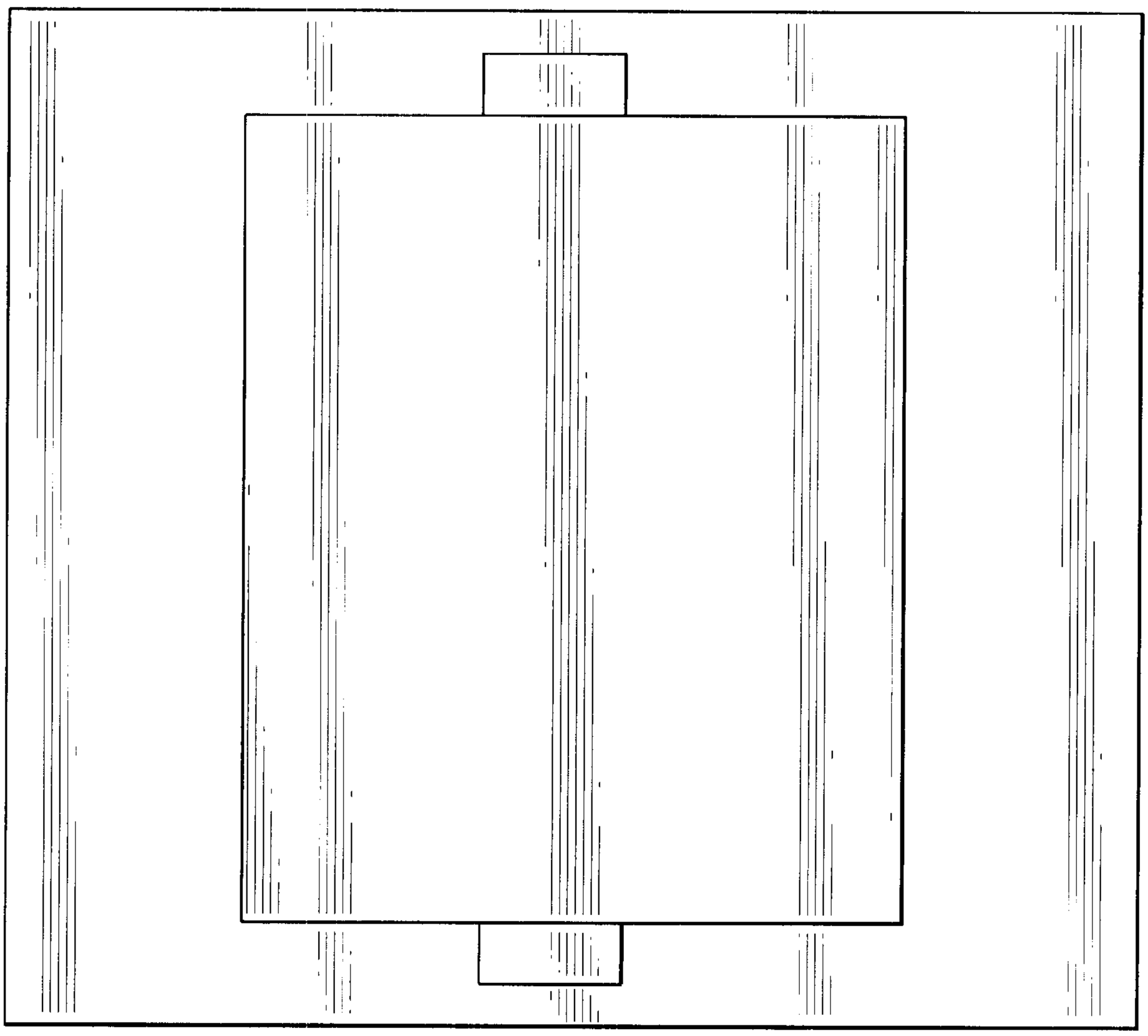

FIG. 4