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(12) **United States Design Patent**
Ebihara et al.

(10) **Patent No.:** **US D471,524 S**

(45) **Date of Patent:** **** Mar. 11, 2003**

(54) **HYBRID INTEGRATED CIRCUIT DEVICE**

(56)

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(**) Term: **14 Years**

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(21) Appl. No.: **29/158,473**

Primary Examiner—Ted Shooman

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(74) *Attorney, Agent, or Firm*—Bacon & Thomas

Related U.S. Application Data

(57) **CLAIM**

(62) Division of application No. 29/145,538, filed on Jul. 26, 2001.

The ornamental design for a hybrid integrated circuit device, as shown and described.

(30) **Foreign Application Priority Data**

DESCRIPTION

Apr. 27, 2001 (JP) 2001-016231

FIG. 1 is a perspective view of a hybrid integrated circuit device showing an embodiment of our new design;

(51) **LOC (7) Cl.** **13-03**

FIG. 2 is a front elevational view thereof;

(52) **U.S. Cl.** **D13/182**

FIG. 3 is a rear elevational view thereof;

(58) **Field of Search** D13/123, 133,

FIG. 4 is a left side elevational view thereof;

D13/180, 182, 184, 199; D10/46, 75; 29/829-832,

FIG. 5 is a right side elevational view thereof;

846; 174/250-251, 253-255, 260-261,

FIG. 6 is a top plan view thereof; and,

268; 216/13; 292/314; 316/718, 748, 752-753,

FIG. 7 is a bottom plan view thereof.

760, 783-784, 820; 411/500; 428/901;

470/27

1 Claim, 3 Drawing Sheets

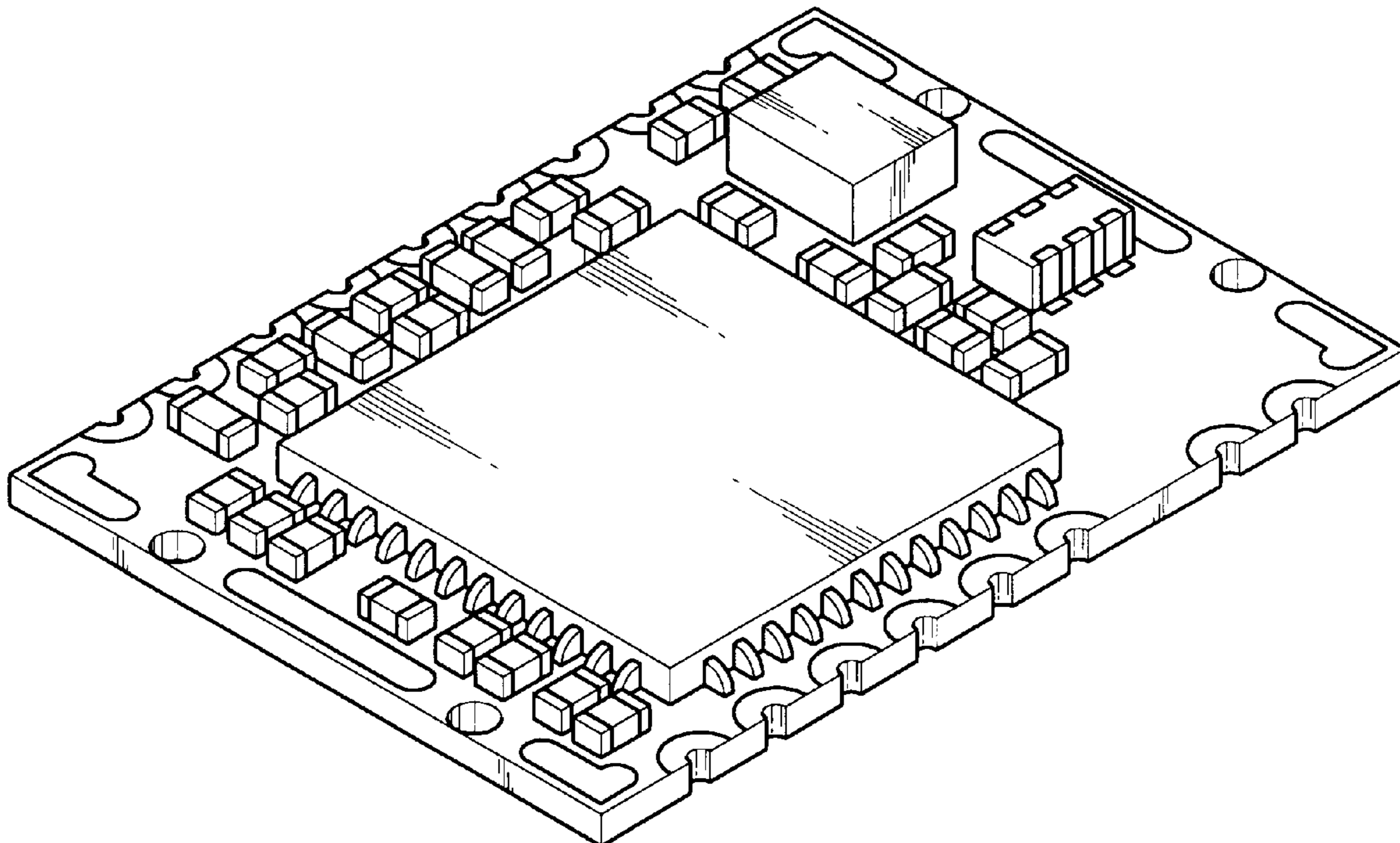


FIG. 1

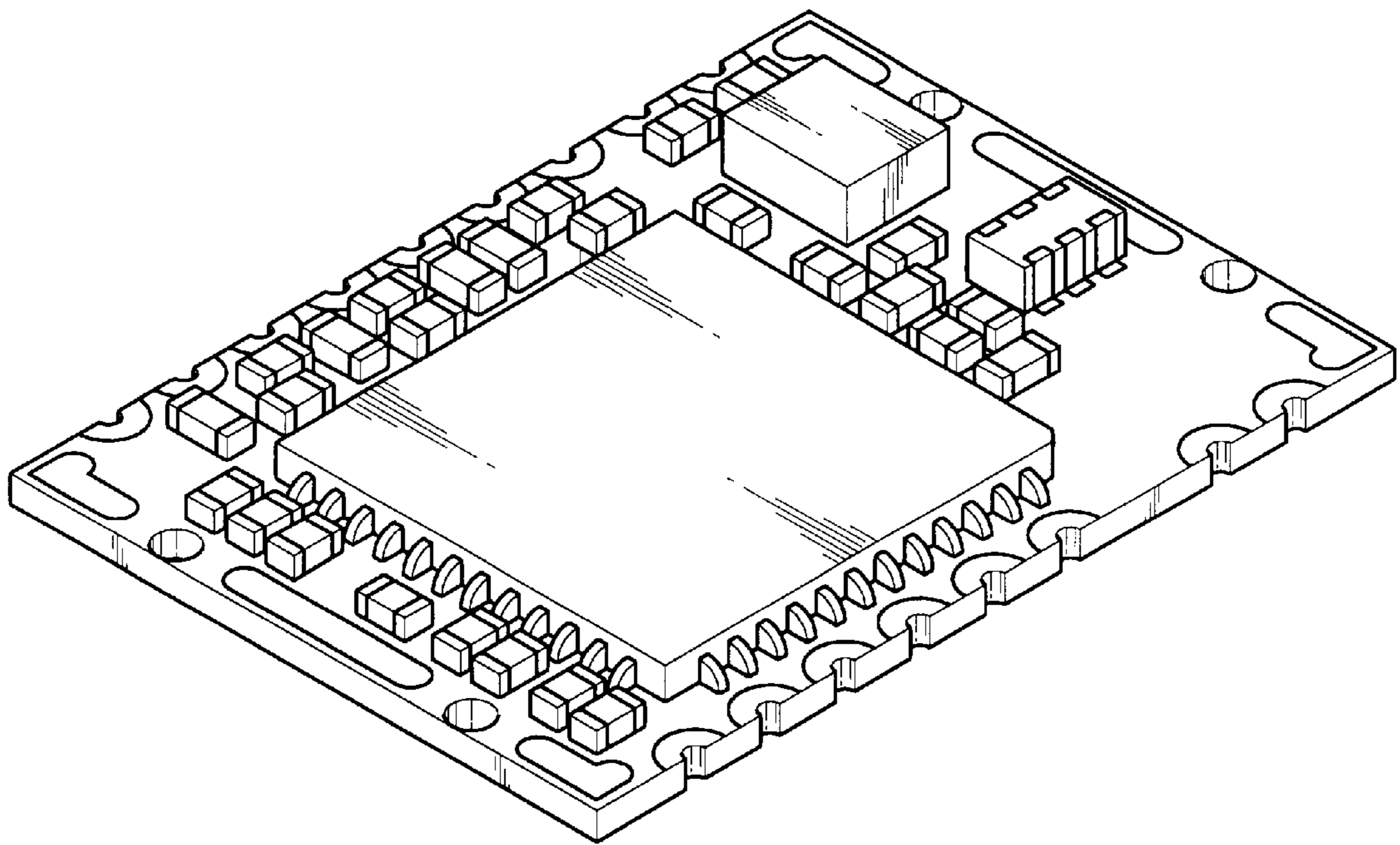


FIG. 2

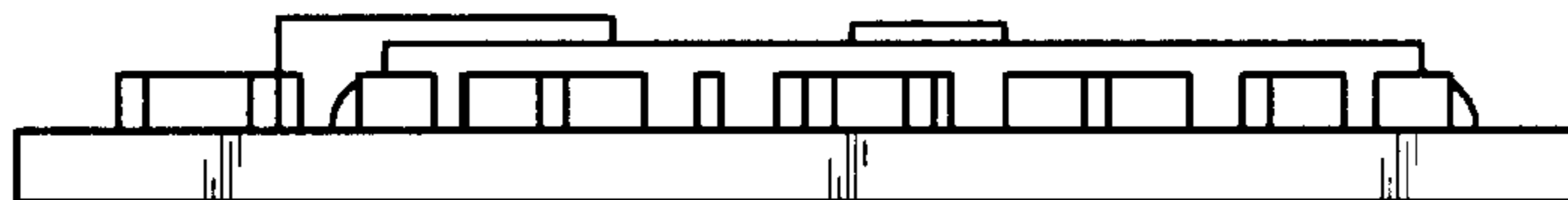


FIG. 3

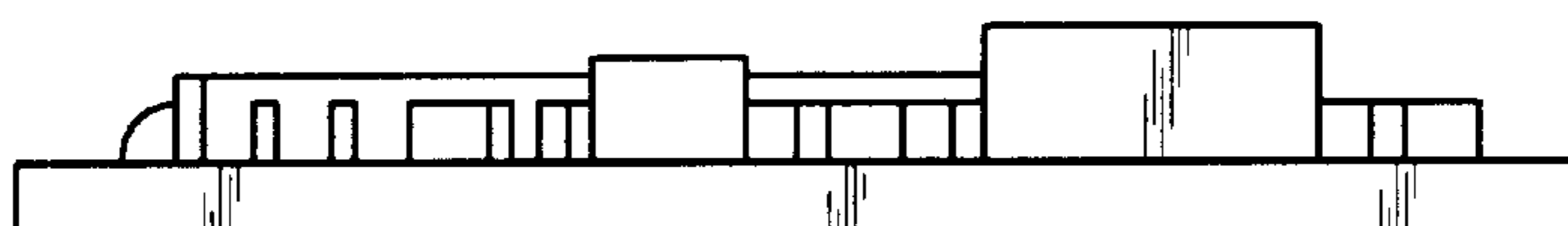


FIG. 4

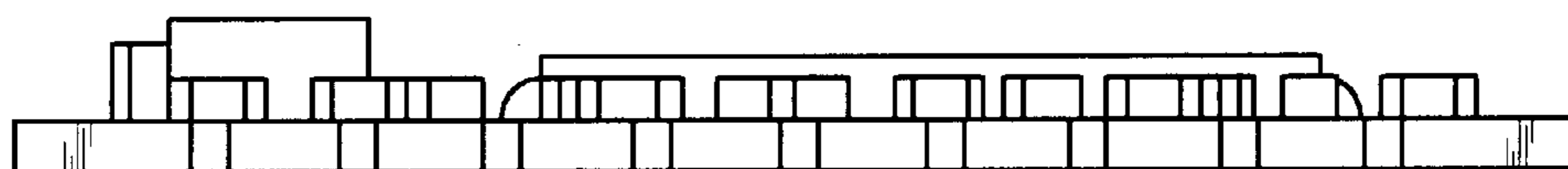


FIG. 5



FIG. 6

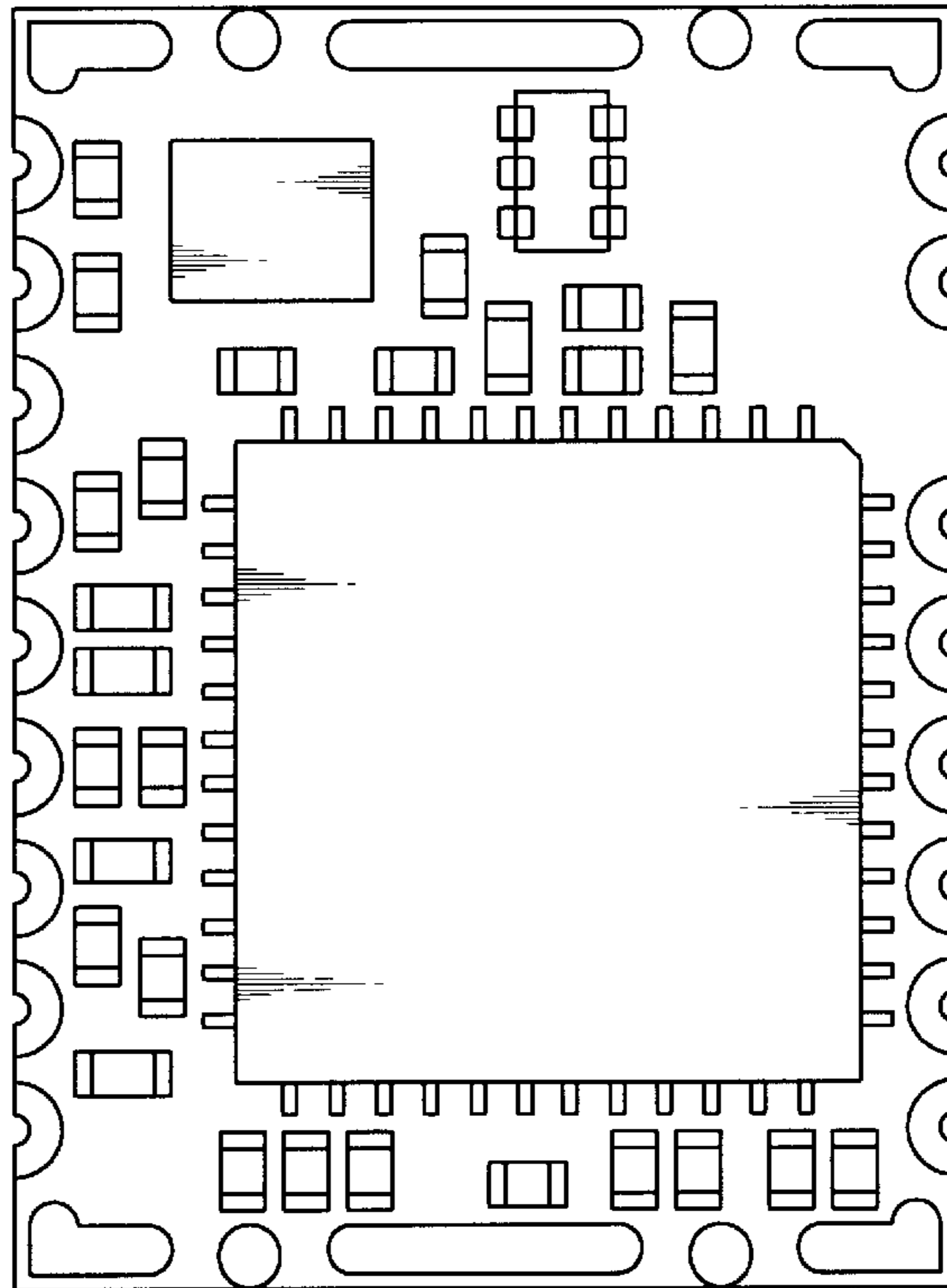


FIG. 7

