US00D470825S

(12) United States Design Patent
Iwasaki et al.

(10) **Patent No.:** **US D470,825 S**
(45) **Date of Patent:** ** **Feb. 25, 2003**

(54) **SEMICONDUCTOR DEVICE**

(75) Inventors: **Mitsutaka Iwasaki**, Tokyo (JP); **Toru Iwagami**, Tokyo (JP); **Hisashi Kawafuji**, Fukuoka (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/159,531**

(22) Filed: **Apr. 24, 2002**

(30) **Foreign Application Priority Data**

Dec. 28, 2001 (JP) 2001-038794
Dec. 28, 2001 (JP) 2001-038795

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182; 174/16.3, 174/52.1, 52.2, 52.4; 257/670, 672, 676, 686, 688, 690–696, 703, 787; 361/736, 742, 748, 752, 760, 761, 774, 783, 784, 785, 798, 813, 820

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,221,859 A	*	6/1993	Kobayashi et al.	257/676
D357,462 S	*	4/1995	Terasawa et al.	D13/182
D357,671 S	*	4/1995	Terasawa et al.	D13/182
D360,619 S	*	7/1995	Terasawa et al.	D13/182
D394,244 S		5/1998	Majumdar et al.	
5,757,070 A	*	5/1998	Fritz	257/675
D401,912 S		12/1998	Majumdar et al.	
5,877,548 A	*	3/1999	Washida et al.	257/690
D421,969 S	*	3/2000	Kawafuji et al.	D13/182
D448,739 S		10/2001	Iwasaki et al.	
D459,705 S	*	7/2002	Yokota et al.	D13/182

* cited by examiner

Primary Examiner—Ted Shooman
Assistant Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) CLAIM

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and right side perspective view of a semiconductor device, showing our new design;

FIG. **2** is a front, bottom and right side perspective view thereof;

FIG. **3** is a front elevational view thereof;

FIG. **4** is a rear elevational view thereof;

FIG. **5** is a top plan view thereof;

FIG. **6** is a bottom plan view thereof;

FIG. **7** is a right side elevational view thereof;

FIG. **8** is a left side elevational view thereof;

FIG. **9** is a cross-sectional view thereof, taken along line **9**—**9** of FIG. **5**, with the internal system omitted;

FIG. **10** is a cross-sectional view thereof, taken along line **10**—**10** of FIG. **5**, with the internal system omitted;

FIG. **11** is a front, top and right side perspective view of a second embodiment of the semiconductor device, showing our new design;

FIG. **12** is a front, bottom and right side perspective view thereof;

FIG. **13** is a front elevational view thereof;

FIG. **14** is a rear elevational view thereof;

FIG. **15** is a top plan view thereof;

FIG. **16** is a bottom plan view thereof;

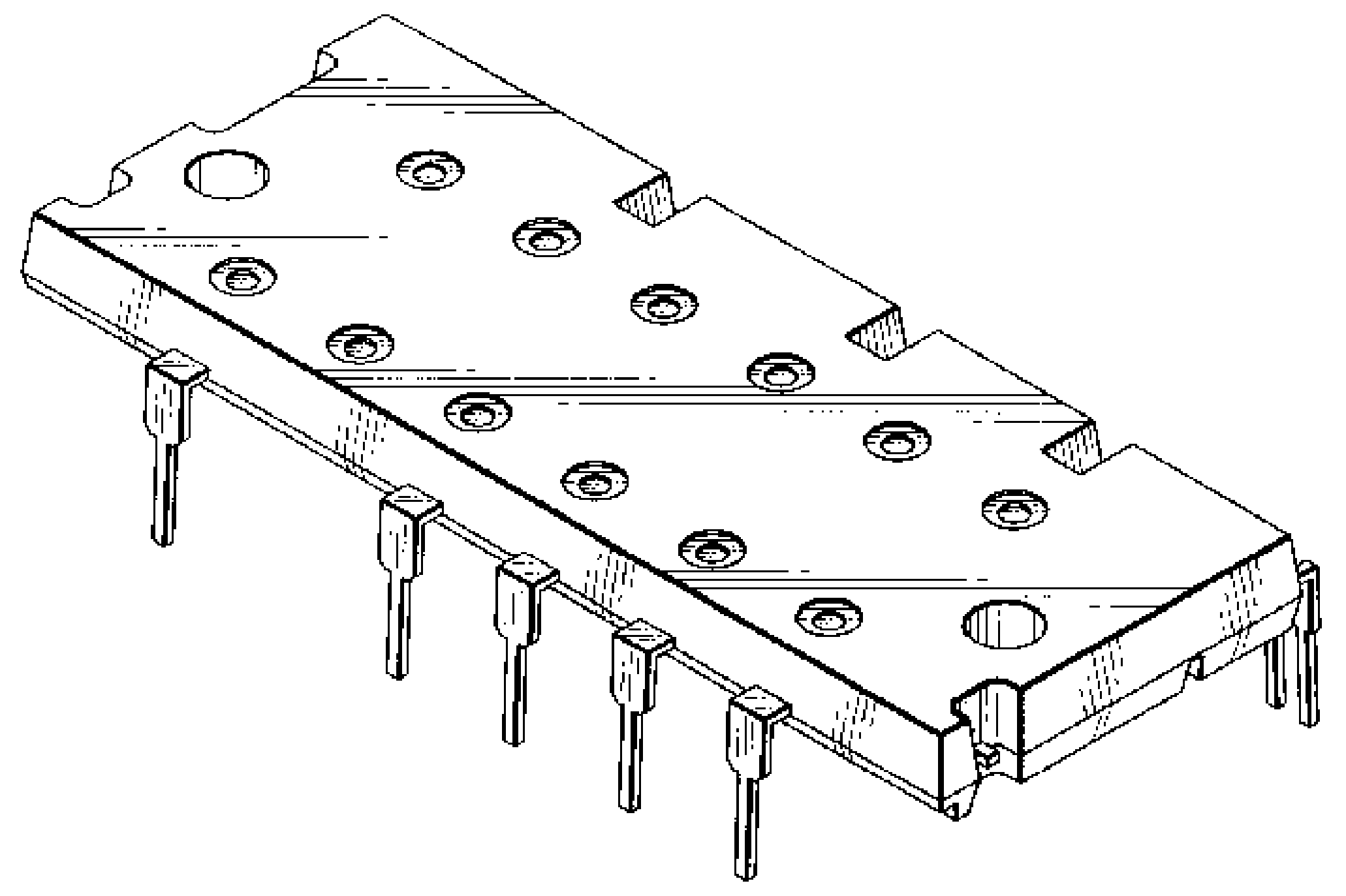
FIG. **17** is a right side elevational view thereof;

FIG. **18** is a left side elevational view thereof;

FIG. **19** is a cross-sectional view thereof, taken along line **19**—**19** of FIG. **15**, with the internal system omitted; and,

FIG. **20** is a cross-sectional view thereof, taken along line **20**—**20** of FIG. **15**, with the internal system omitted.

1 Claim, 6 Drawing Sheets



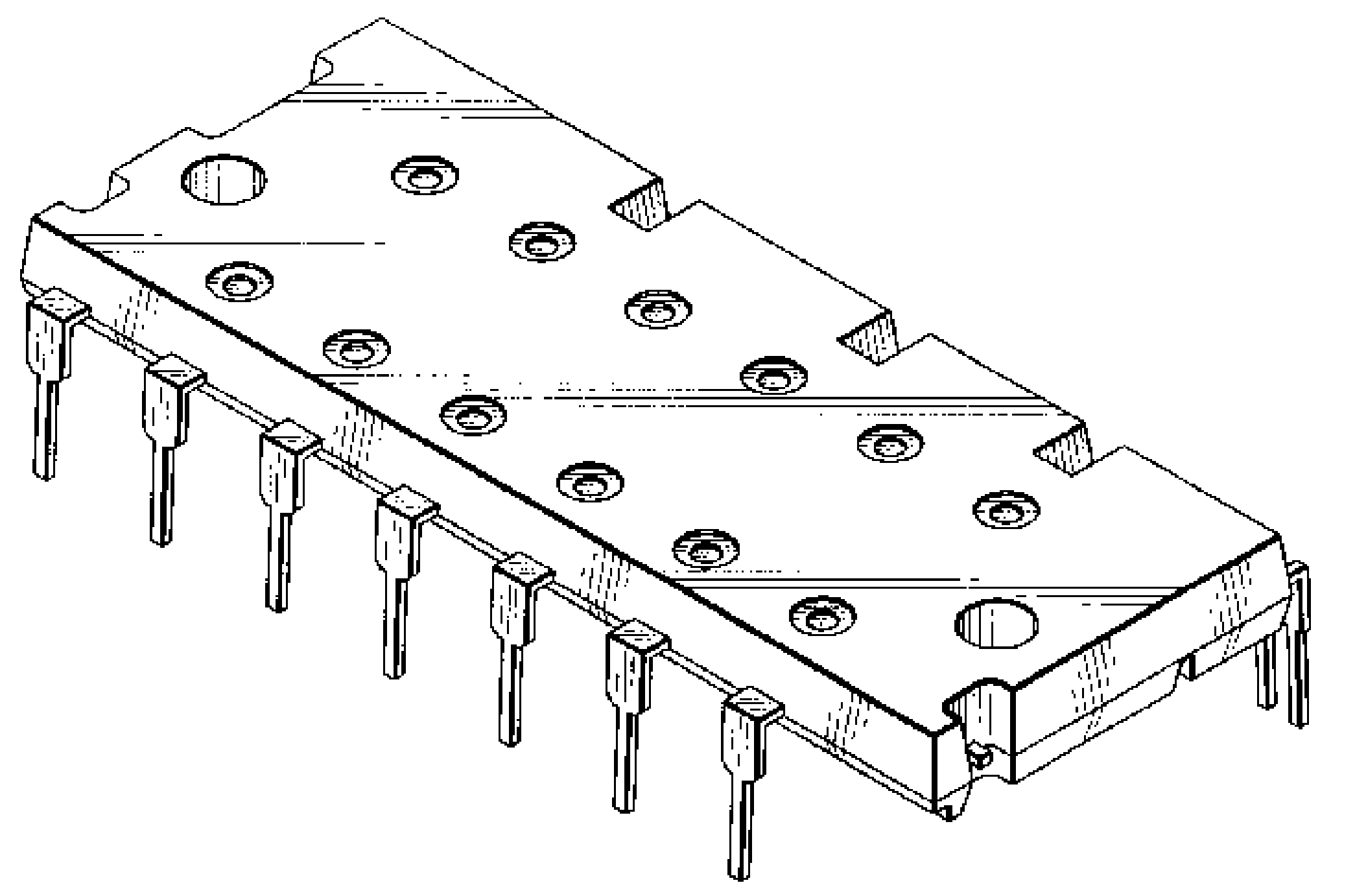


FIG.1

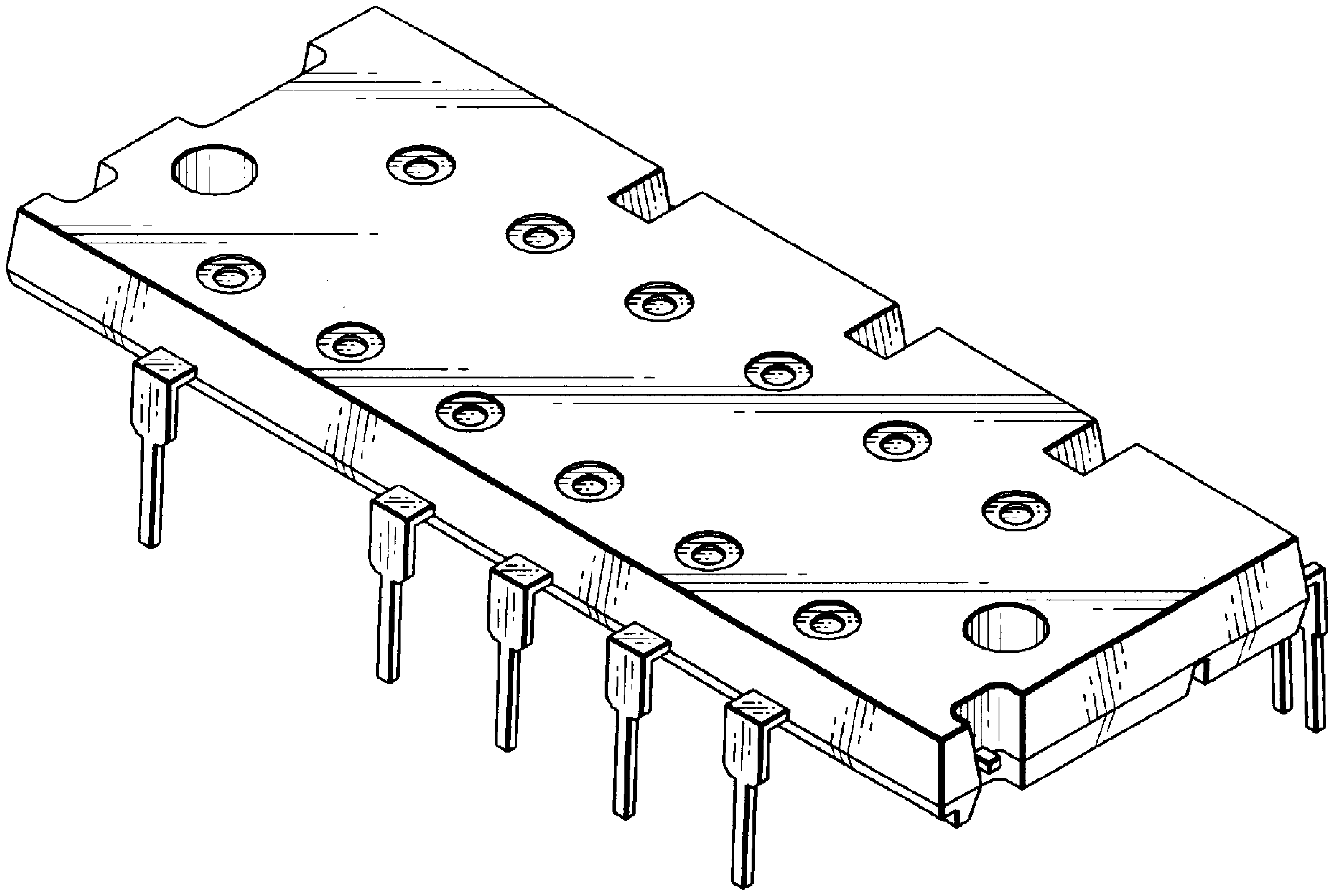


FIG.2

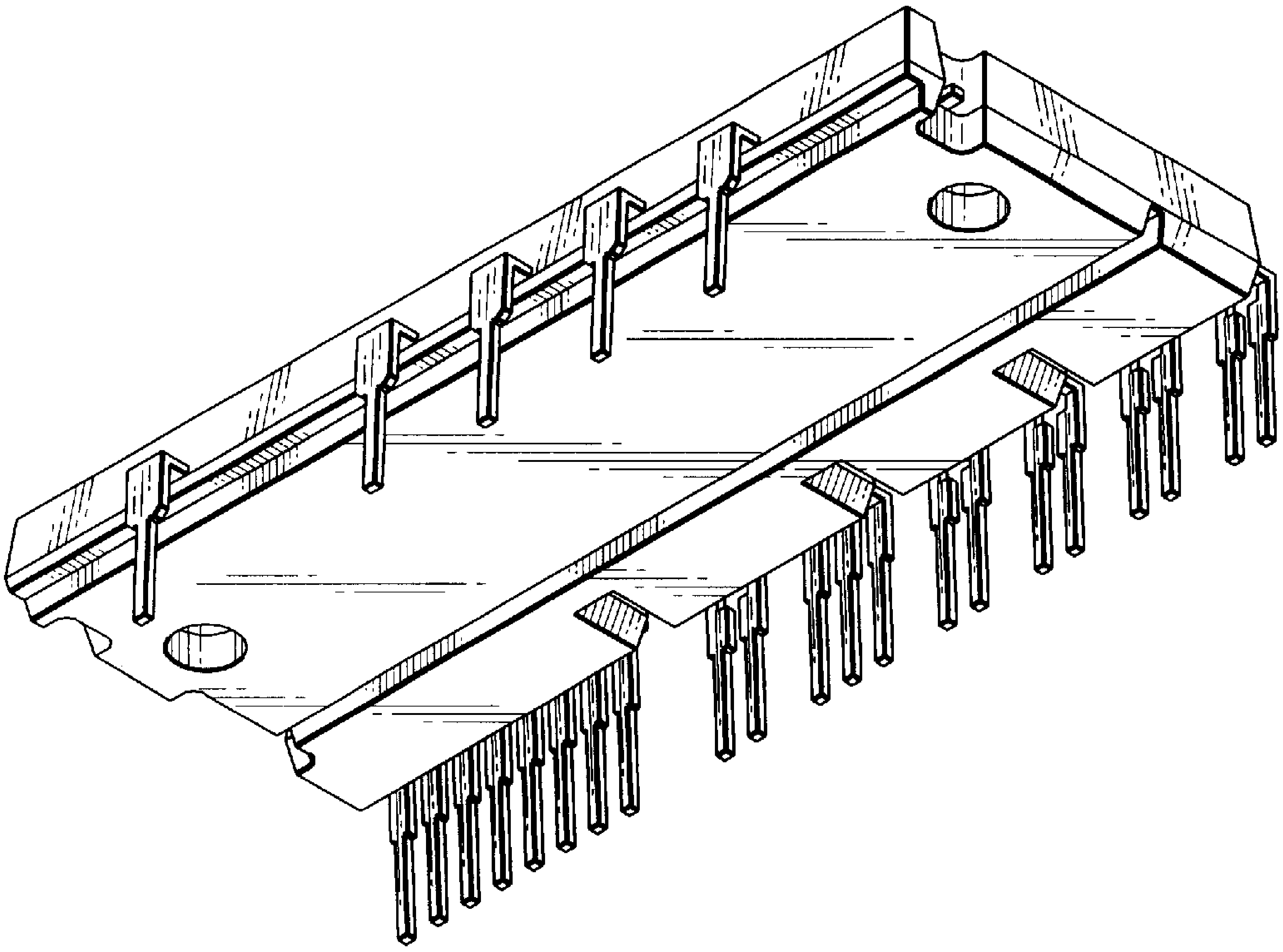


FIG.3

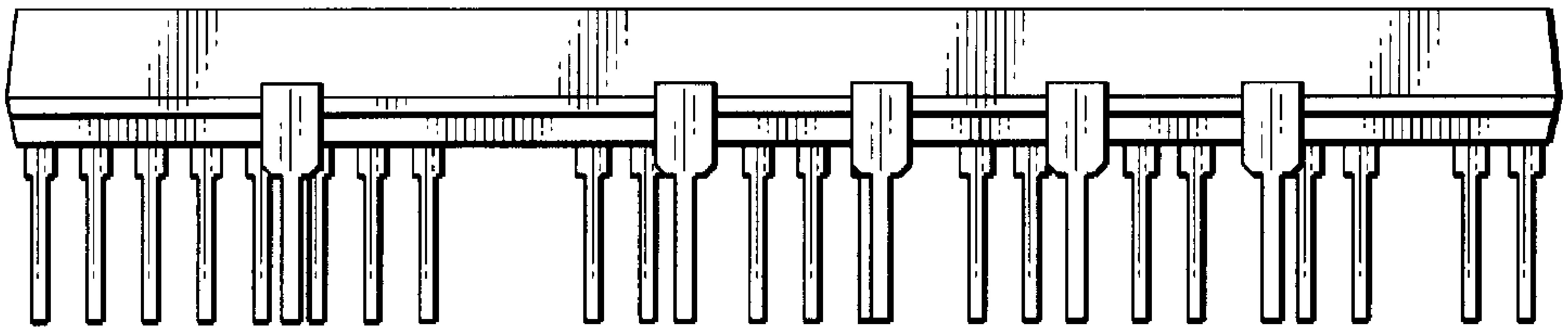


FIG.4

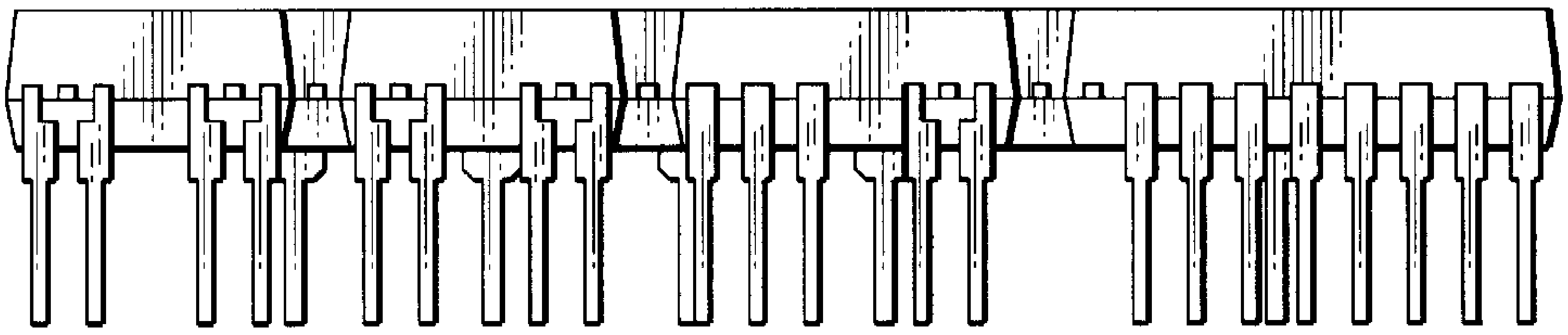


FIG.5

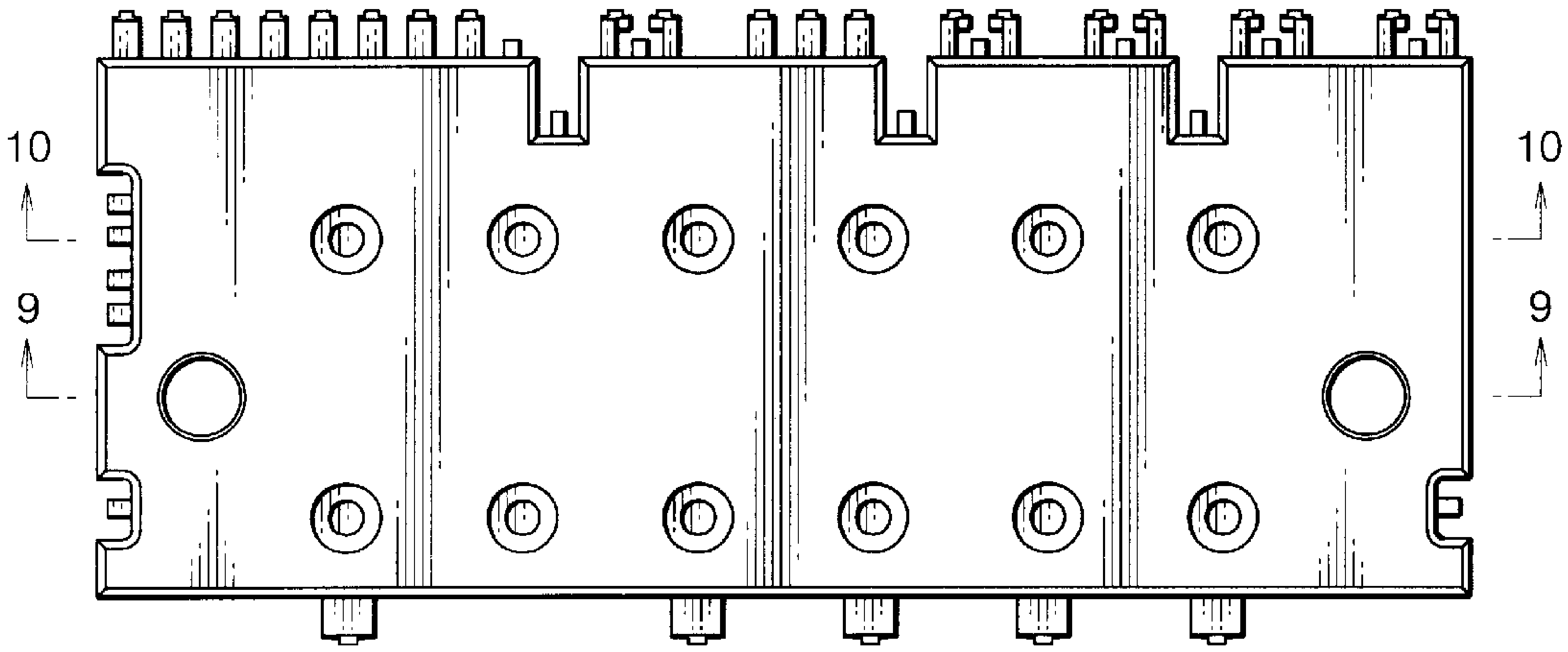


FIG.6

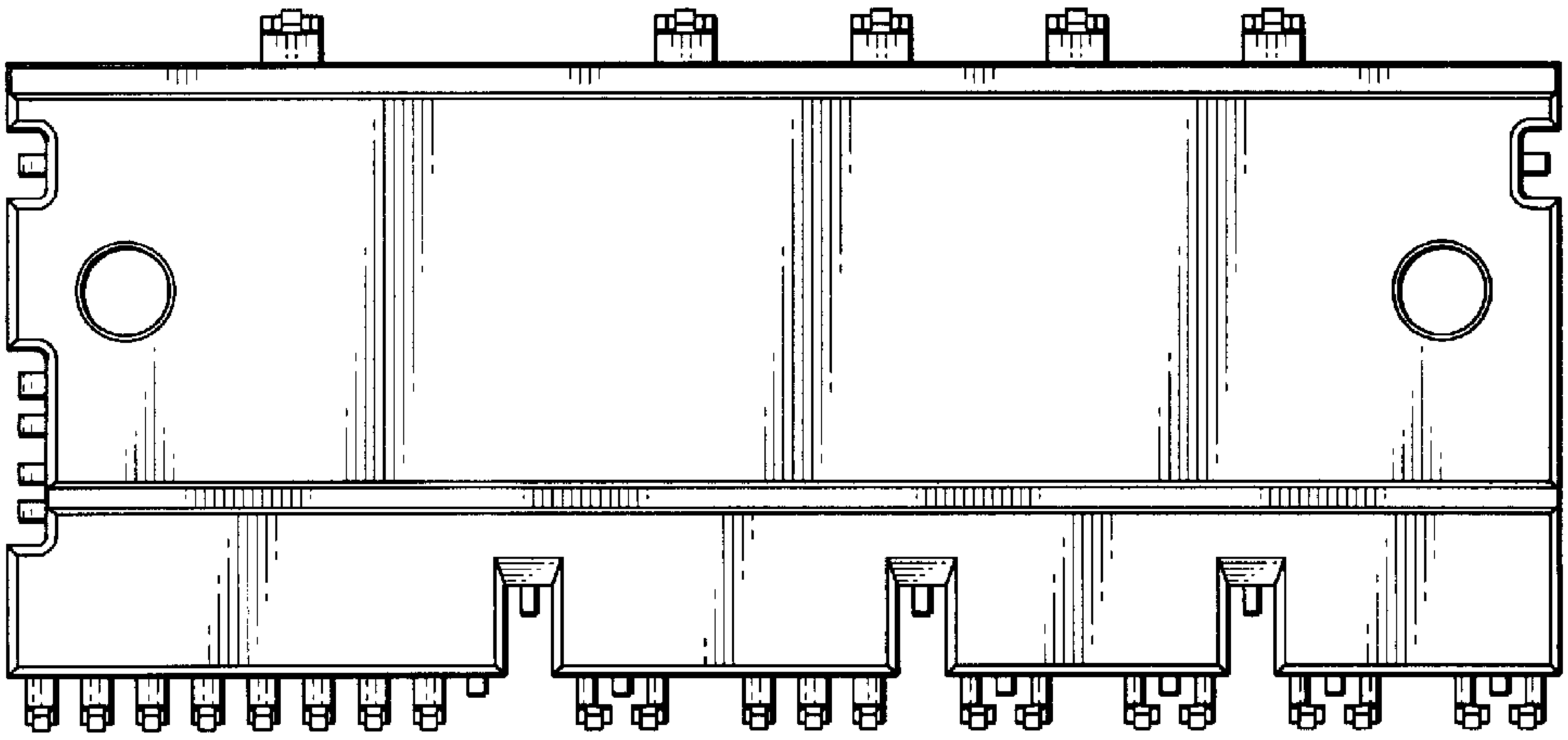


FIG.7

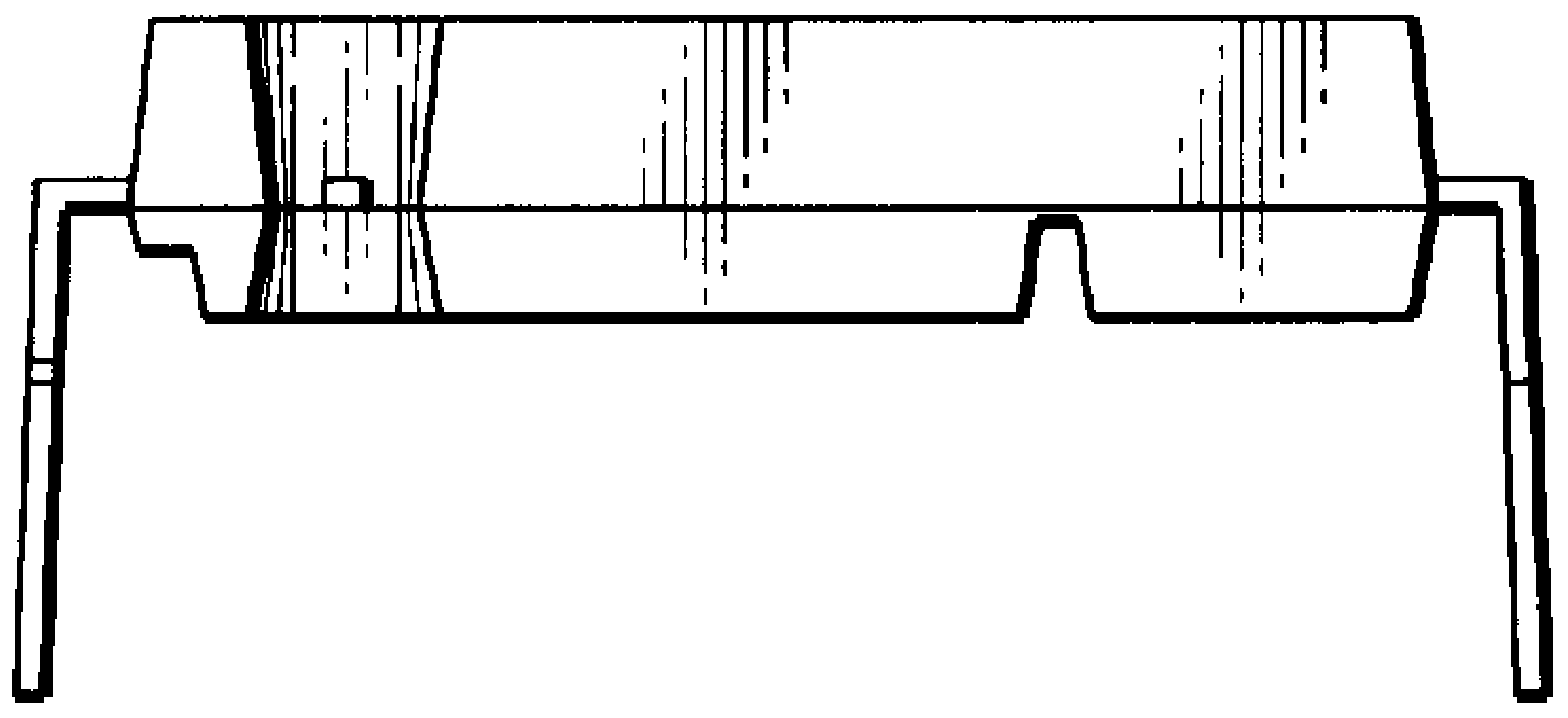


FIG.8

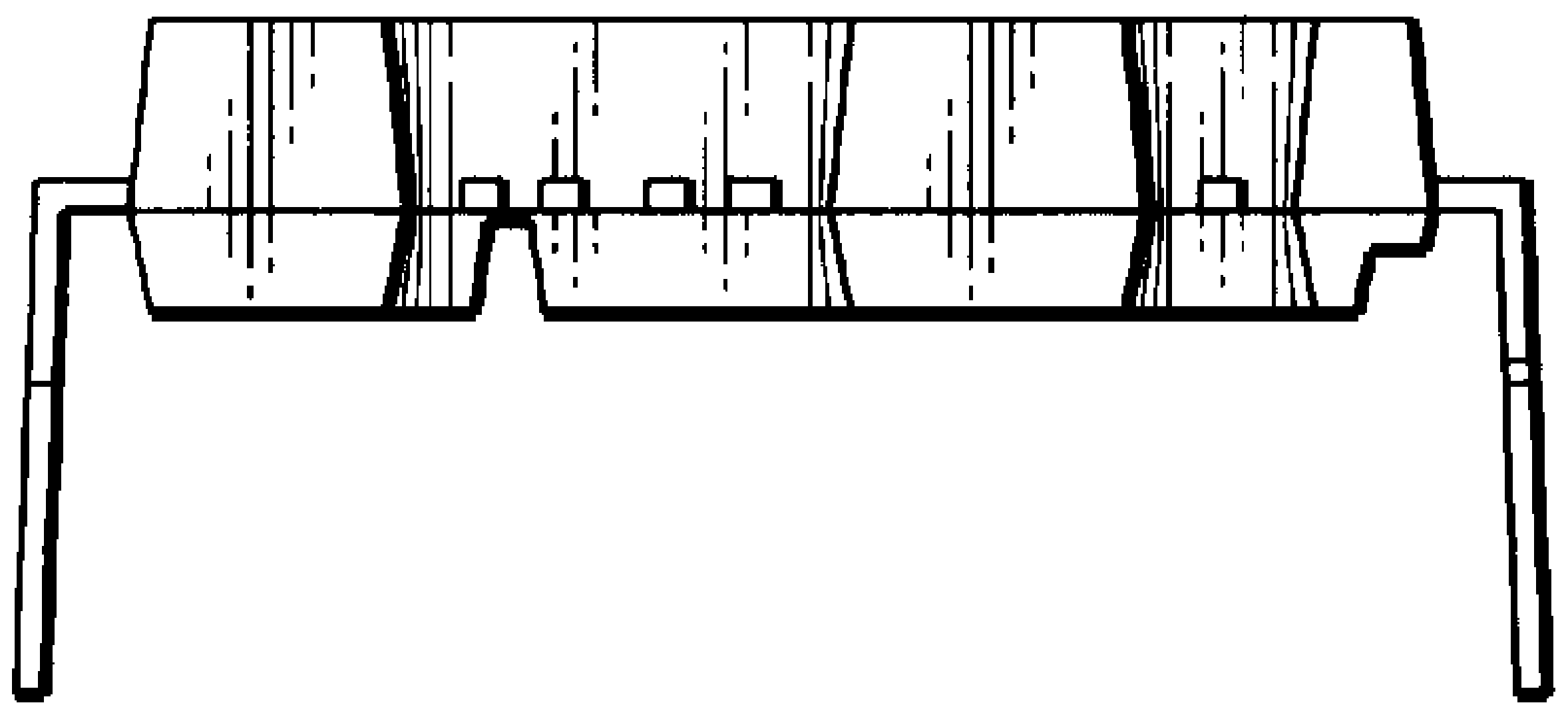


FIG.9

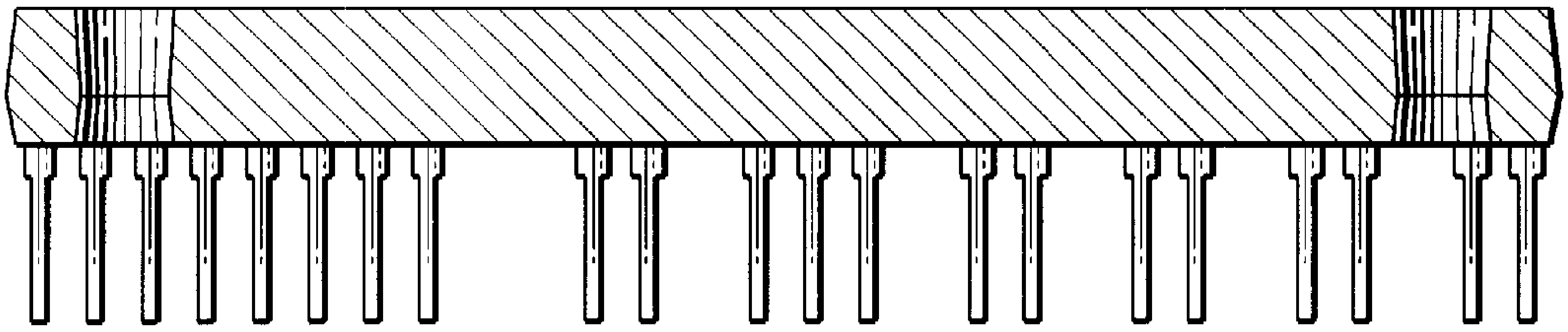


FIG.10

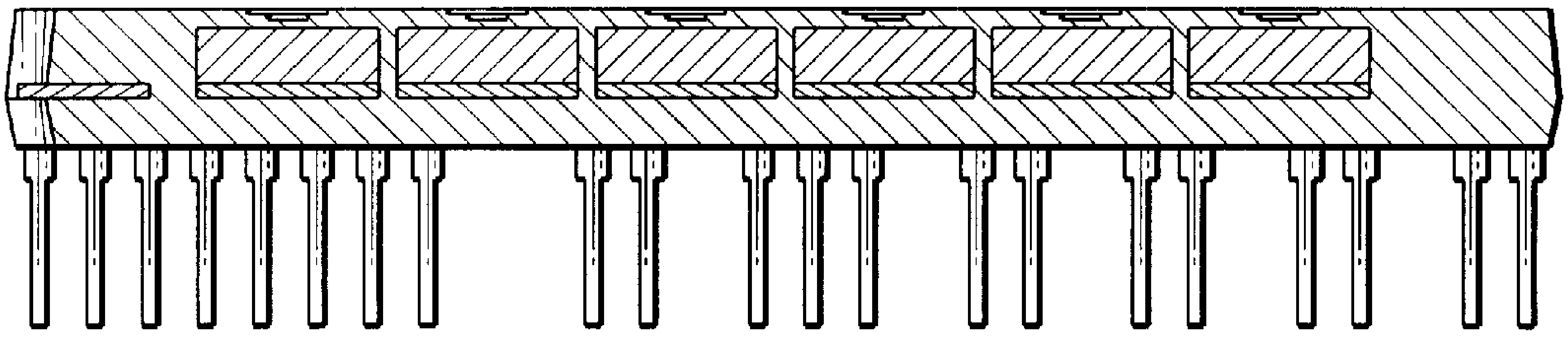


FIG.11

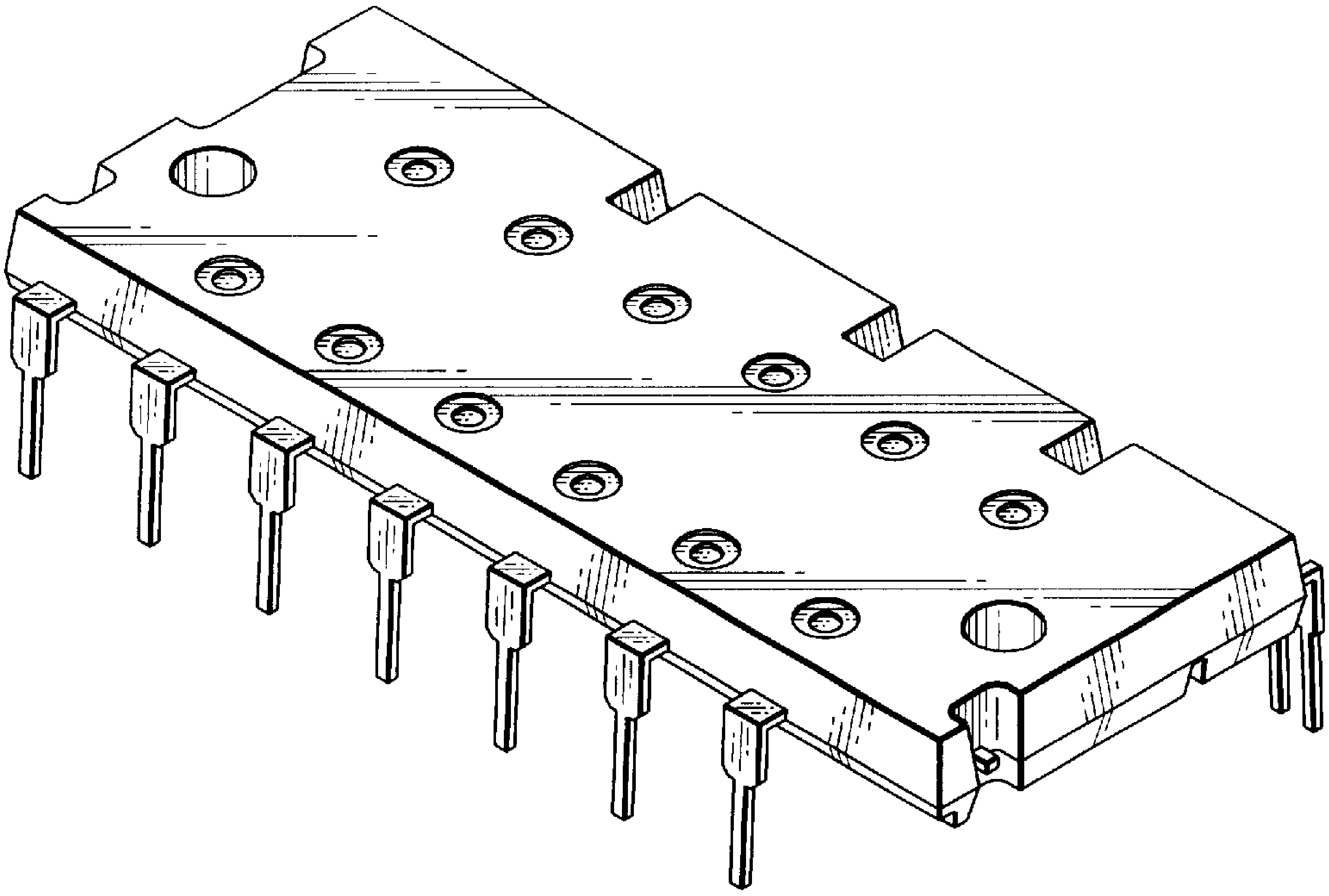


FIG.12

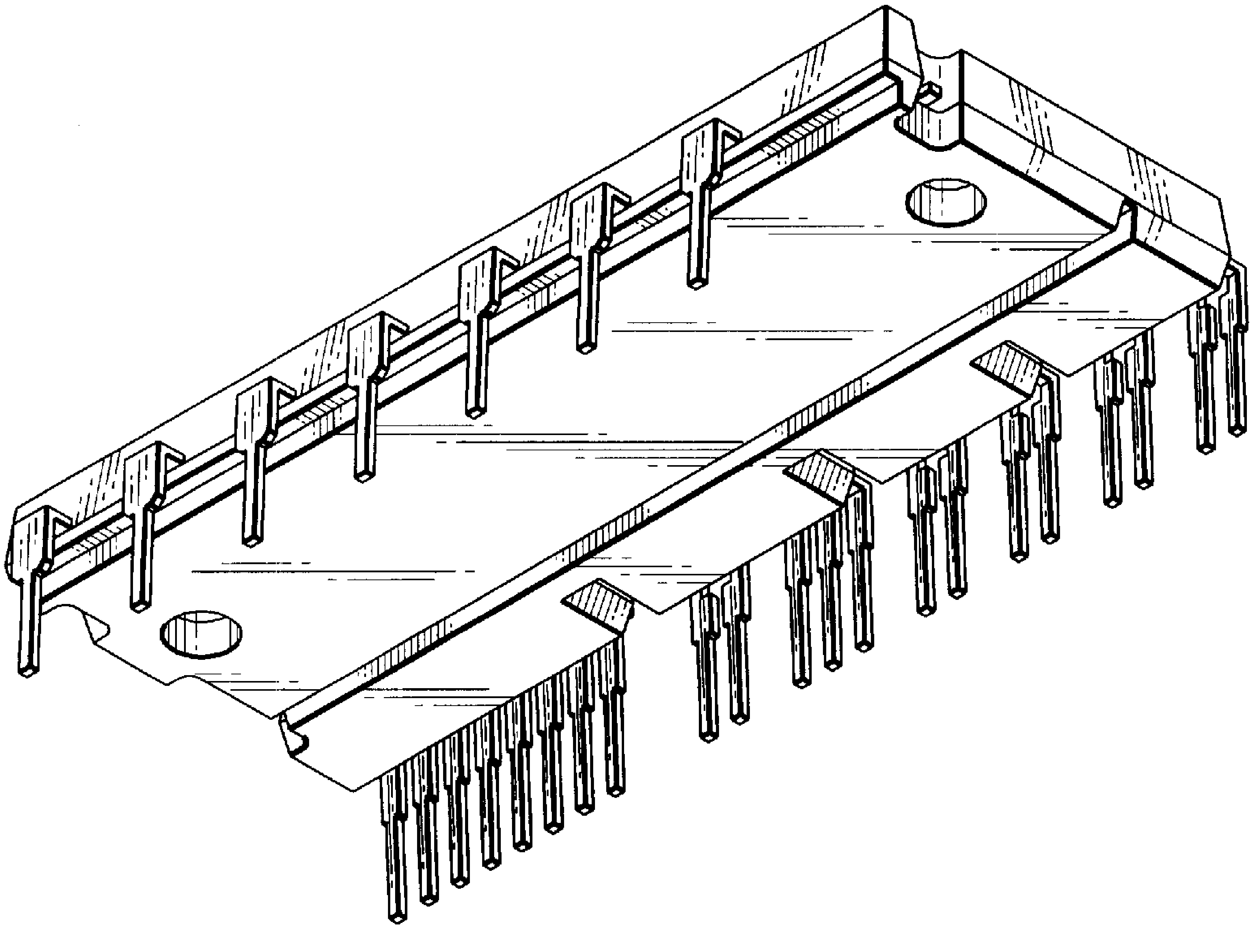


FIG.13

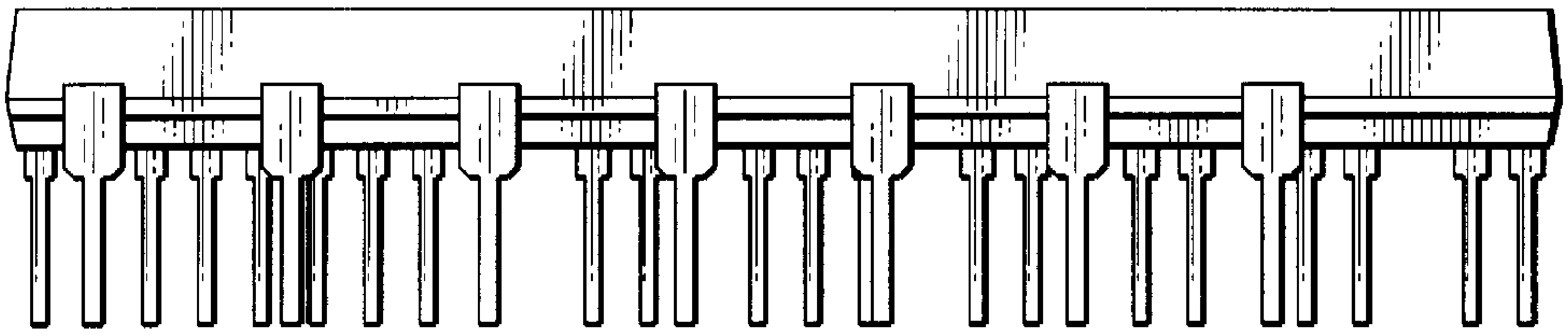


FIG.14

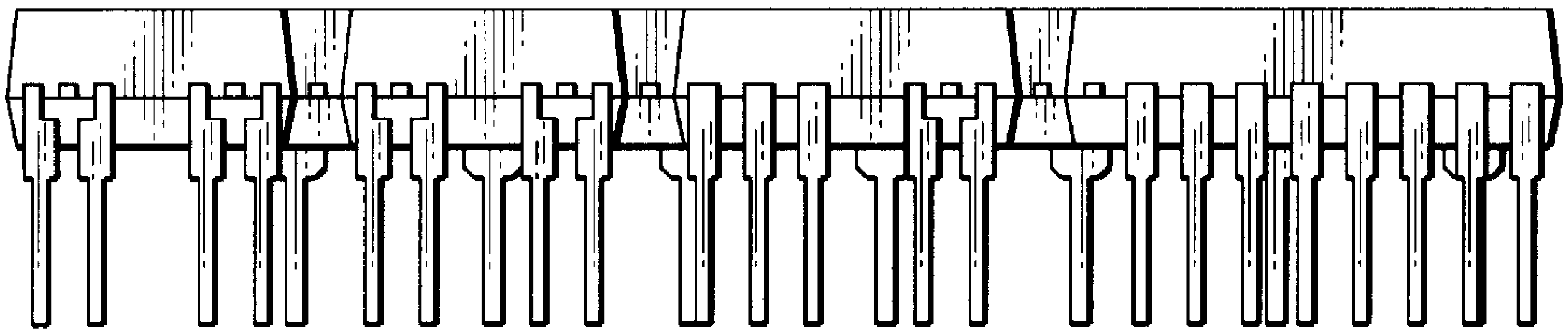


FIG.15

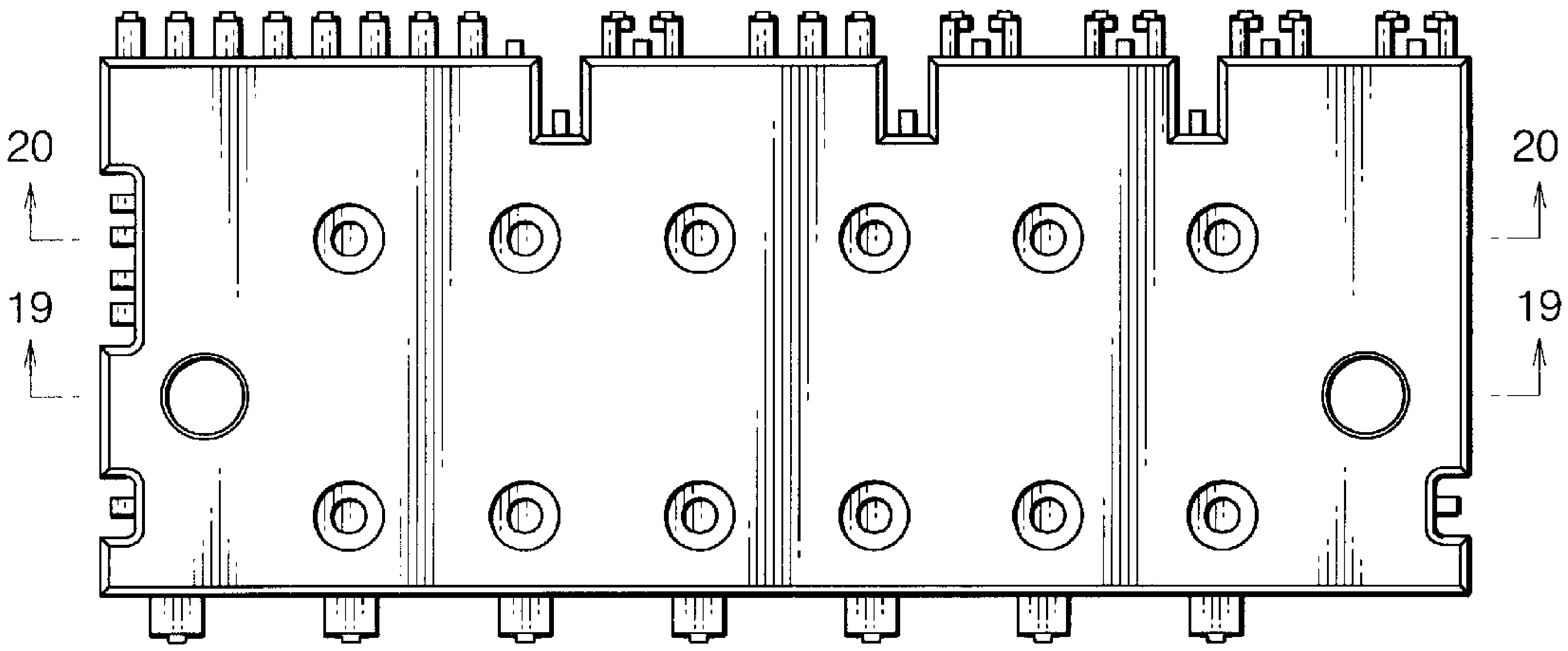


FIG.16

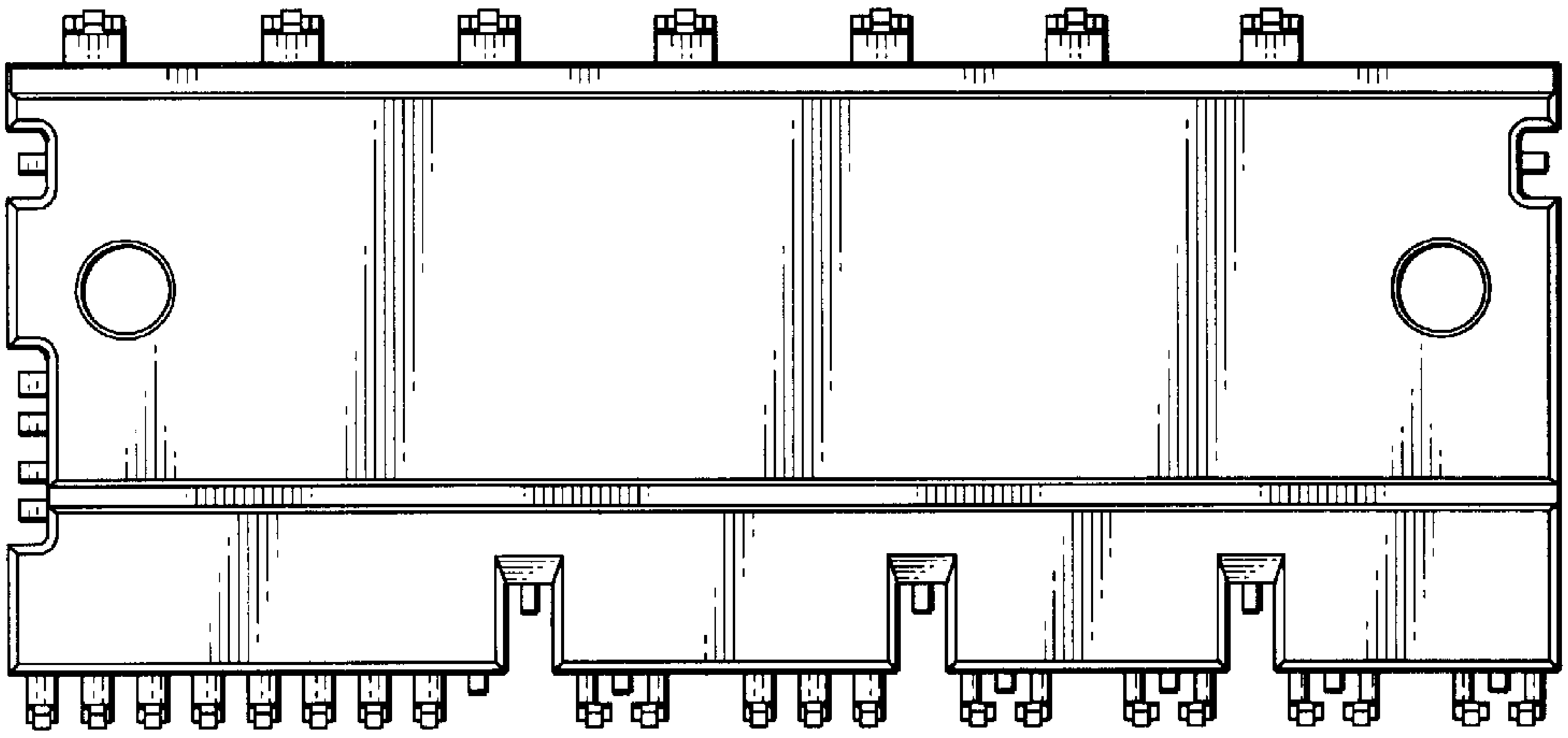


FIG.17

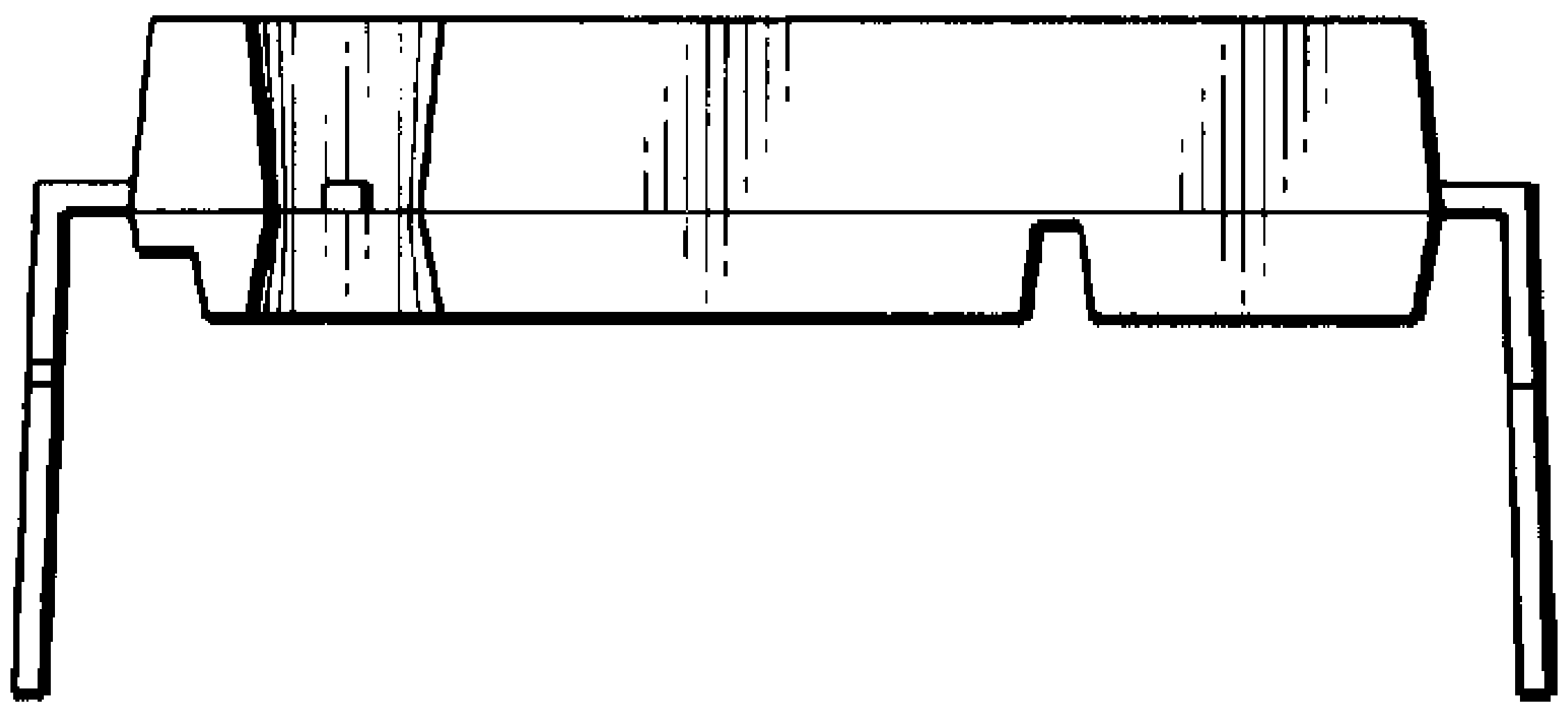


FIG.18

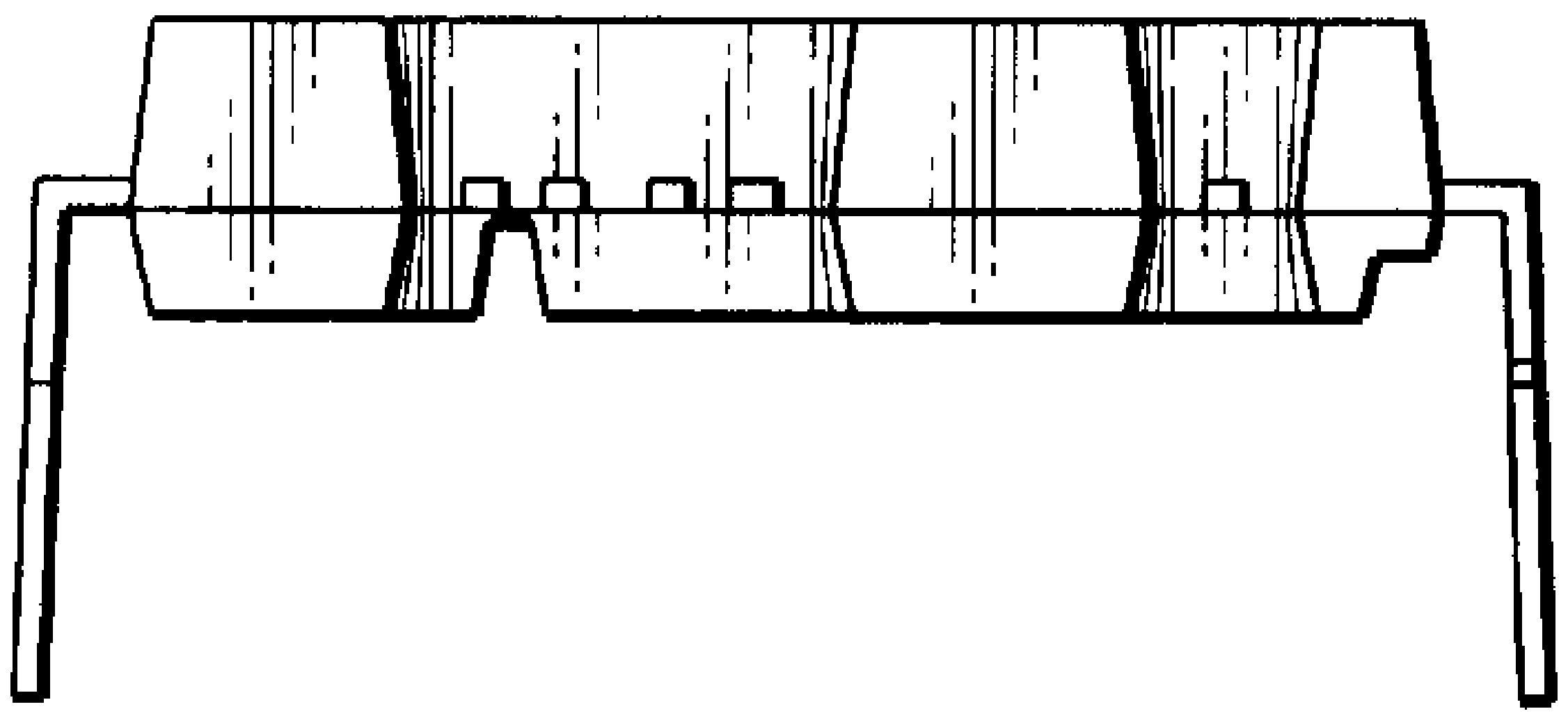


FIG.19

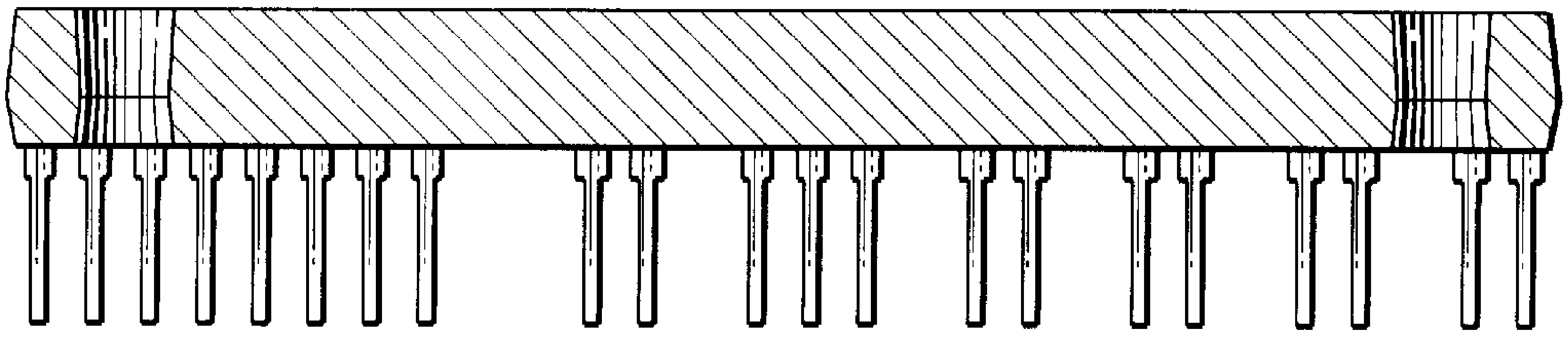


FIG.20