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(12) United States Design Patent

Sakasegawa

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(45) Date of Patent: ** Dec. 24, 2002

(54) **SIGNAL INPUT/OUTPUT DEVICE**

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(73) Assignee: **SMC Kabushiki Kaisha**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/151,152**

(22) Filed: **Nov. 1, 2001**

(30) **Foreign Application Priority Data**

May 9, 2001 (JP) 2001-013256

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/123**
(58) **Field of Search** D13/123, 110, D13/184; 439/639, 540.1, 654

(56) **References Cited**

U.S. PATENT DOCUMENTS

D413,323 S * 8/1999 Tashiro D13/123
D433,998 S * 11/2000 Ishitsuka et al. D13/123
D448,344 S * 9/2001 Ishitsuka et al. D13/123

* cited by examiner

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(57) **CLAIM**

The ornamental design for a signal input/output device, as shown.

DESCRIPTION

FIG. **1** is a top, front and left side perspective view of a signal input/output device showing my new design;
FIG. **2** is a front view thereof;
FIG. **3** is a rear view thereof;
FIG. **4** is a top plan view thereof;
FIG. **5** is a bottom plan view thereof;
FIG. **6** is a right side view thereof; and,
FIG. **7** is a left side view thereof.

1 Claim, 4 Drawing Sheets

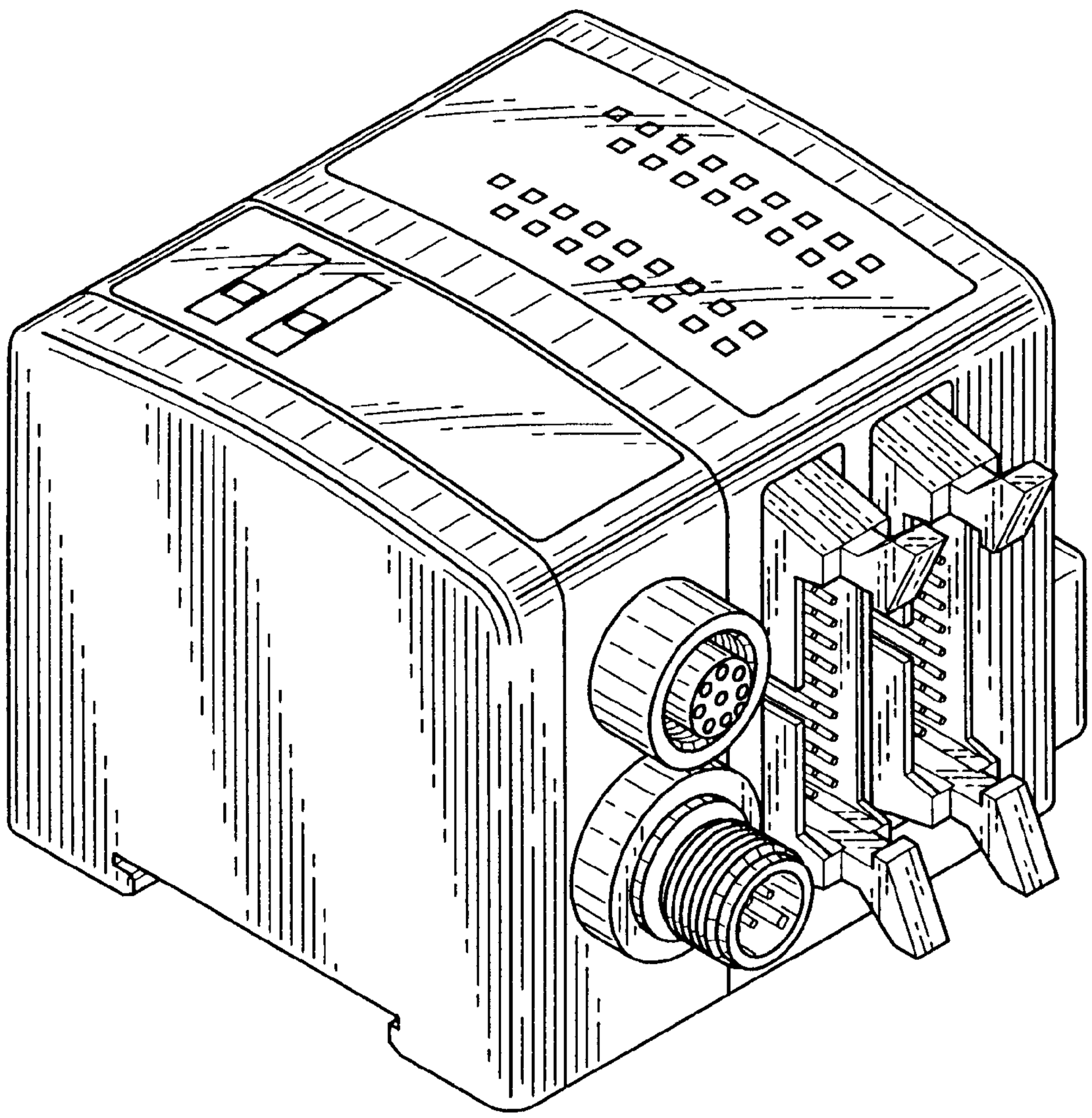

FIG. 1

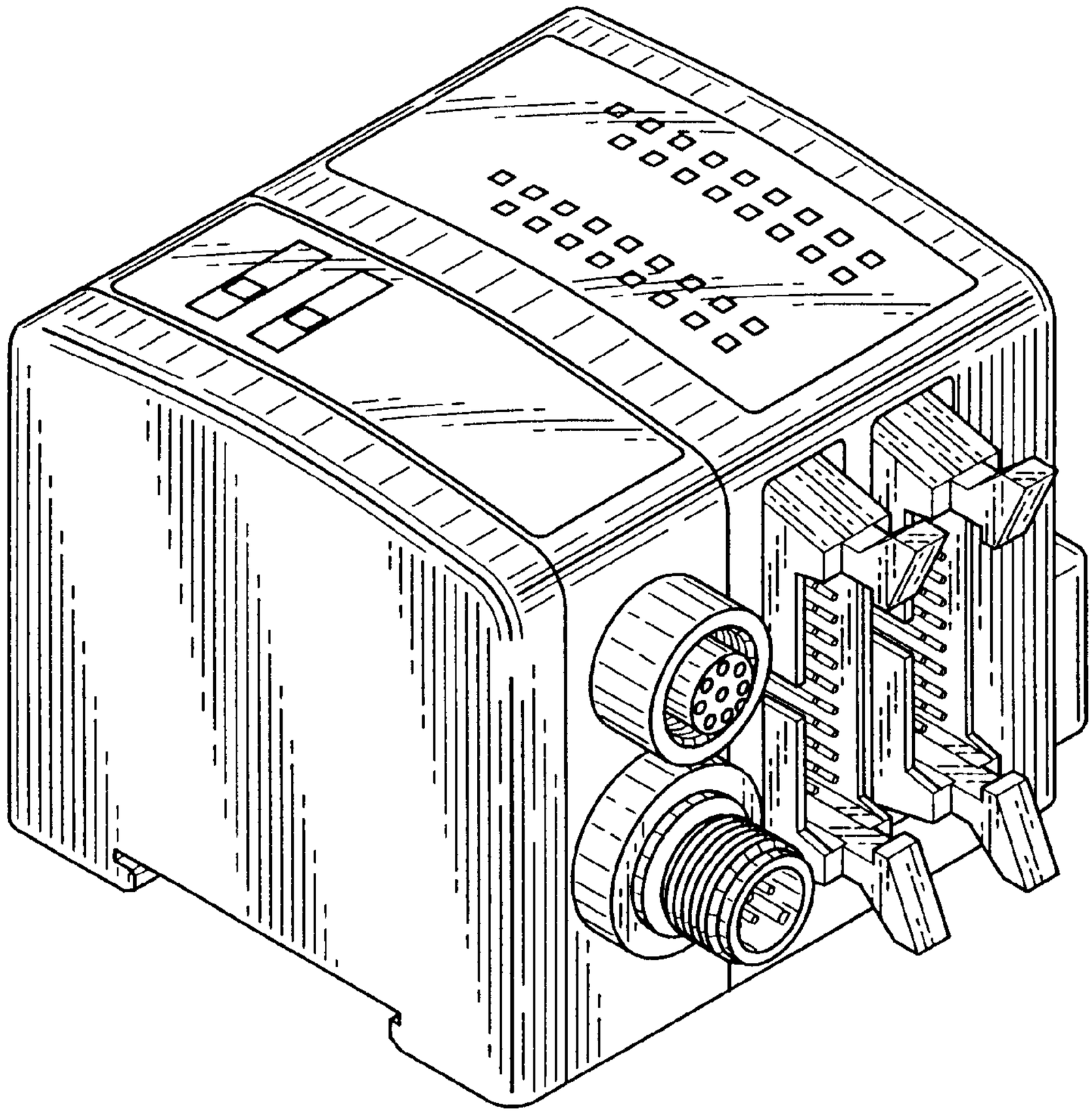

FIG. 2

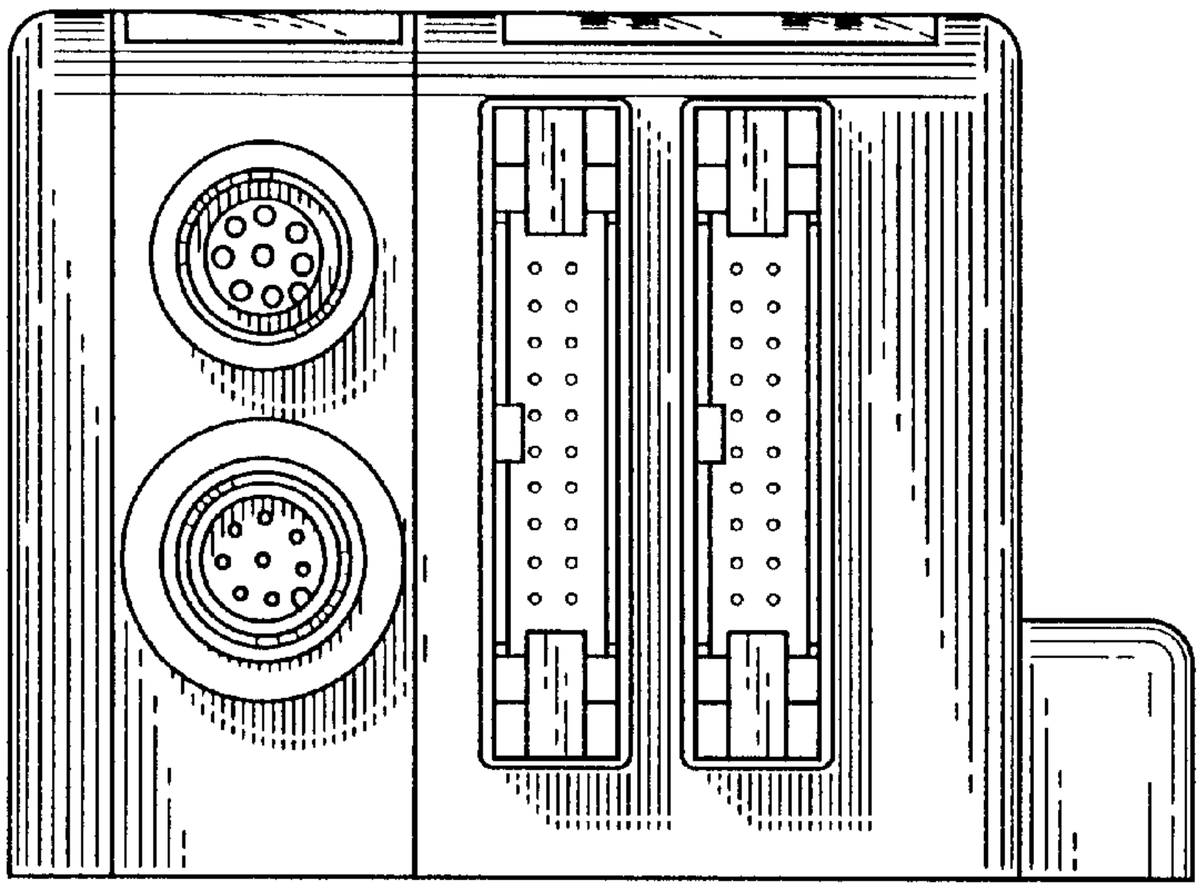

FIG. 3

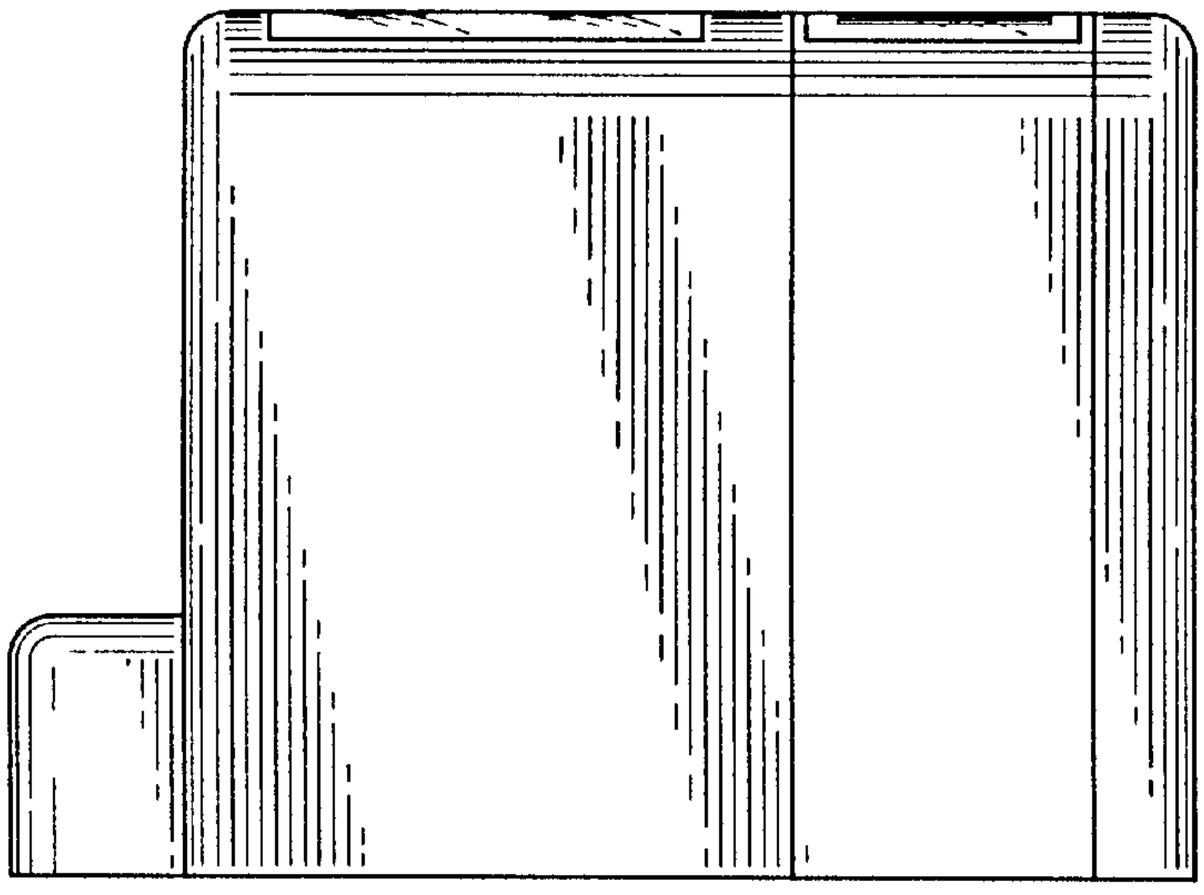

FIG. 4

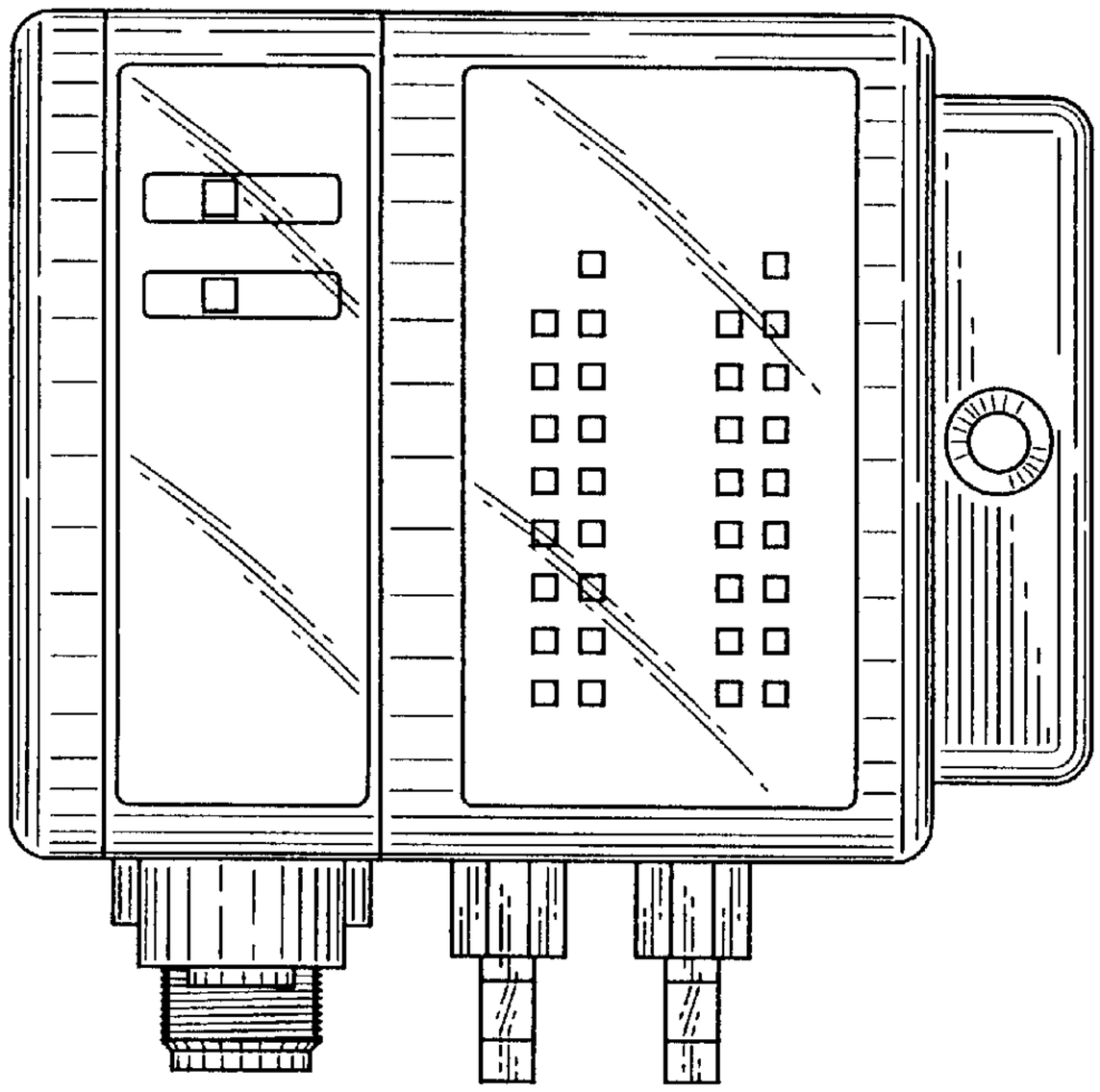

FIG. 5

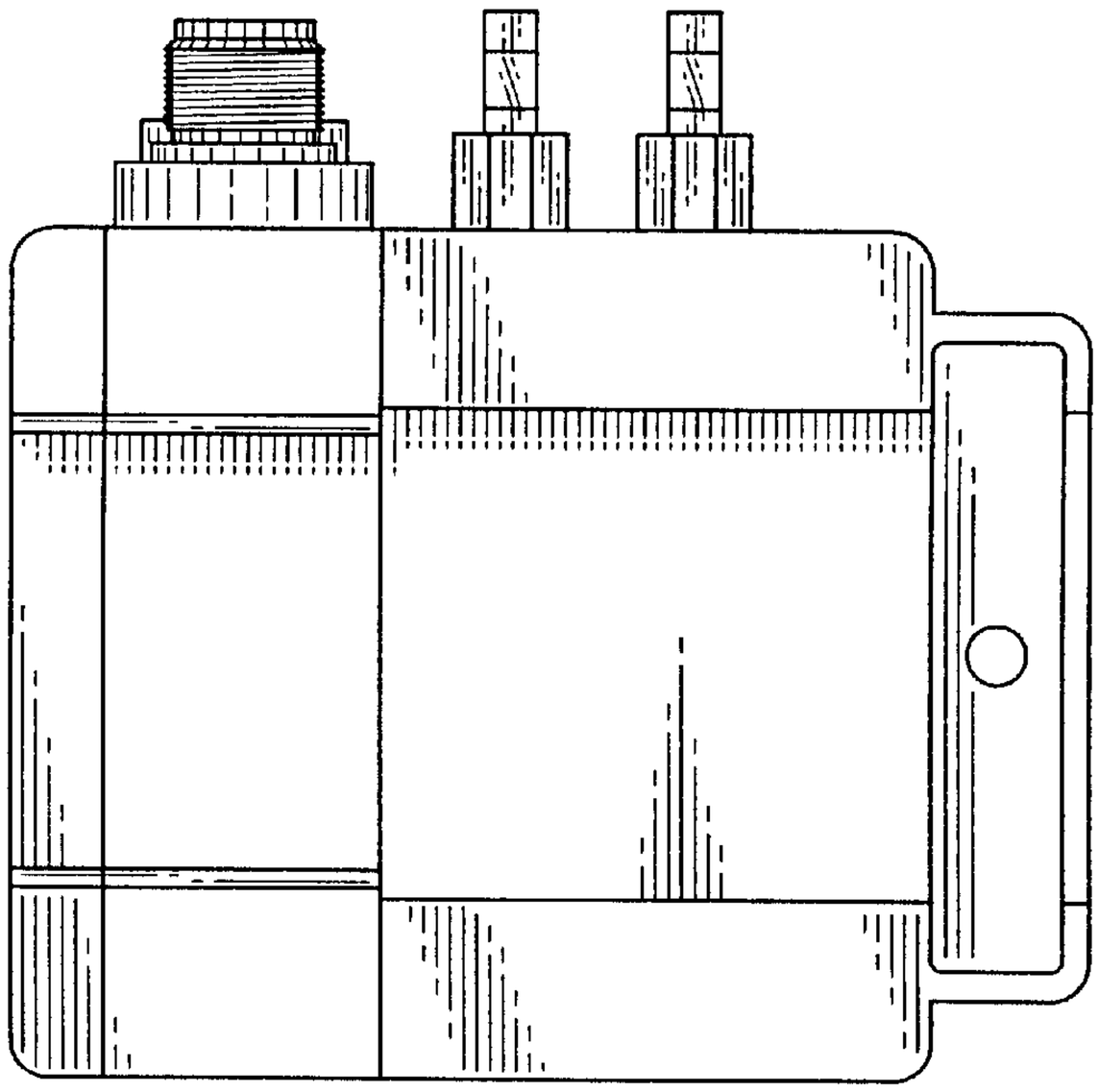

FIG. 6

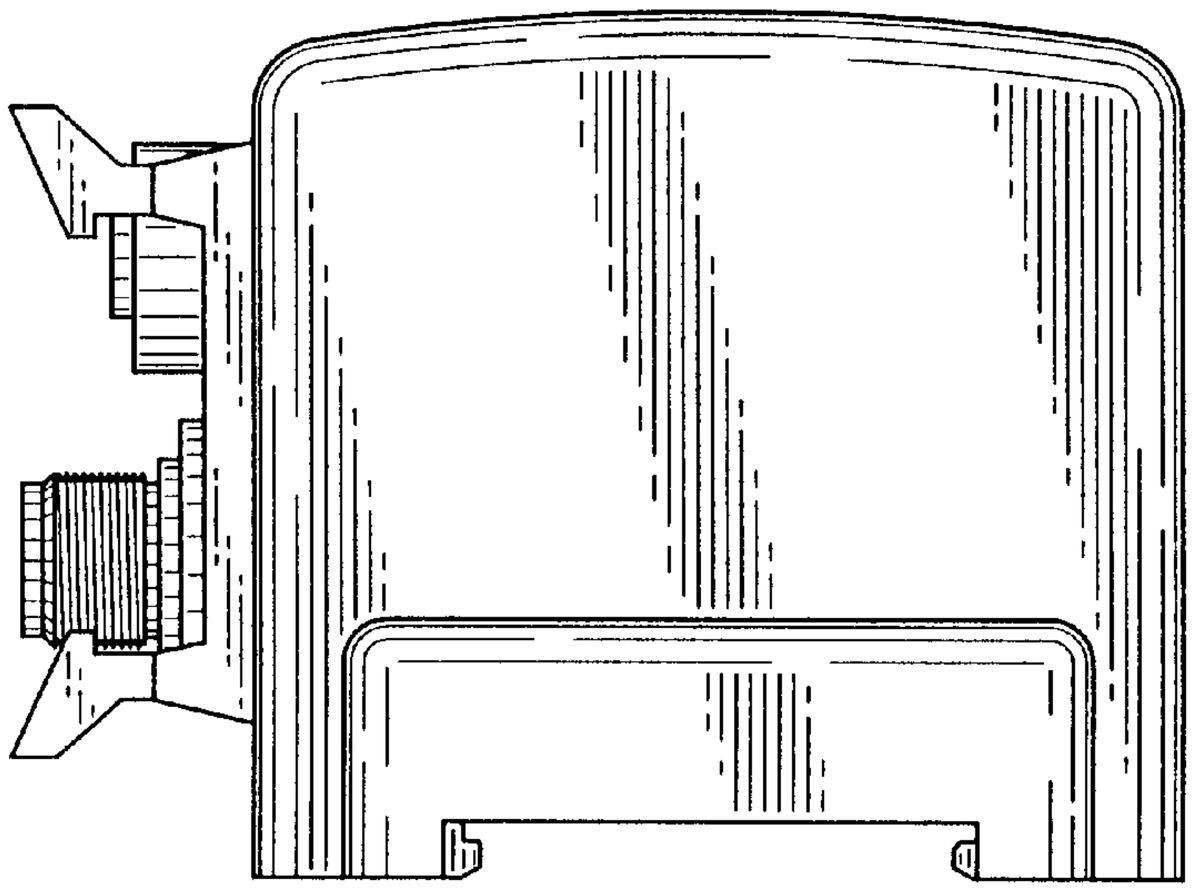

FIG. 7