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(12) **United States Design Patent**  
**Maehara et al.**

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(54) **SEMICONDUCTOR PACKAGE**

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(73) Assignee: **Shindengen Electric Manufacturing Co., Ltd.**, Tokyo (JP)

(\*\*) Term: **14 Years**

(21) Appl. No.: **29/142,263**

(22) Filed: **May 23, 2001**

(51) **LOC (7) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Search** ..... D13/182; D14/114;  
174/52.1, 52.2, 52.4, 52.5, 16.3; 206/710,  
719; 257/254, 659, 697, 730, 738; 324/755,  
765; 361/752, 798, 850, 718, 730

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(57) **CLAIM**

The ornamental design for a semiconductor package, as shown and described.

**DESCRIPTION**

FIG. 1 is a front, plan and right side perspective view of a semiconductor package showing our new design;

FIG. 2 is a front, bottom and right side perspective view thereof;

FIG. 3 is a rear, plan and left side perspective view thereof;

FIG. 4 is a rear, bottom and left side perspective view thereof;

FIG. 5 is a front elevational view thereof;

FIG. 6 is a rear elevational view thereof;

FIG. 7 is a top plan view thereof;

FIG. 8 is a bottom plan view thereof;

FIG. 9 is a left side elevational view thereof; and,

FIG. 10 is a right side elevational view thereof.

**1 Claim, 4 Drawing Sheets**

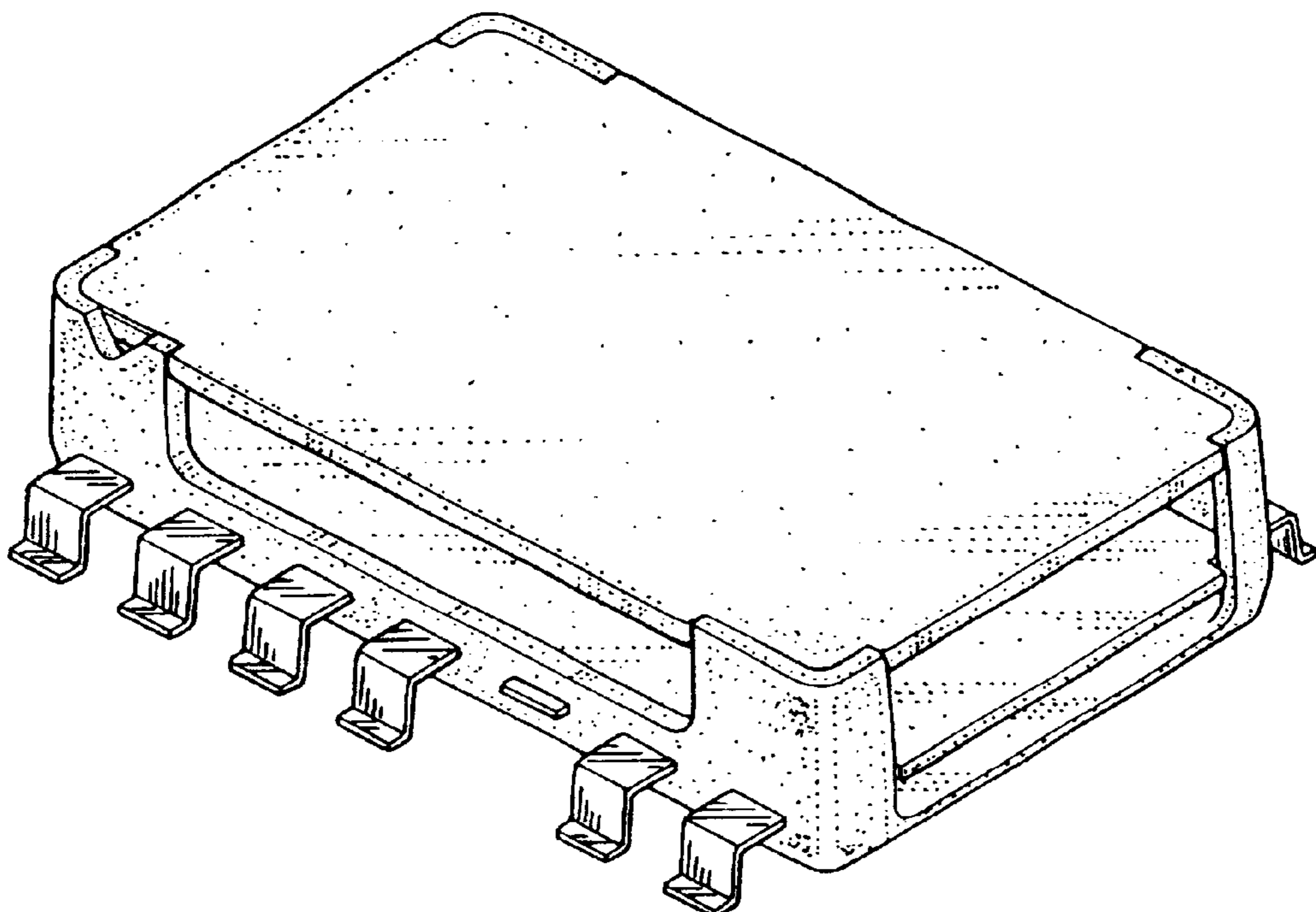


FIG. 1

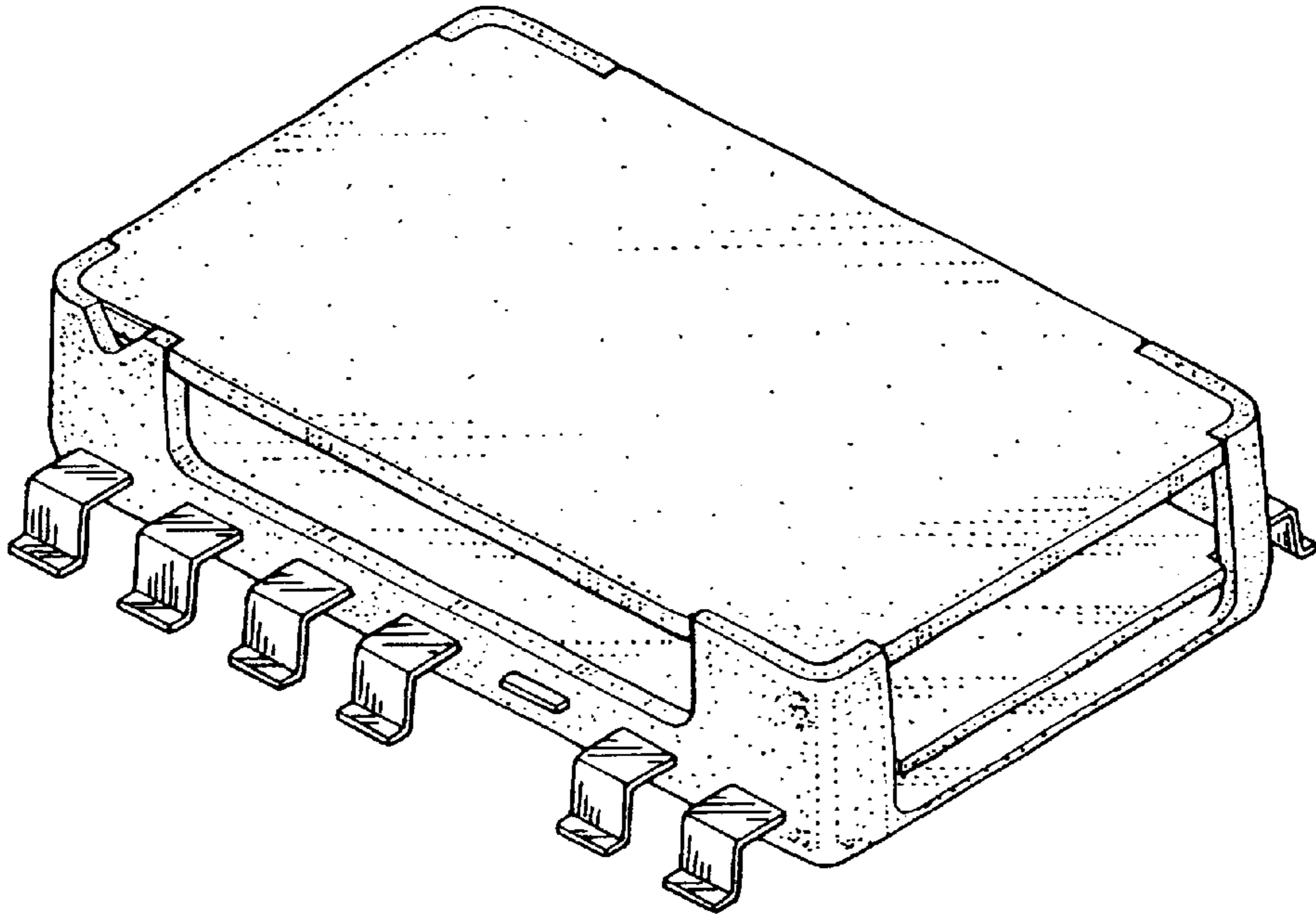


FIG. 2

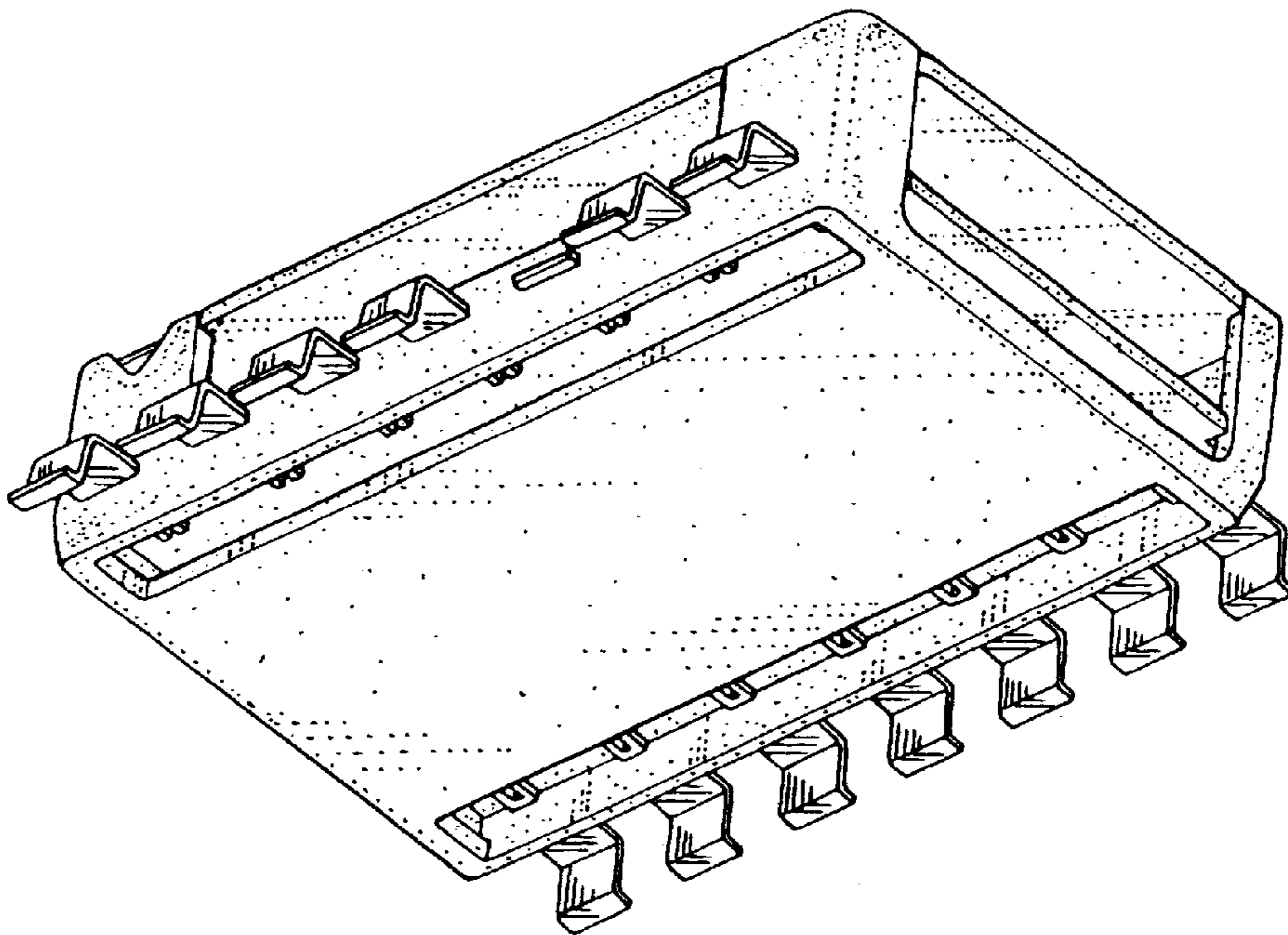


FIG. 3

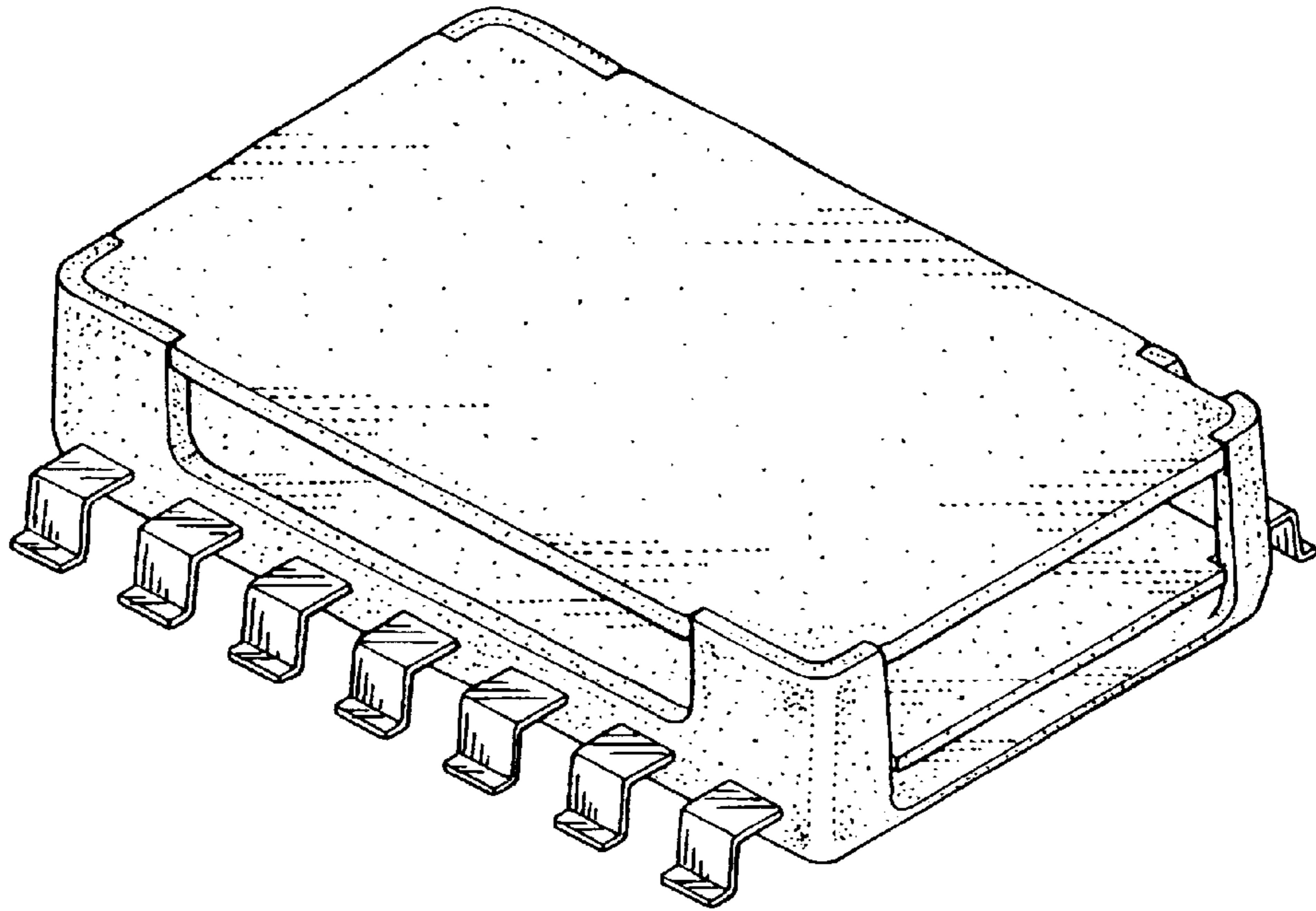


FIG. 4

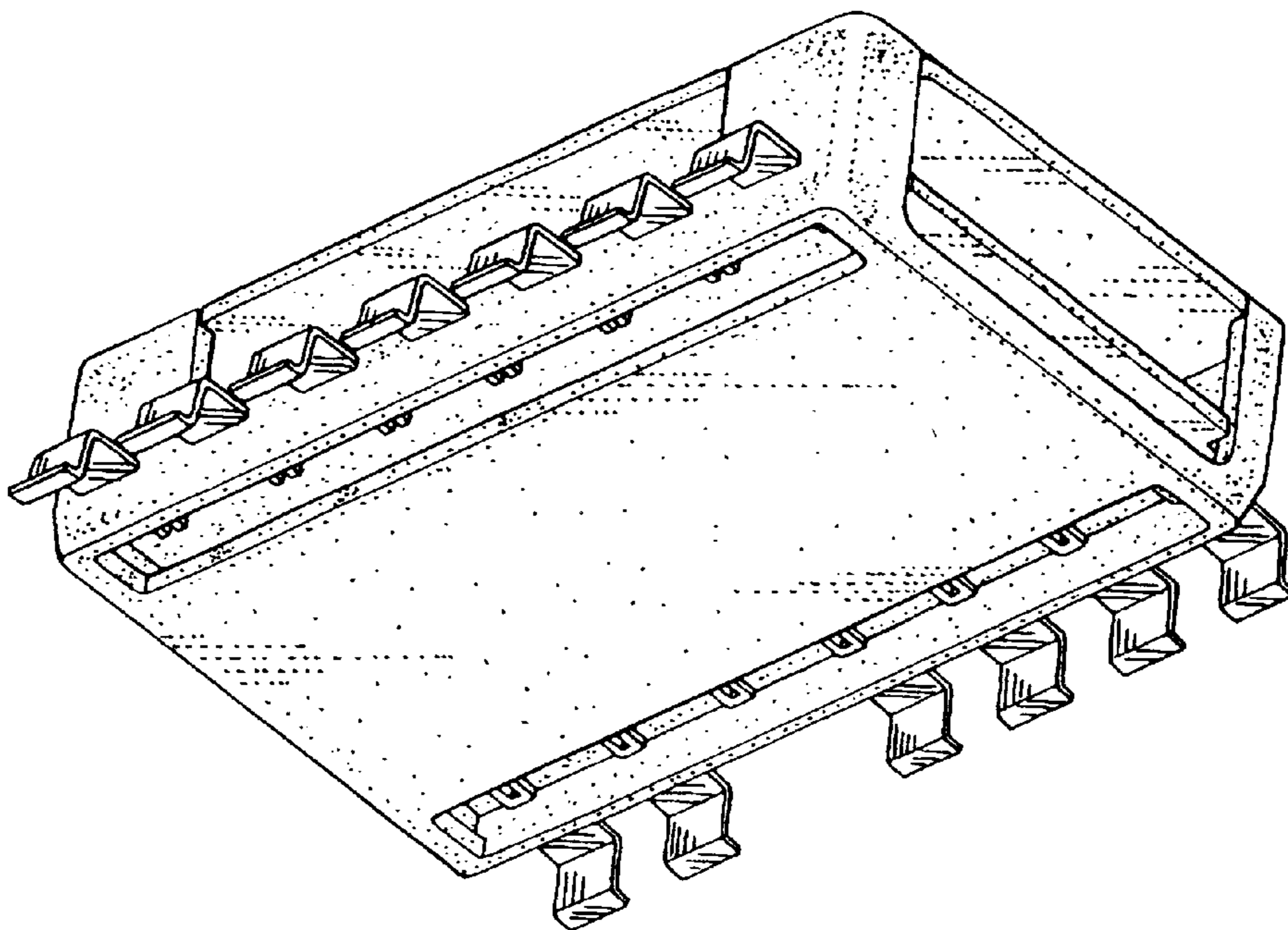


FIG. 5

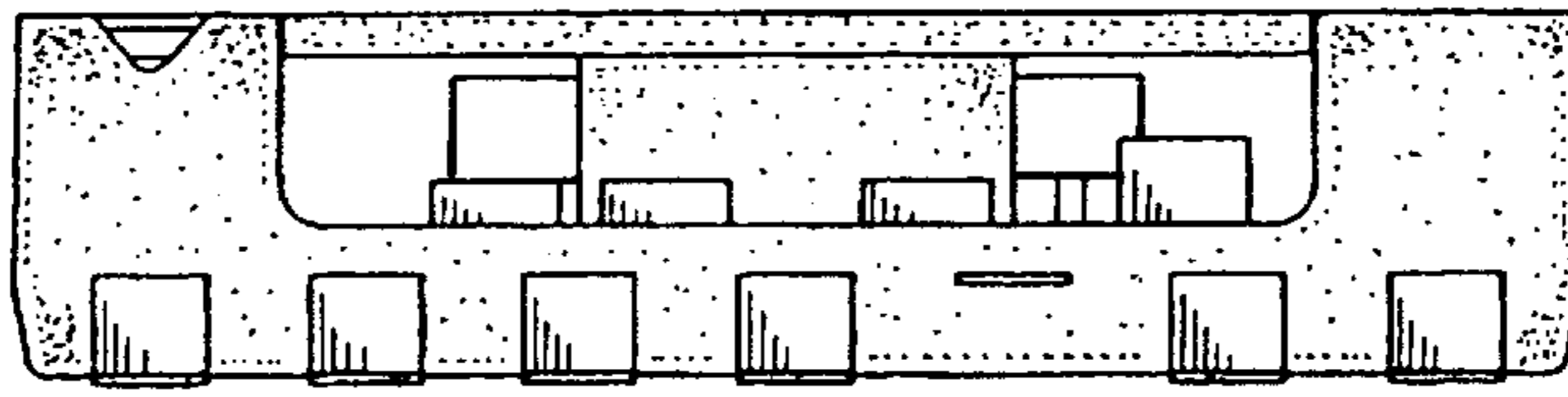


FIG. 6

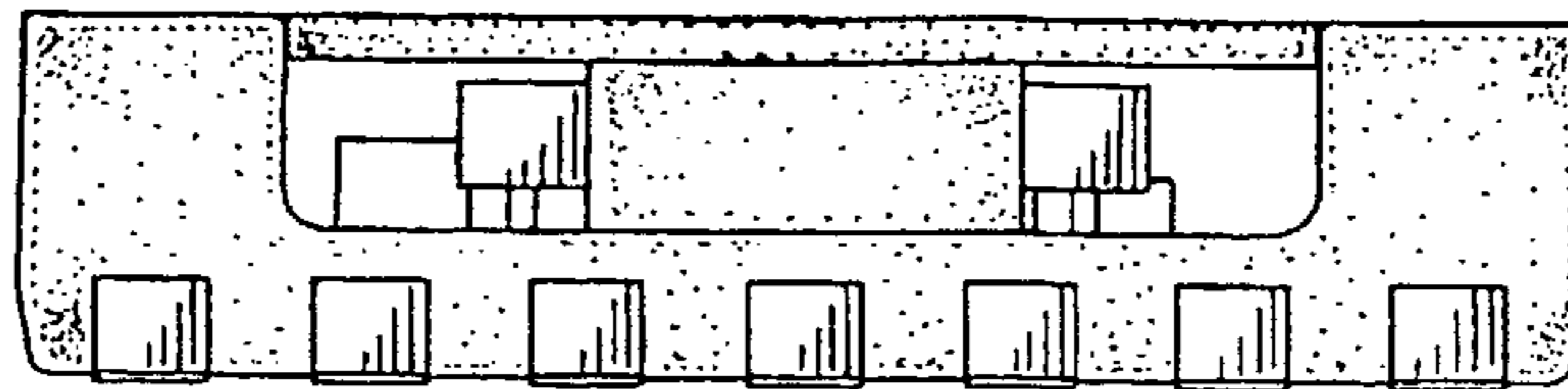


FIG. 7

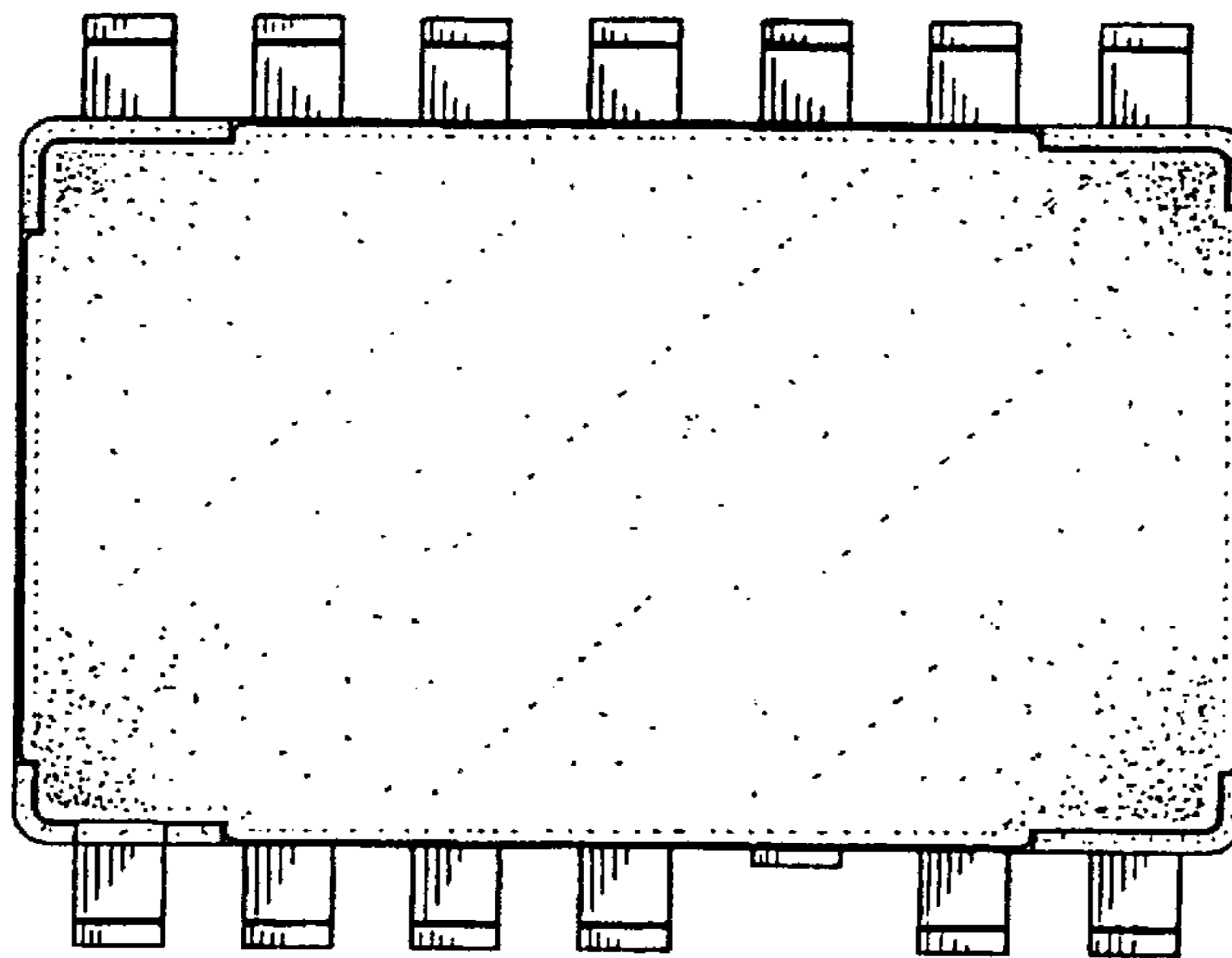


FIG. 8

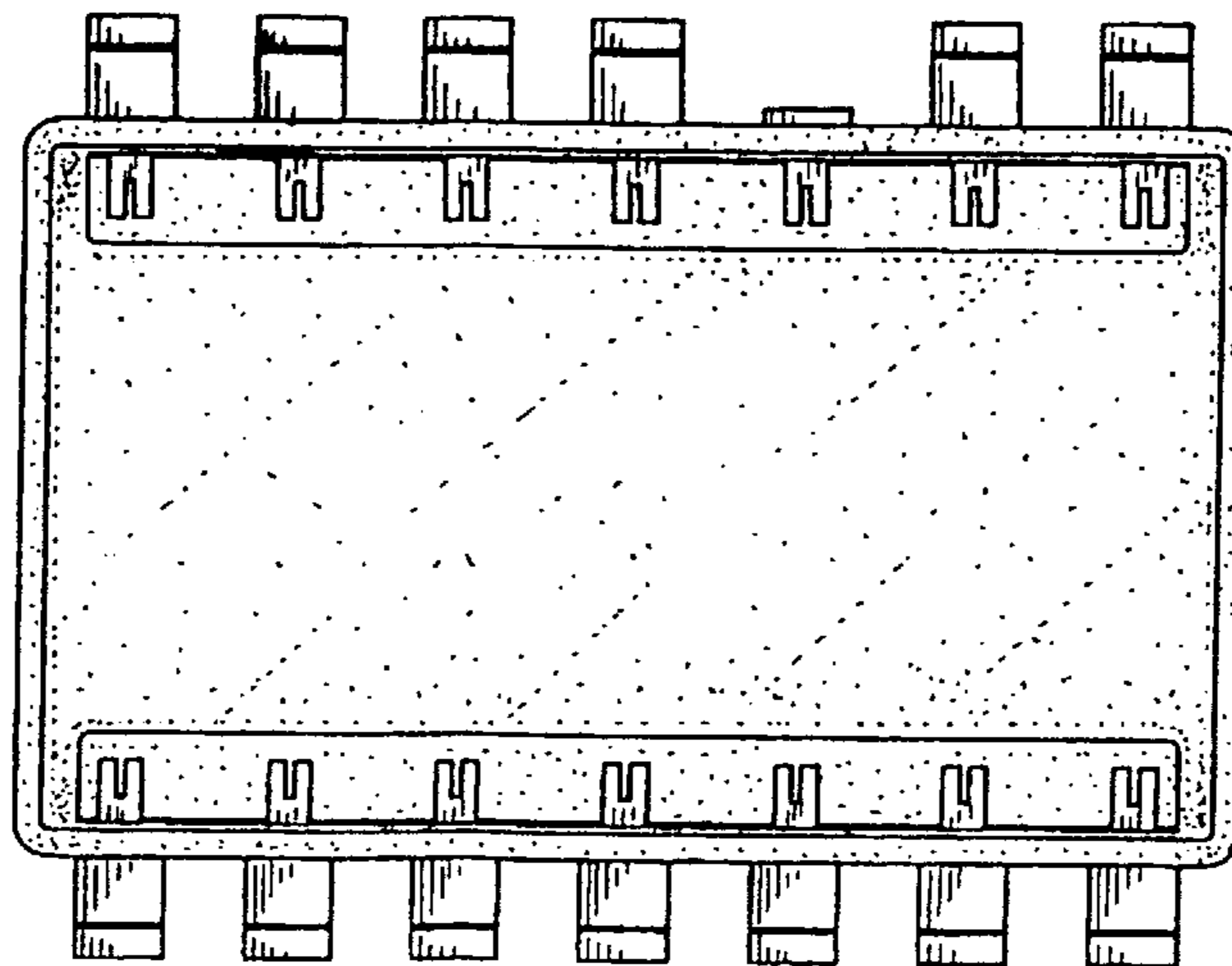


FIG. 9

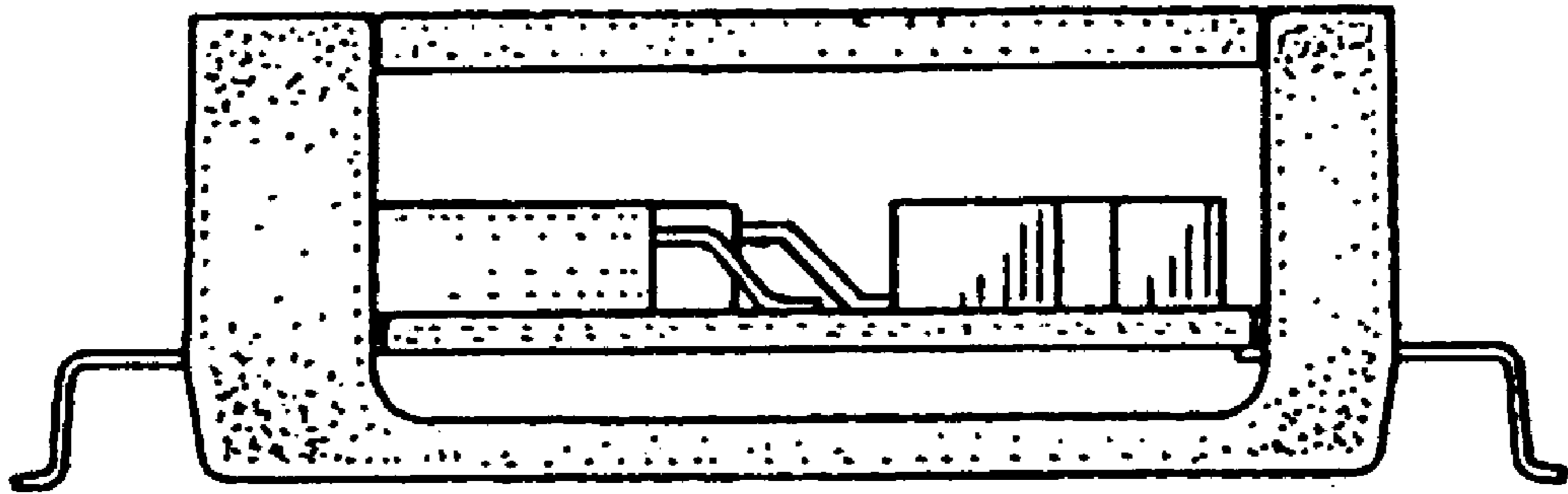


FIG. 10

