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(12) United States Design Patent
Kaise

(10) **Patent No.:** **US D460,702 S**
(45) **Date of Patent:** ** **Jul. 23, 2002**

(54) **CIRCUIT TESTER**

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(73) Assignee: **Kaise Kabushiki Kaisha**, Nagano (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/139,954**

(22) Filed: **Apr. 9, 2001**

(51) **LOC (7) Cl.** **10-04**
(52) **U.S. Cl.** **D10/78**
(58) **Field of Search** D10/78; 324/72.5, 324/149, 156, 508, 509, 538; 340/815.74

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(57) **CLAIM**

The ornamental design for a circuit tester, as shown and described.

DESCRIPTION

FIG. **1** is a plane view of a circuit tester showing my new design;

FIG. **2** is a front elevational view thereof;

FIG. **3** is a rear elevational view of thereof

FIG. **4** is a bottom plane view thereof;

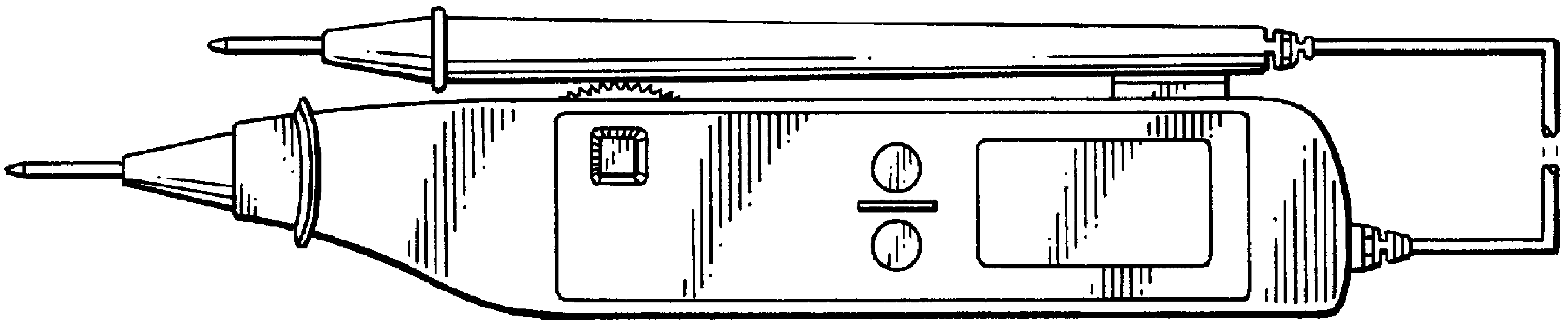
FIG. **5** is a left side elevational view thereof;

FIG. **6** is a right side elevational view thereof;

FIG. **7** is a plane view, in which the testing rod is separated from the main body section; and,

FIG. **8** is a perspective elevational view thereof.

1 Claim, 3 Drawing Sheets



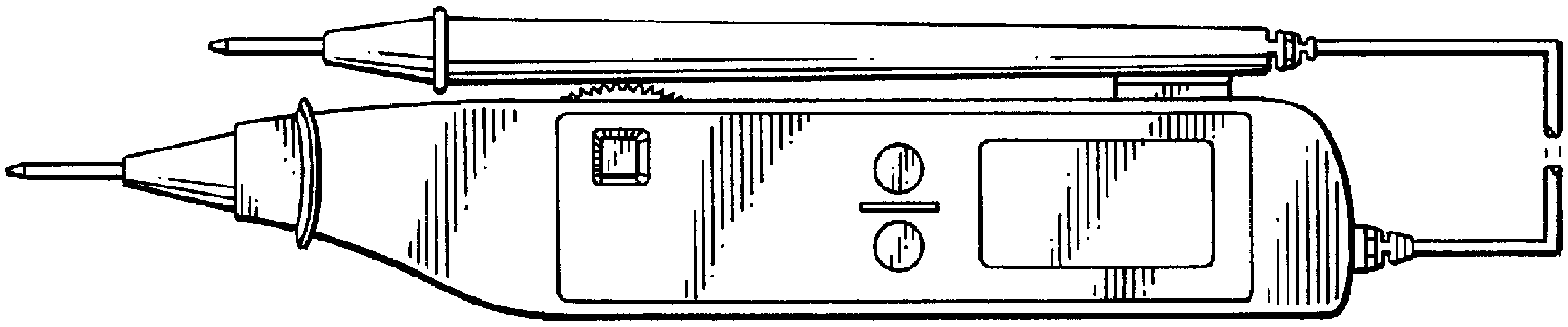


FIG. 1

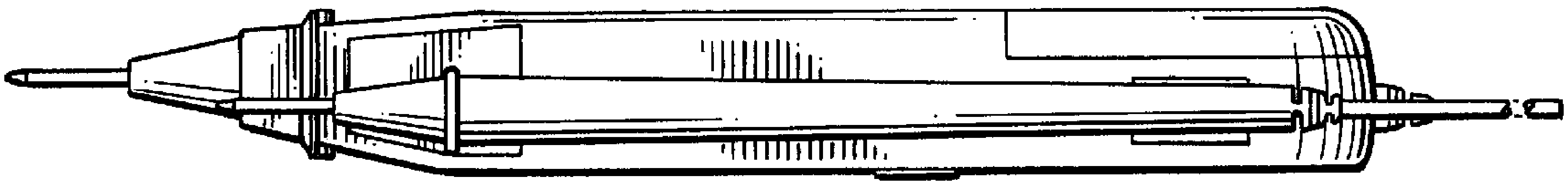


FIG. 2

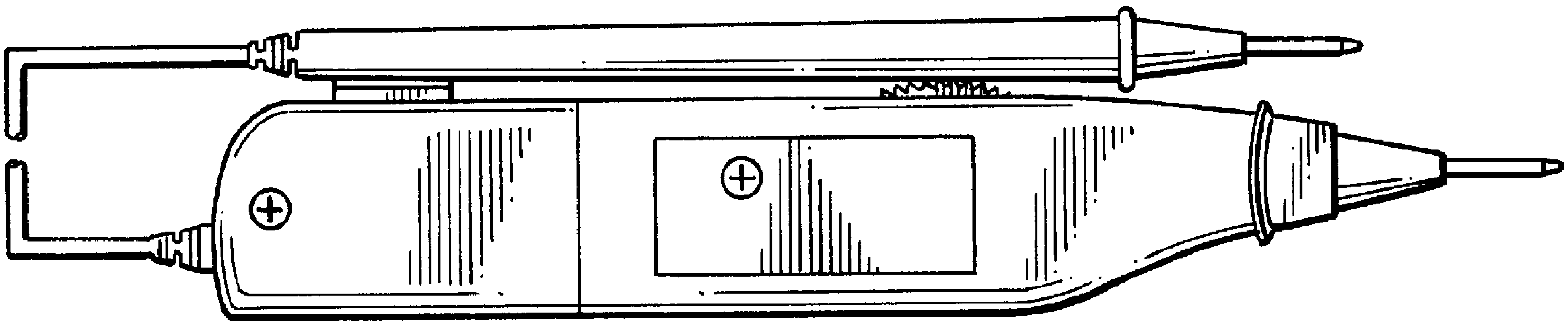


FIG. 3

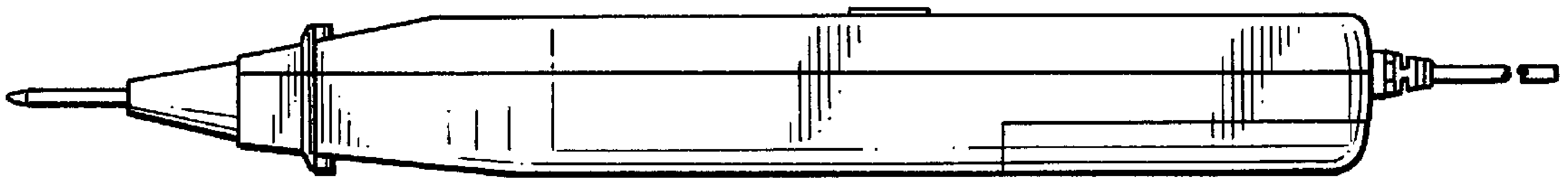


FIG. 4

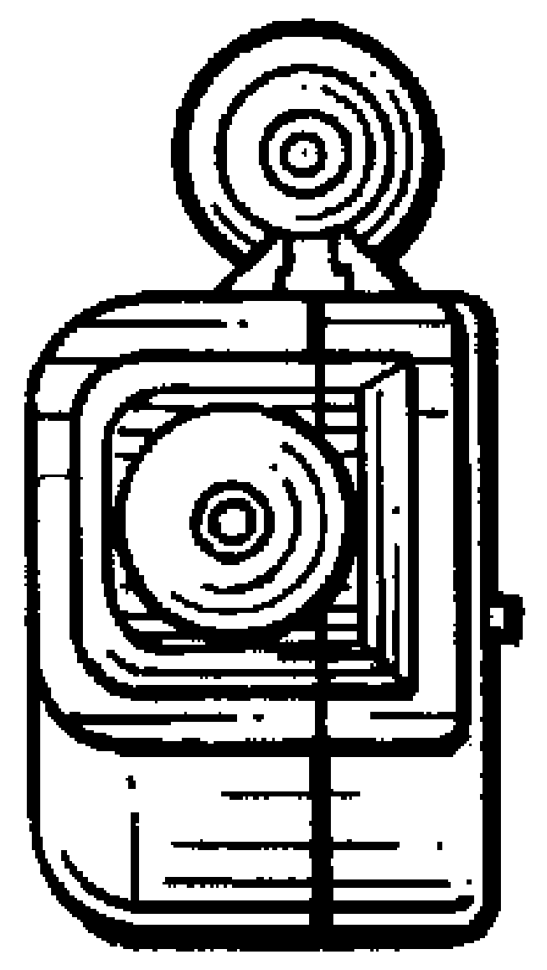


FIG. 5

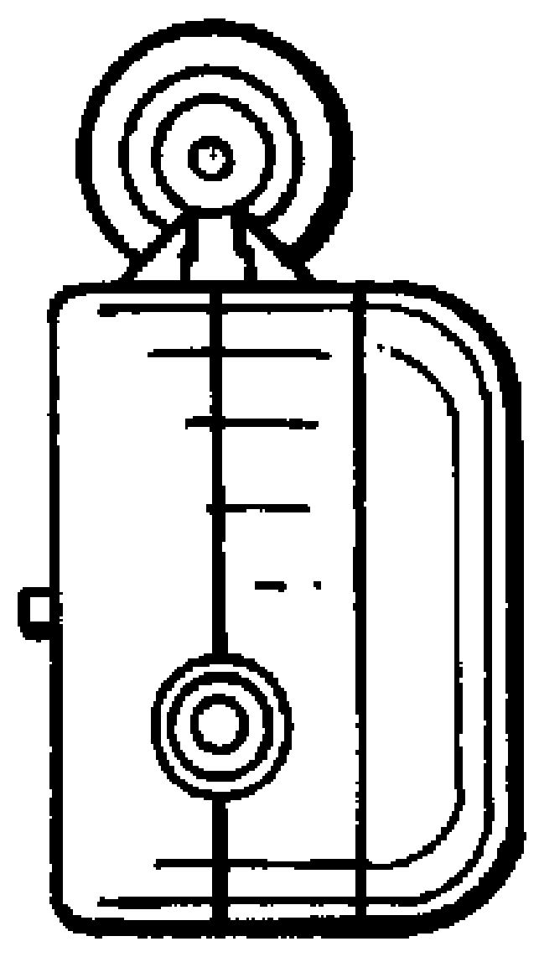


FIG. 6

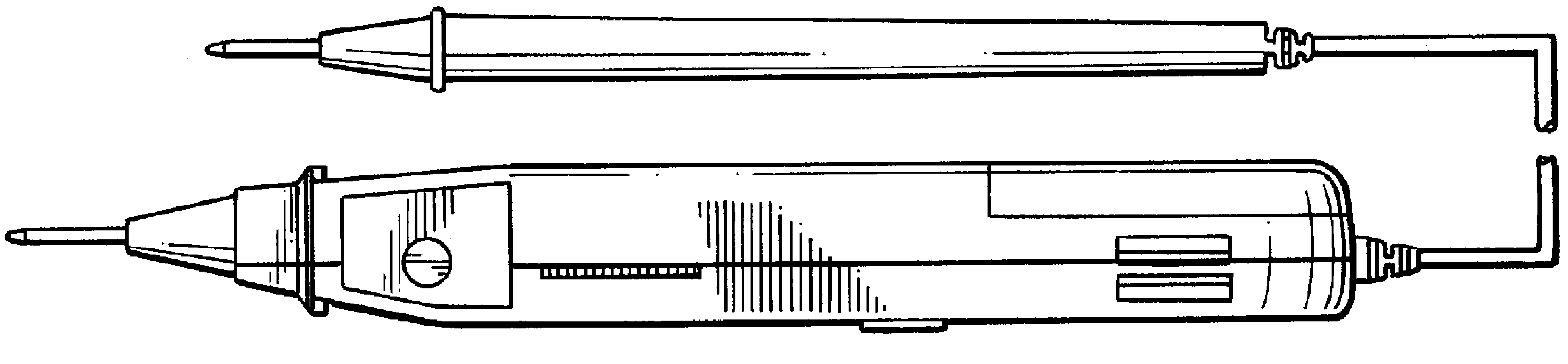


FIG. 7

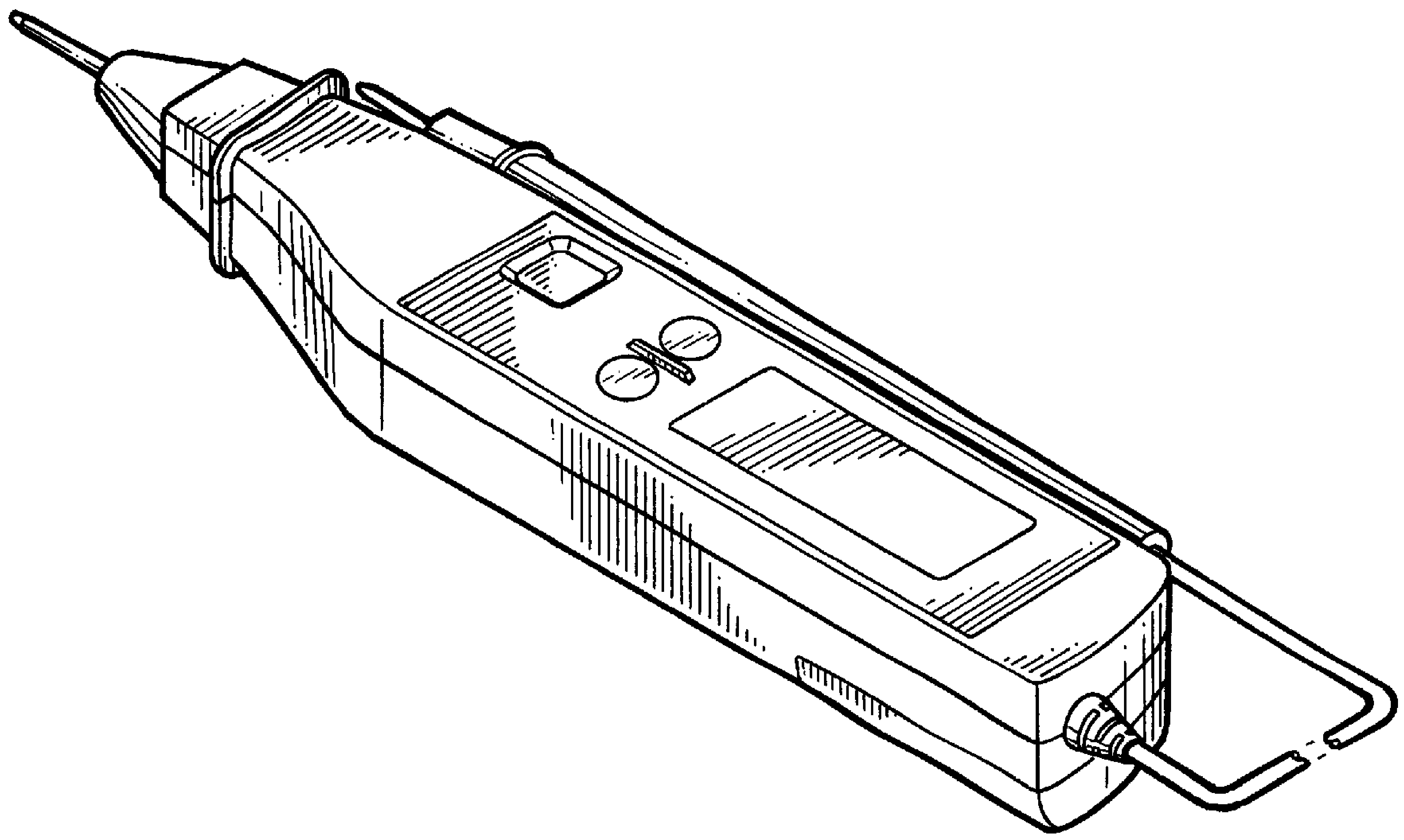


FIG. 8