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(12) **United States Design Patent**
Kato et al.

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(54) **HYBRID INTEGRATED CIRCUIT DEVICE**

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(**) Term: **14 Years**

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(51) **LOC (7) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Search** D13/182, 110,
D13/123, 133, 199; 29/829, 830, 831, 832,
846; 174/250, 251, 253, 254, 255, 260,
261, 268; 361/748, 752, 753, 718, 760,
783, 784, 820

(56) **References Cited**

U.S. PATENT DOCUMENTS

D357,671 S * 4/1995 Terasawa et al. D13/182
5,742,480 A * 4/1998 Sawada et al. 361/749

D396,450 S * 7/1998 Nishiura et al. D13/182
5,838,546 A * 11/1998 Miyoshi 361/749
5,905,639 A * 5/1999 Warren 361/776
6,028,773 A * 2/2000 Hundt 361/760
6,201,701 B1 * 3/2001 Linden et al. 361/720

* cited by examiner

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(57) **CLAIM**

The ornamental design for a hybrid integrated circuit device,
as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of a hybrid integrated circuit
device showing an embodiment of our new design;
FIG. 2 is a front elevational view thereof;
FIG. 3 is a rear elevational view thereof;
FIG. 4 is a left side elevational view thereof;
FIG. 5 is a right side elevational view thereof;
FIG. 6 is a top plan view thereof; and,
FIG. 7 is a bottom plan view thereof.

1 Claim, 3 Drawing Sheets

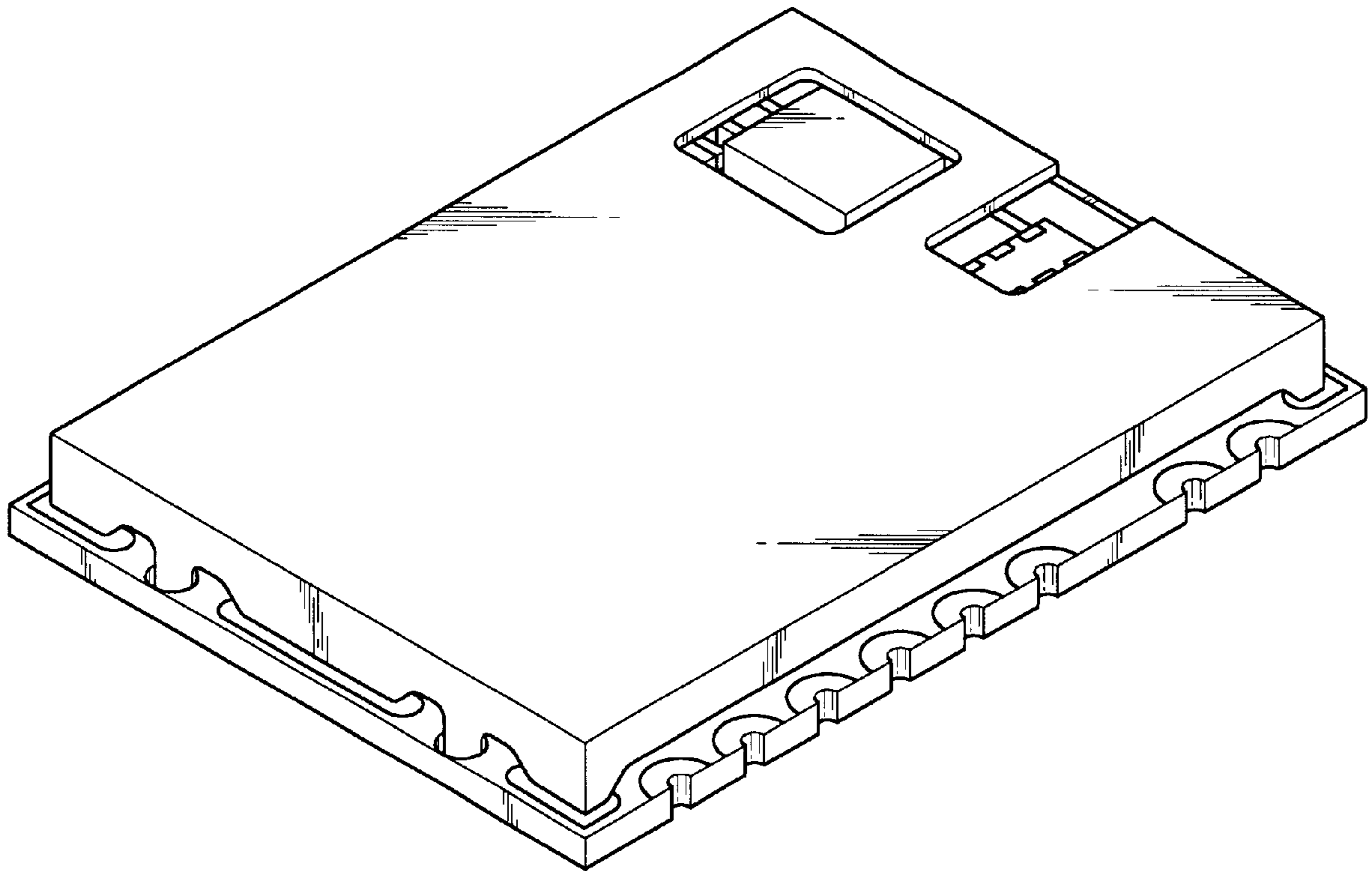


FIG. 1

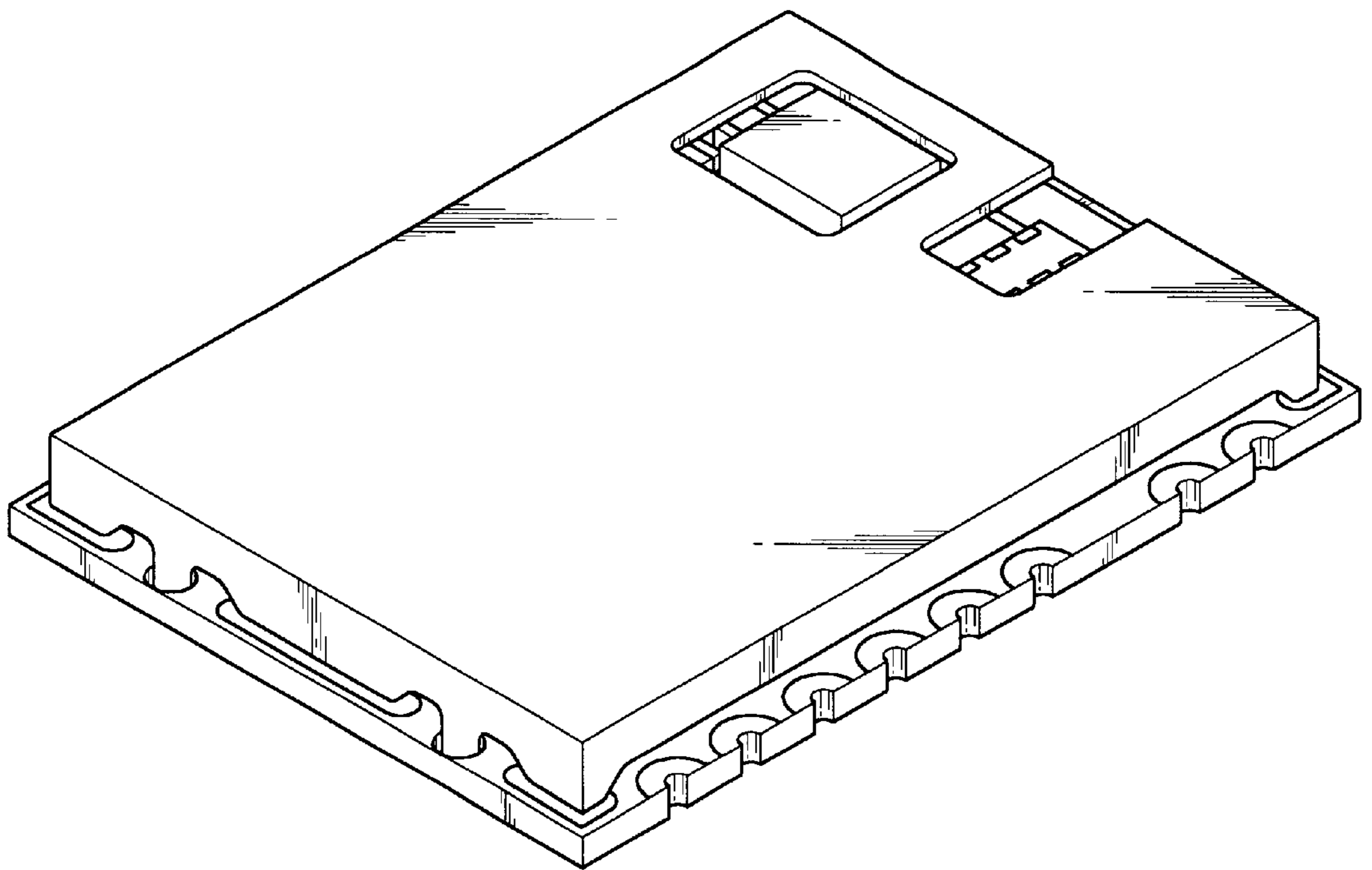


FIG. 2



FIG. 3



FIG. 4

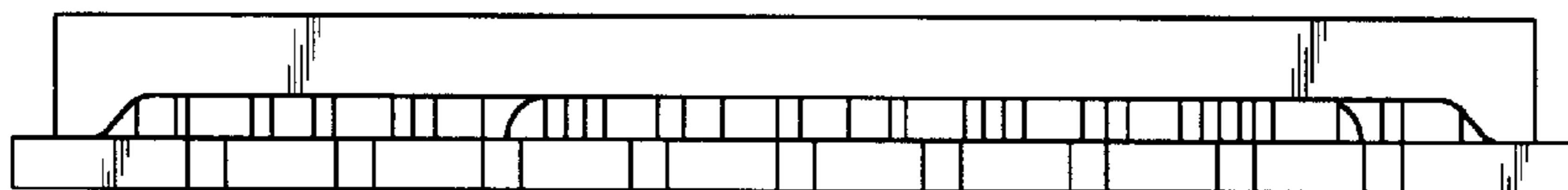


FIG. 5

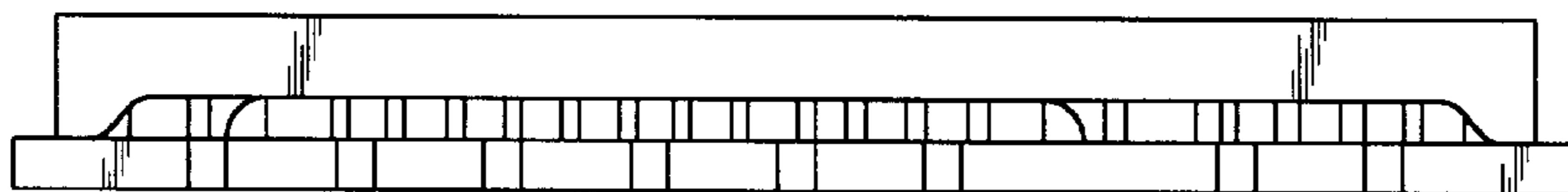


FIG. 6

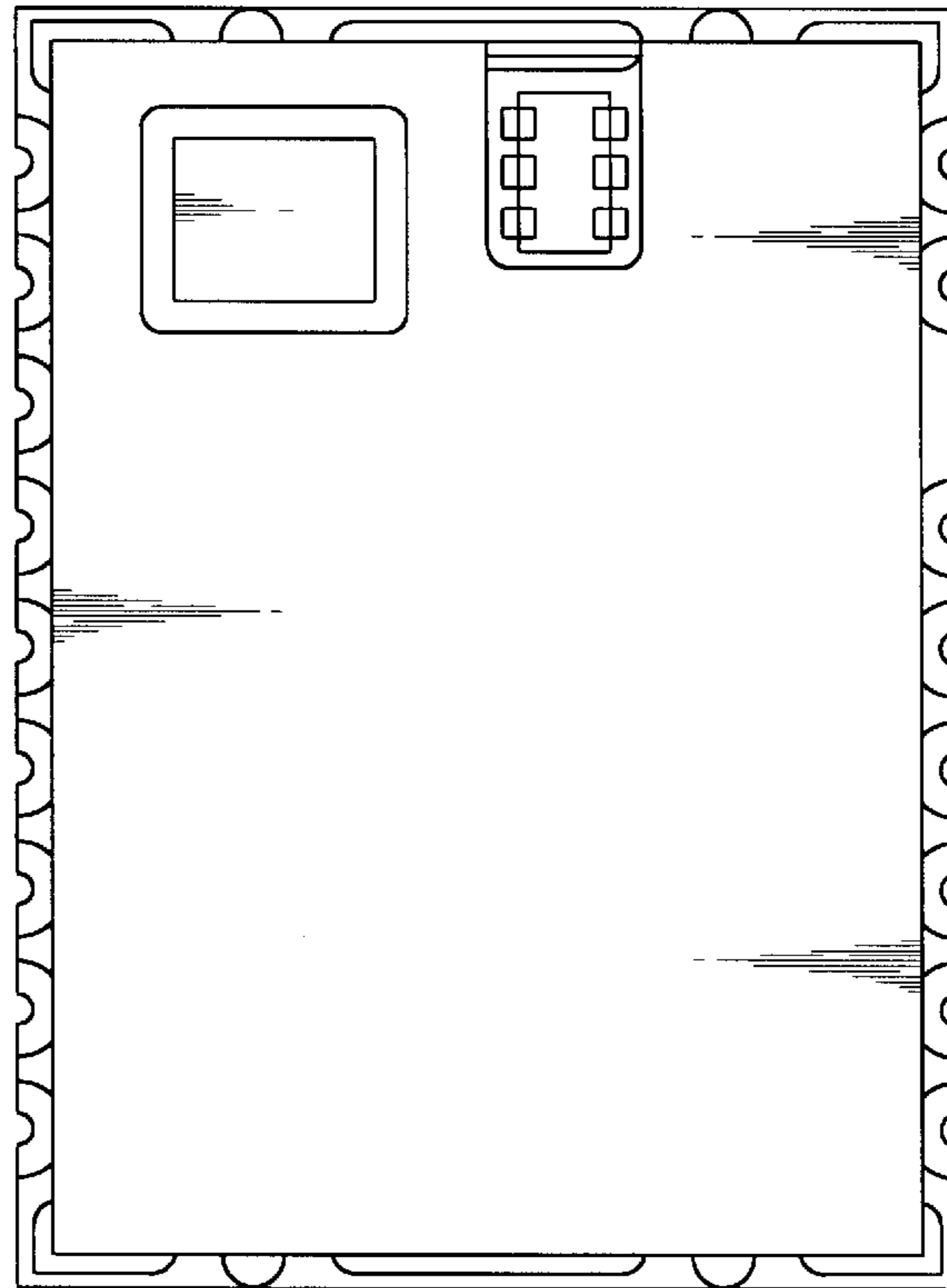


FIG. 7

