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(12) **United States Design Patent**
Hiramoto et al.

(10) **Patent No.:** **US D452,845 S**

(45) **Date of Patent:** **** *Jan. 8, 2002**

(54) **CONNECTOR FOR PRINTED CIRCUIT
BOARDS**

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(*) Notice: This patent is subject to a terminal dis-
claimer.

(57) **CLAIM**

(**) Term: **14 Years**

The ornamental design for a connector for printed circuit
boards, as shown and described.

(21) Appl. No.: **29/132,847**

DESCRIPTION

(22) Filed: **Nov. 17, 2000**

(30) **Foreign Application Priority Data**

May 19, 2000 (JP) 12-013303

(51) **LOC (7) Cl.** **13-03**

(52) **U.S. Cl.** **D13/147**

(58) **Field of Search** D13/146, 147;
439/162, 282, 374, 378, 557, 660, 680,
733.1, 953

FIG. 1 is a top plan view;
FIG. 2 is a front elevation;
FIG. 3 is a rear elevation;
FIG. 4 is a bottom plan view;
FIG. 5 is a right-side elevation;
FIG. 6 is a perspective view;
FIG. 7 is a cross section taken along the line 7—7 in FIG.
2;
FIG. 8 is a cross section taken along the line 8—8 in FIG.
2;
FIG. 9 is a cross section taken along the line 9—9 in FIG.
2; and,
FIG. 10 is an auxiliary figure of the connector shown in use,
in which a mating connector with eight electrical wire ends
secured thereto is fitted in the subject article.

(56) **References Cited**

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The broken lines showing the mating connector and the
electrical wire ends in FIG. 10 are included for the purpose
of illustrating environmental structure only and form no part
of the claimed design.

1 Claim, 2 Drawing Sheets

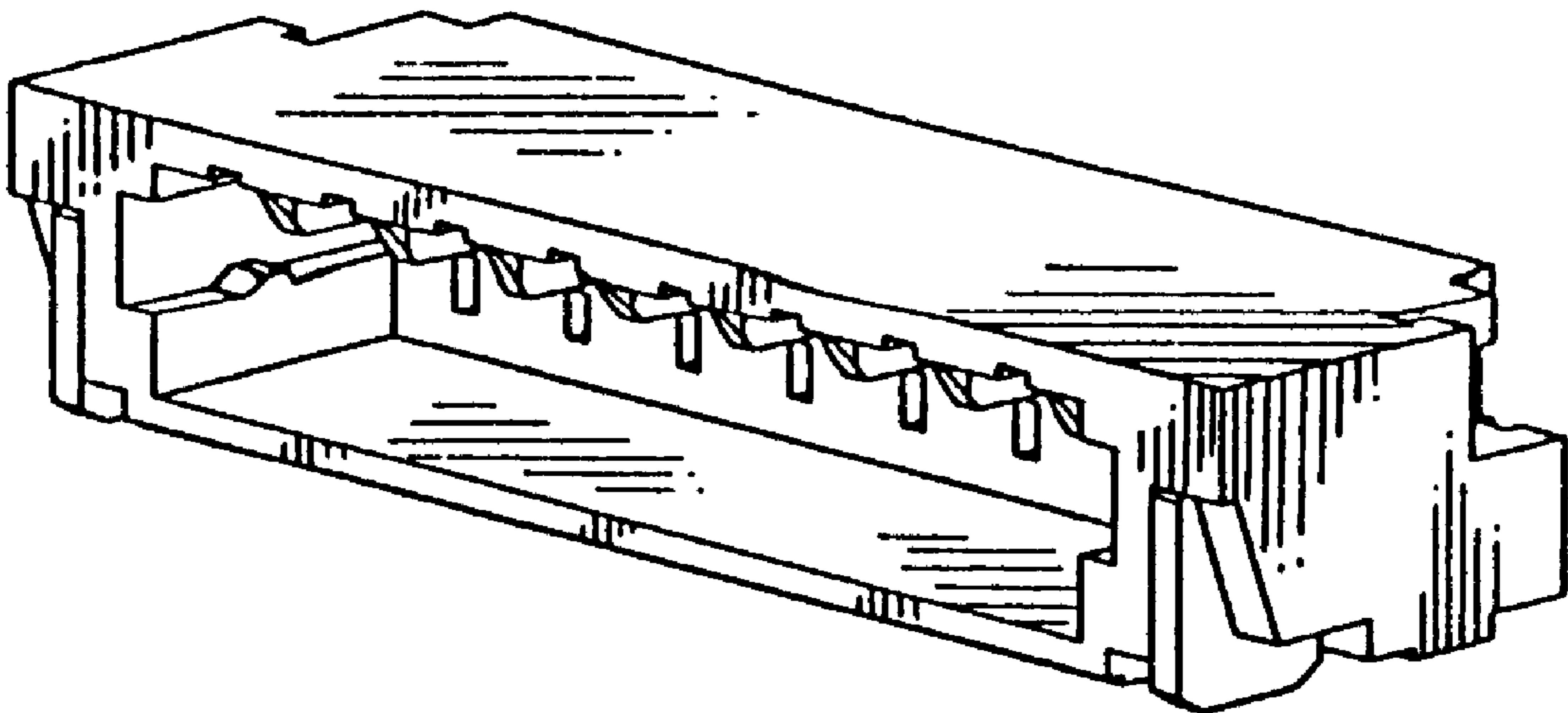


Fig. 1

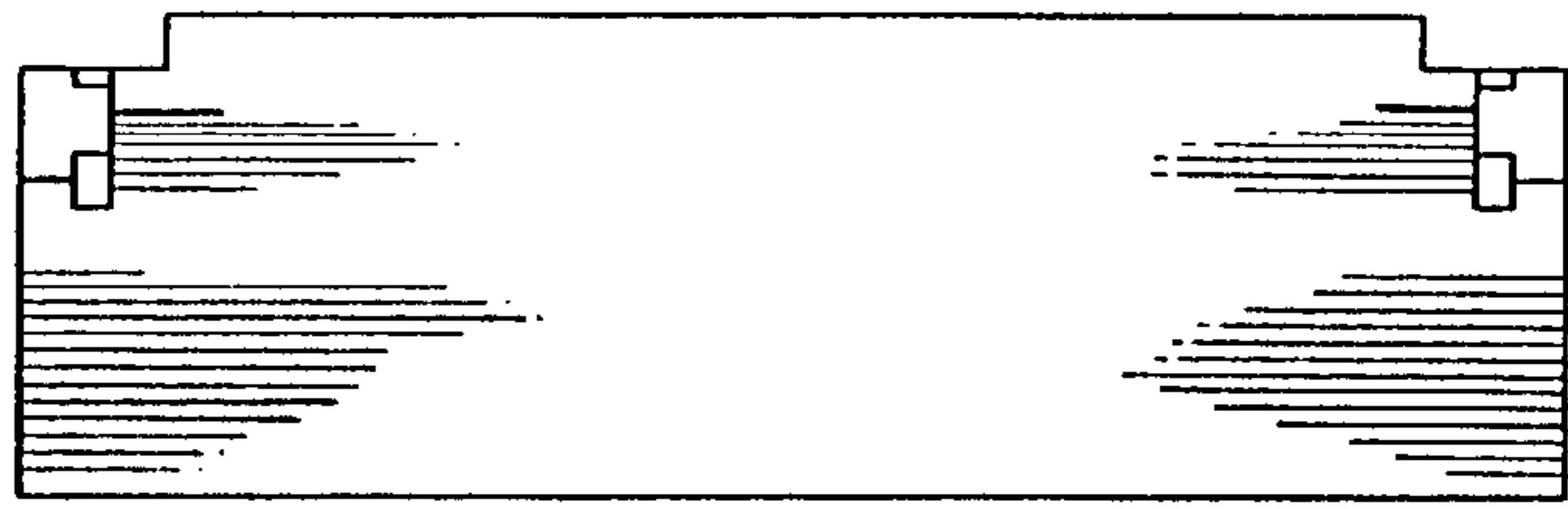


Fig. 2

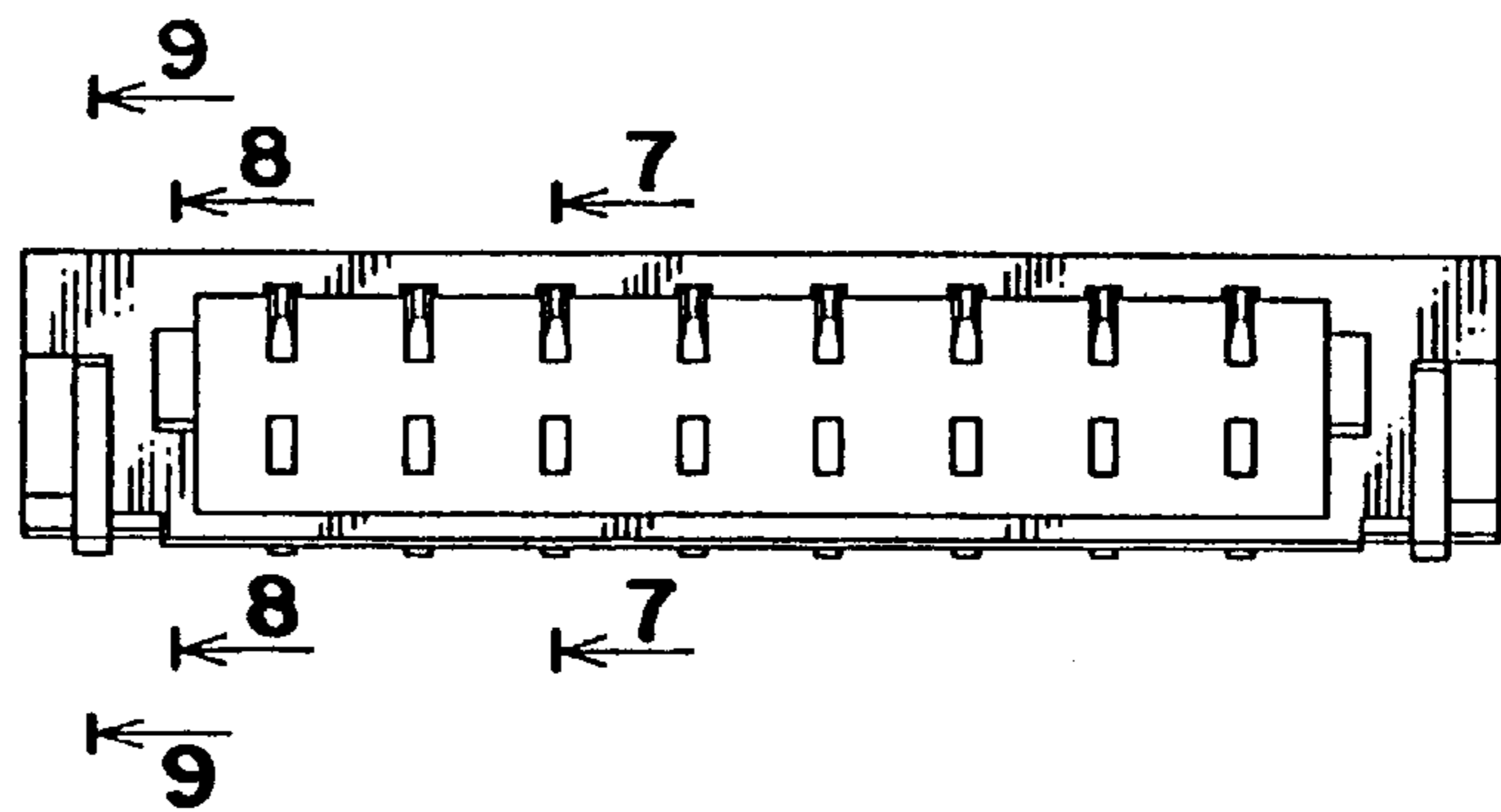


Fig. 3

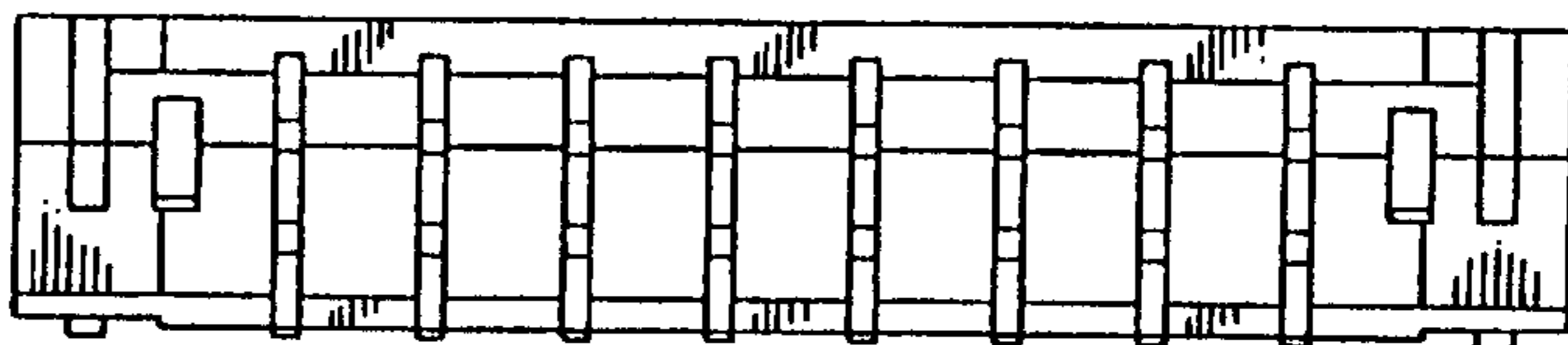


Fig. 4

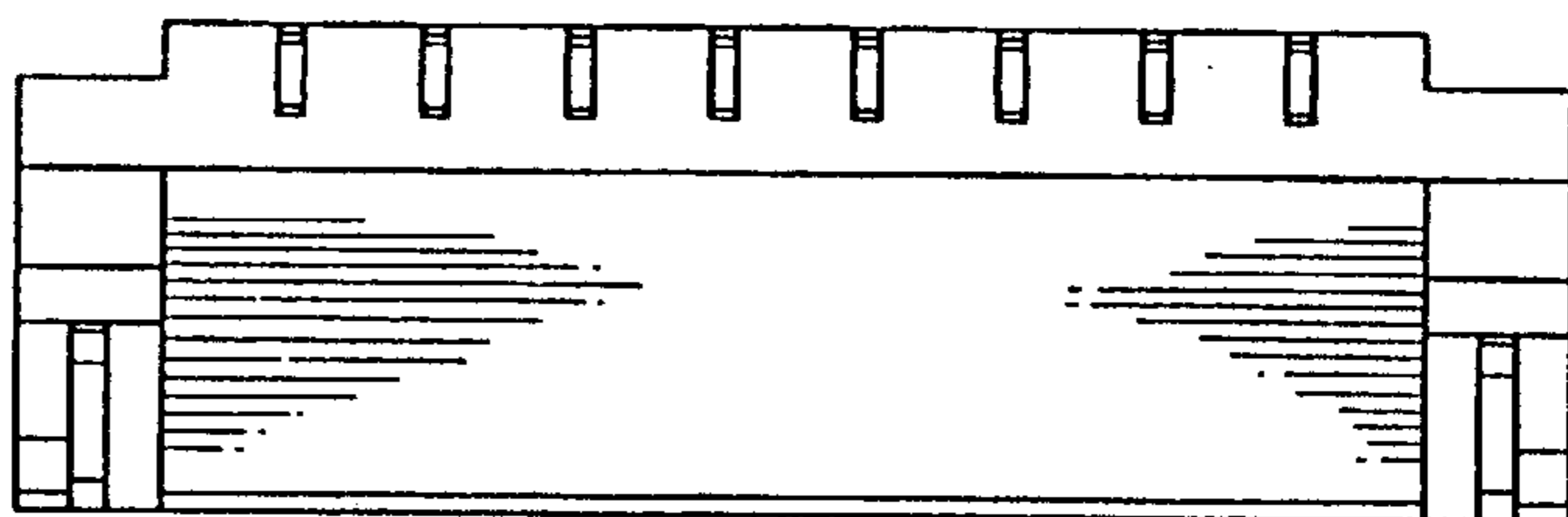


Fig. 5

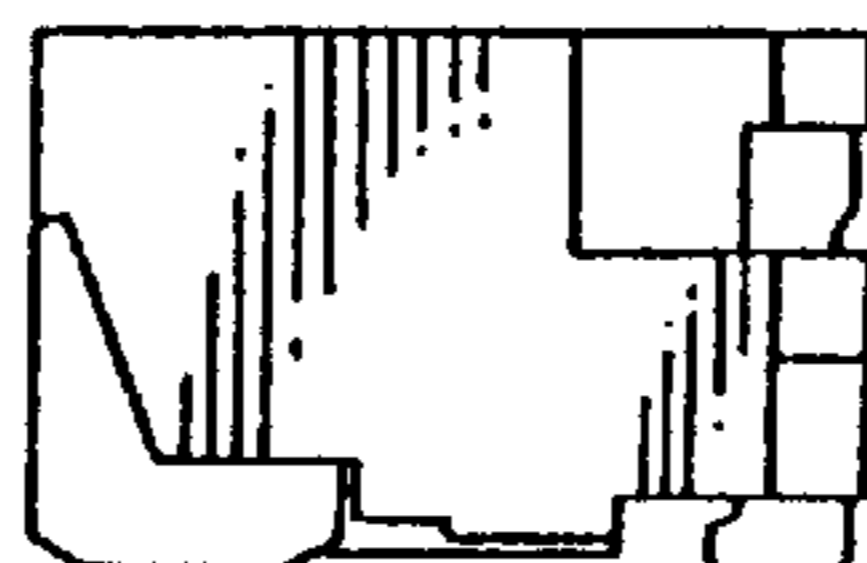


Fig. 6

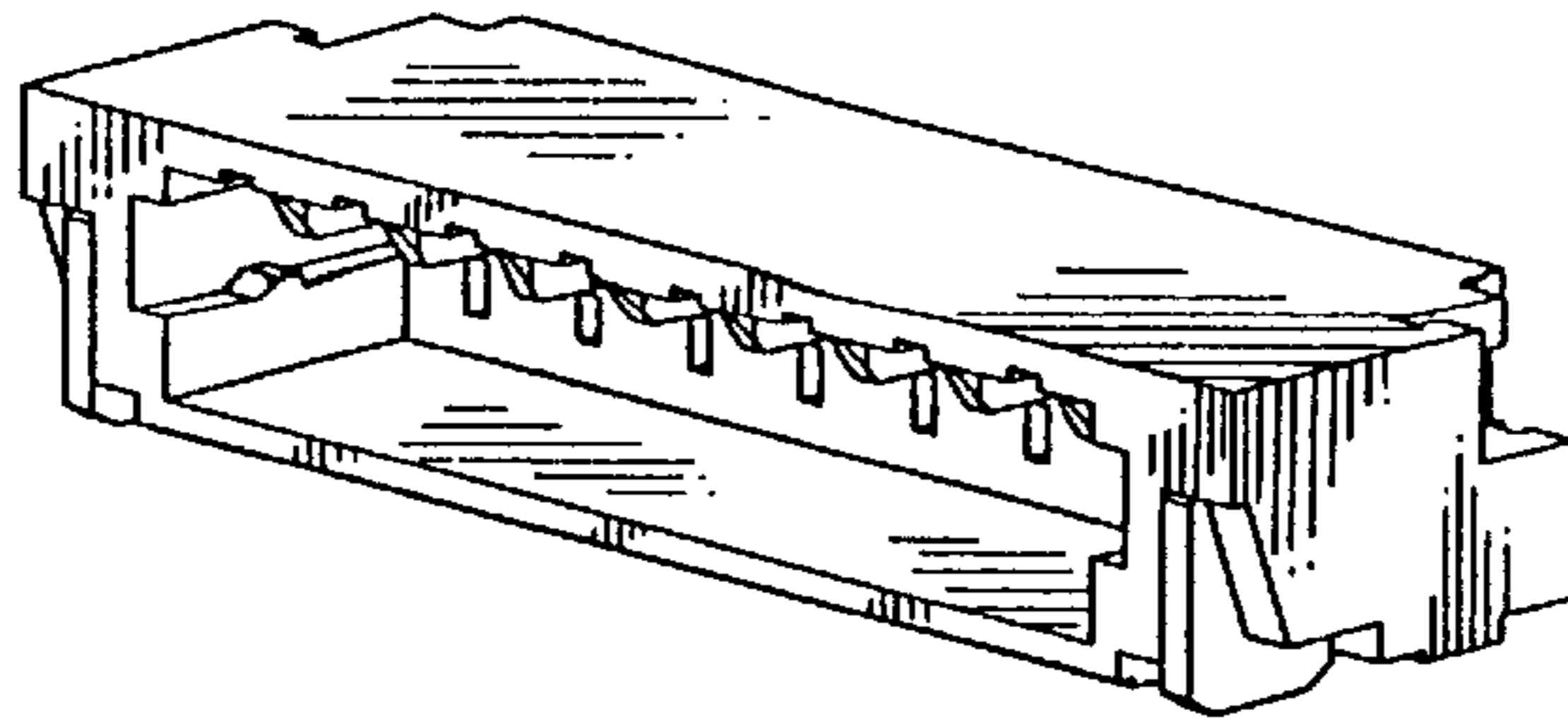


Fig. 7

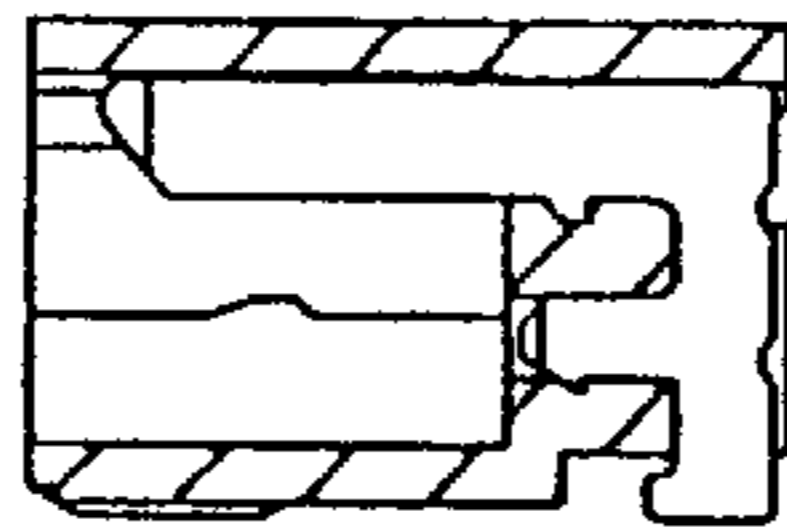


Fig. 8

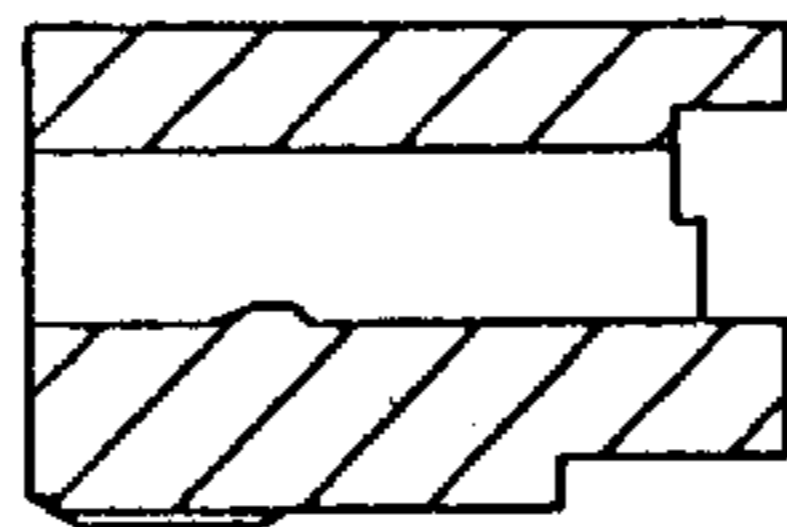


Fig. 9

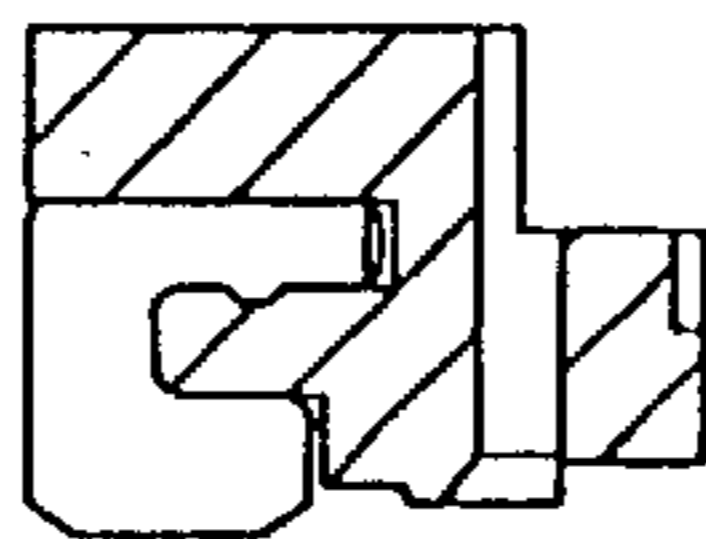


Fig. 10

