



US00D449308B1

(12) **United States Design Patent**
Iwasaki et al.

(10) **Patent No.:** **US D449,308 S**

(45) **Date of Patent:** **** Oct. 16, 2001**

(54) **PARTIALLY TRANSPARENT IC CARD**

OTHER PUBLICATIONS

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Toshiba MOS Digital Integrated Circuit Silicon Gate CMOS 128 Mbit (16M×8bit) CMOS NAND E²PROM (16M Byte SmartMedia™), Toshiba, Nov. 6, 1998.

(73) Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki (JP)

Toshiba MOS Digital Integrated Circuit Silicon Gate CMOS 64 Mbit (8M×8bit) CMOS NAND E²PROM (8M byte SmartMedia™), Toshiba, Nov. 6, 1998.

(**) Term: **14 Years**

* cited by examiner

(21) Appl. No.: **29/114,441**

Primary Examiner—M. H. Tung

(22) Filed: **Nov. 26, 1999**

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(51) **LOC (7) Cl.** **14-02**

(52) **U.S. Cl.** **D14/478**

(58) **Field of Search** D14/435-8, 478-80; 361/737-6, 752, 686; 257/678-9; 40/124.01; 283/75-6, 901; 235/487-95, 441-3, 375; 174/52.1; 439/135, 140, 76.1; 360/60, 129, 132-3, 135, 97.01-99.12

(57) **CLAIM**

The ornamental design for partially transparent IC card, as shown and described.

DESCRIPTION

FIG. 1 is a enlarged top, front and right side perspective view of partially transparent IC card showing our new design; FIG. 2 is a top plan view thereof; FIG. 3 is a front elevational view thereof; FIG. 4 is a rear elevational view thereof; FIG. 5 is a right side elevational view thereof; FIG. 6 is a left side elevational view thereof; FIG. 7 is a bottom plan view thereof; and, FIG. 8 is a greatly enlarged cross-sectional view thereof taken along line 8—8 in FIG. 2.

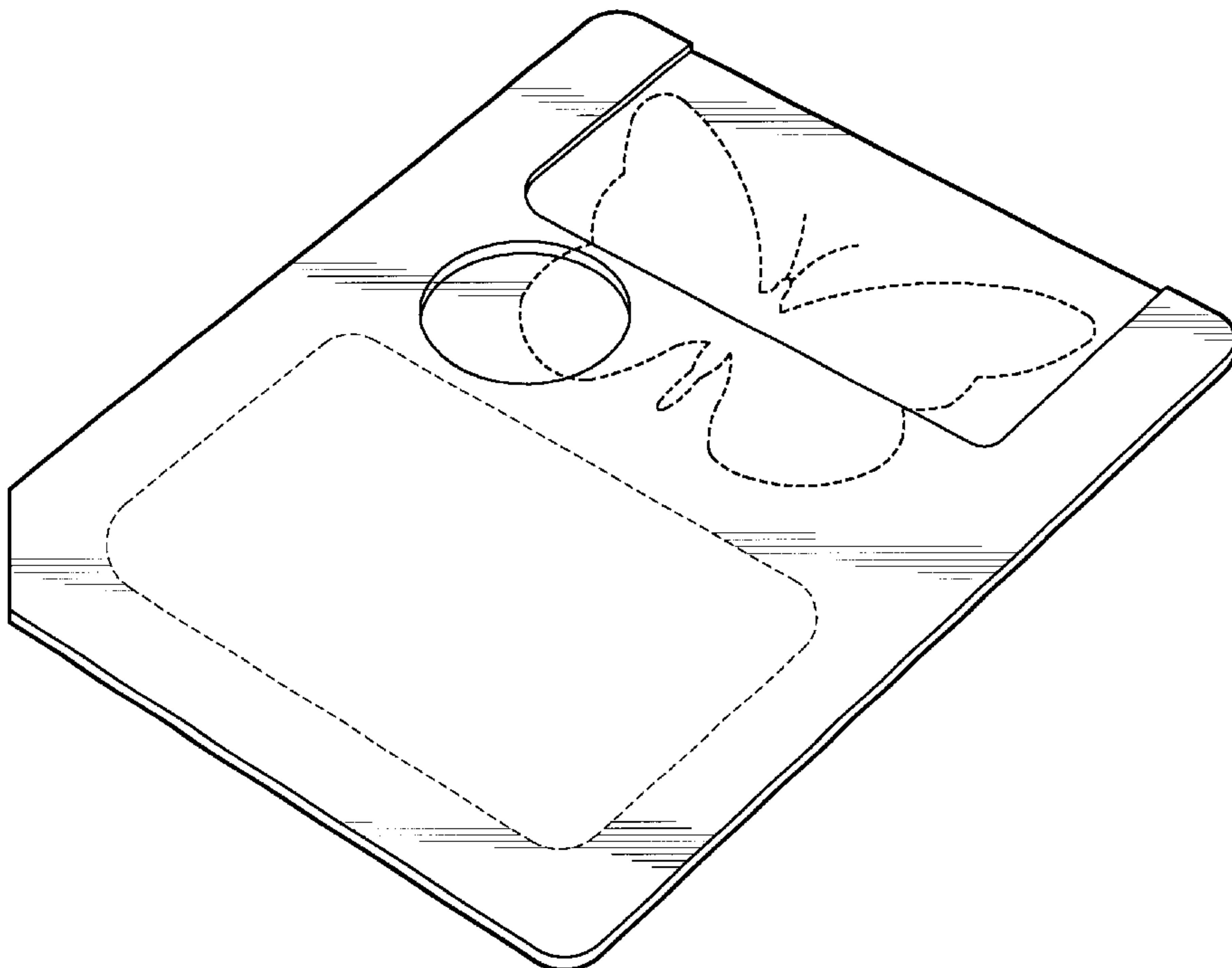
The phantom line showing in the drawings is for illustrative purposes only and forms no part of the claimed design.

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1 Claim, 3 Drawing Sheets



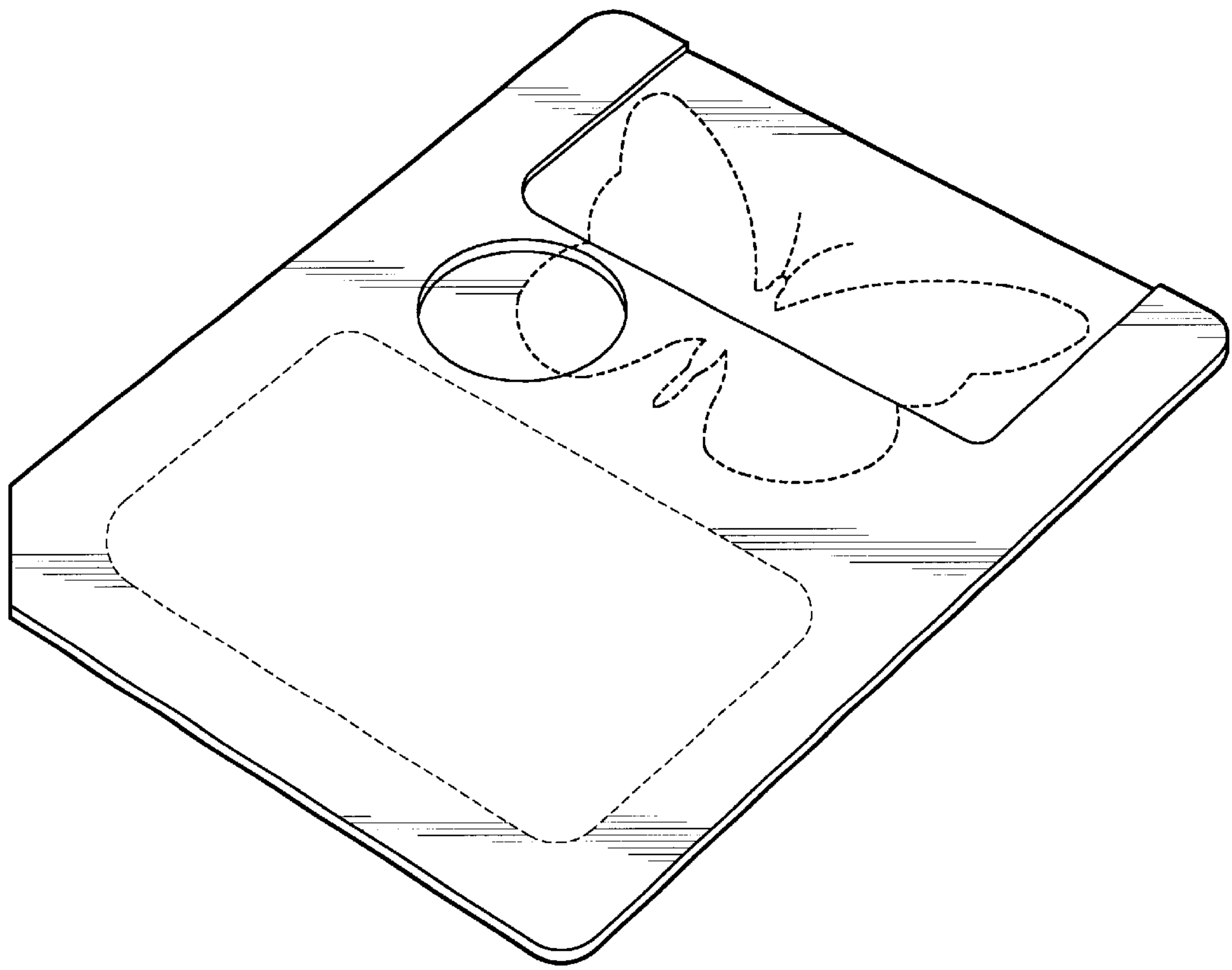


FIG. 1



FIG. 4

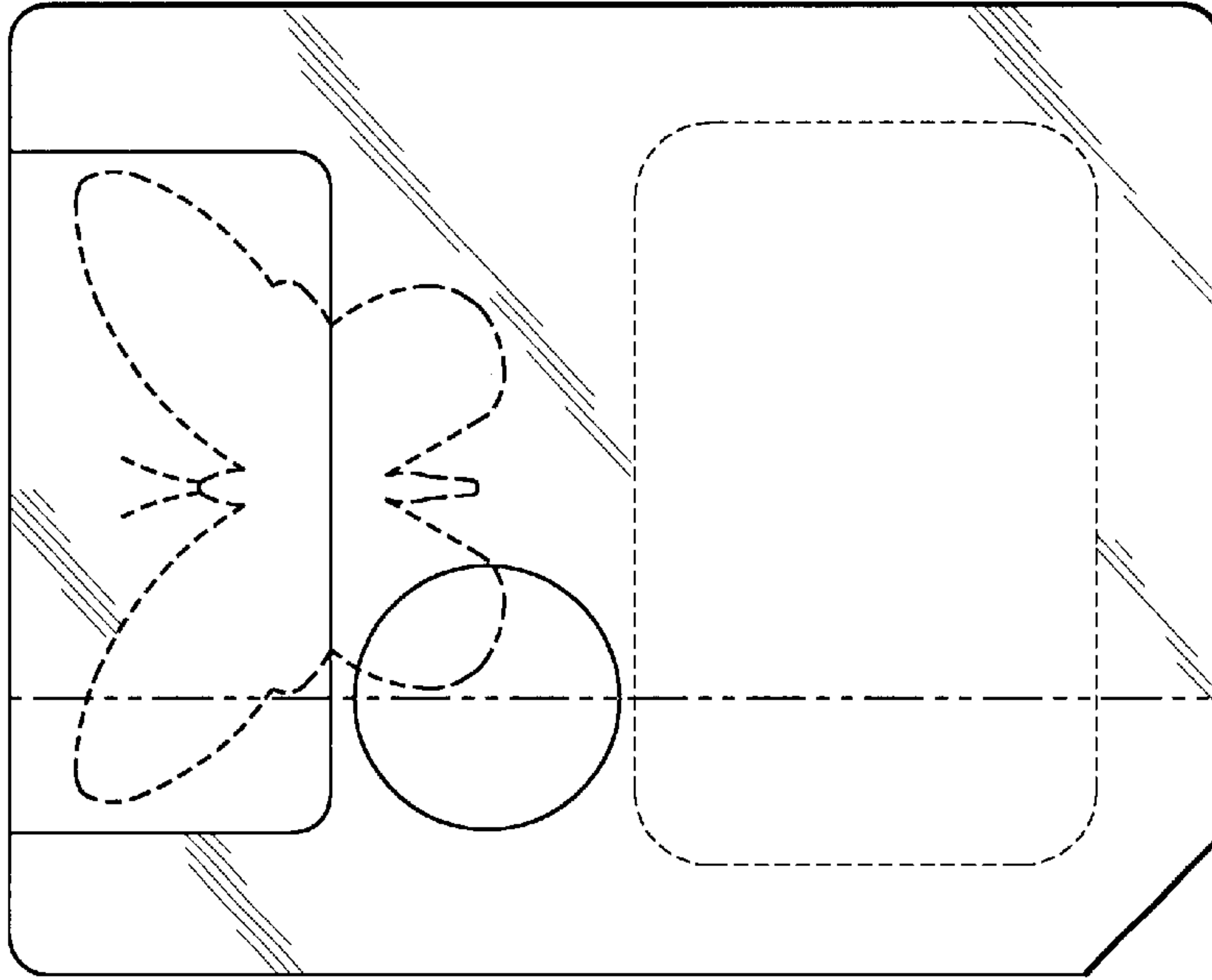


FIG. 2



FIG. 3

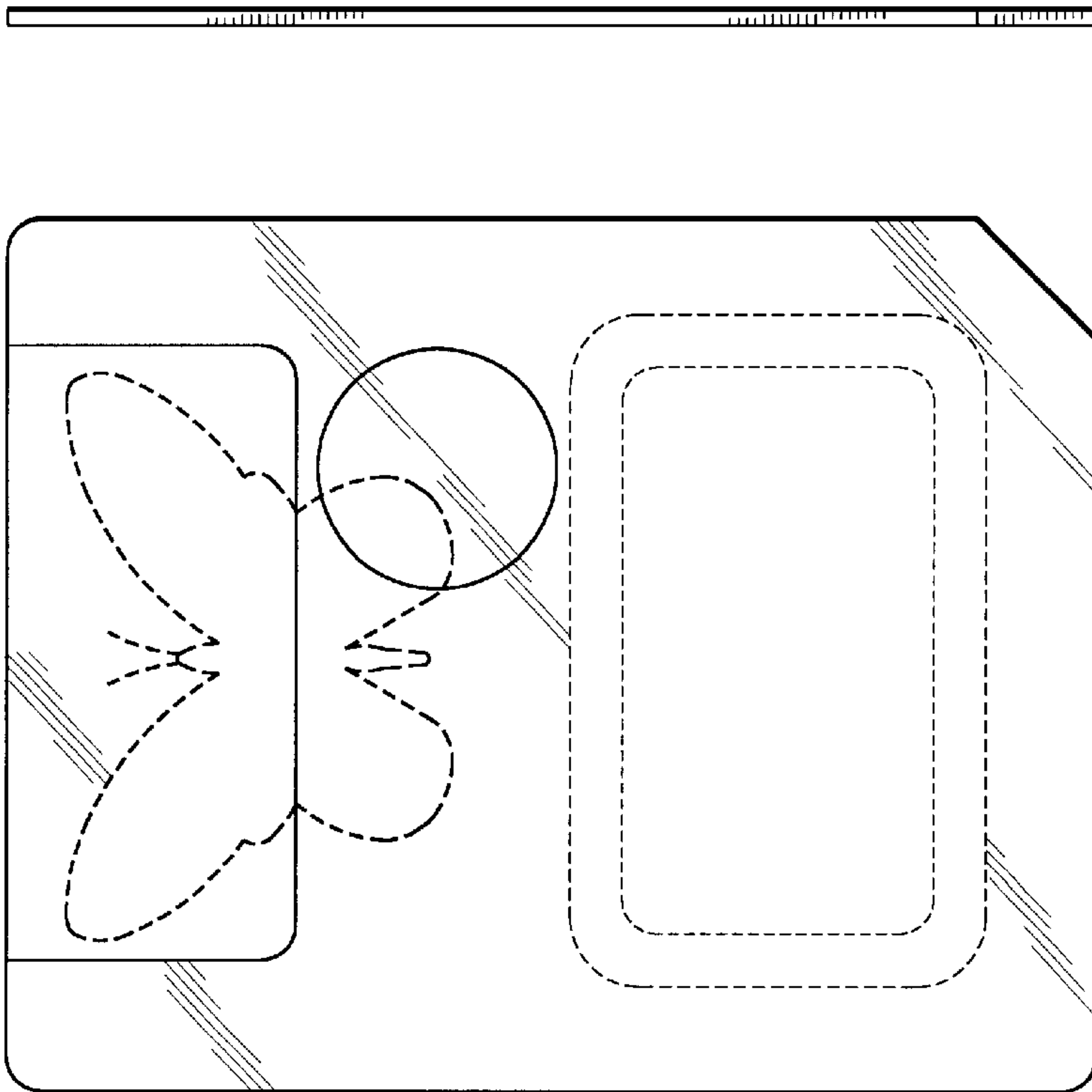


FIG. 6

FIG. 7



FIG. 5



FIG. 8