



US00D443556S

(12) **United States Design Patent** (10) **Patent No.:** **US D443,556 S**
Sinha et al. (45) **Date of Patent:** **** Jun. 12, 2001**

(54) **MINIATURE TABLET**

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(**) Term: **14 Years**

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(51) **LOC (7) Cl.** **11-01**

(52) **U.S. Cl.** **D11/96; D11/80**

(58) **Field of Search** **D11/1, 2, 40, 43-44, D11/48-49, 78, 79, 80-82, 95, 99, 100, 101, 104, 107, 116, 62, 54, 102, 96; 63/13, 14.1, 23**

(56) **References Cited**

U.S. PATENT DOCUMENTS

- D. 74,368 * 2/1928 Hargis D11/96
- D. 329,402 * 9/1992 Zears D11/96
- D. 418,080 * 12/1999 Oak D11/40

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(57) **CLAIM**

The ornamental design for miniature tablet, as shown and described.

DESCRIPTION

The depicted miniature tablet is comprised of an ornamental design on a substrate. Semiconductor processes may be used to create the ornamental design on, for example, a semiconductor substrate. The ornamental design comprises columns of text overlaid with a graphic. As geometries of the text in the columns are so minute, the figures cannot accurately portray the content of this text.

This application is being filed concurrently with related U.S. patent applications: Ser. No. 60/154,401, provisional patent entitled “A VLSI-based System for Durable High-density Information Storage”; Ser. No. 29/110,989, design patent entitled “Miniature Tablet”; U.S. Pat. No. Des. 438,814, design patent entitled “Miniature Tablet”; Ser. No. 29/110,991, design patent entitled “Miniature Tablet”; and, Ser. No. 29/110,964, design patent entitled “Miniature Tablet”.

FIG. 1 is a front-top perspective view of a miniature tablet showing my new design;

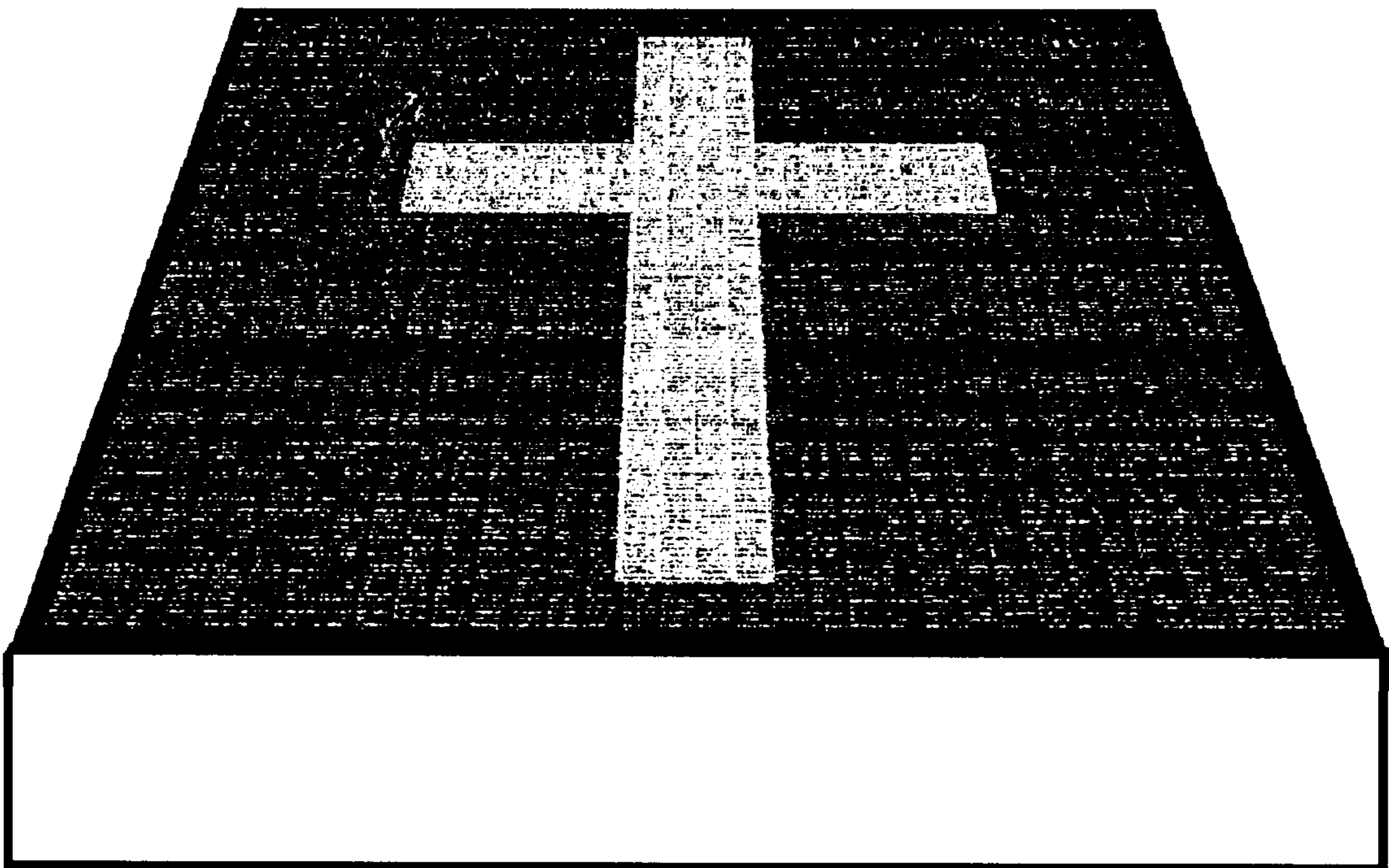
FIG. 2 is a top plan view thereof;

FIG. 3 is a front elevational view, the rear elevational view being a mirror image thereof;

FIG. 4 is a right side elevational view, the left side elevational view being a mirror image thereof; and,

FIG. 5 is a bottom plan view thereof.

1 Claim, 2 Drawing Sheets



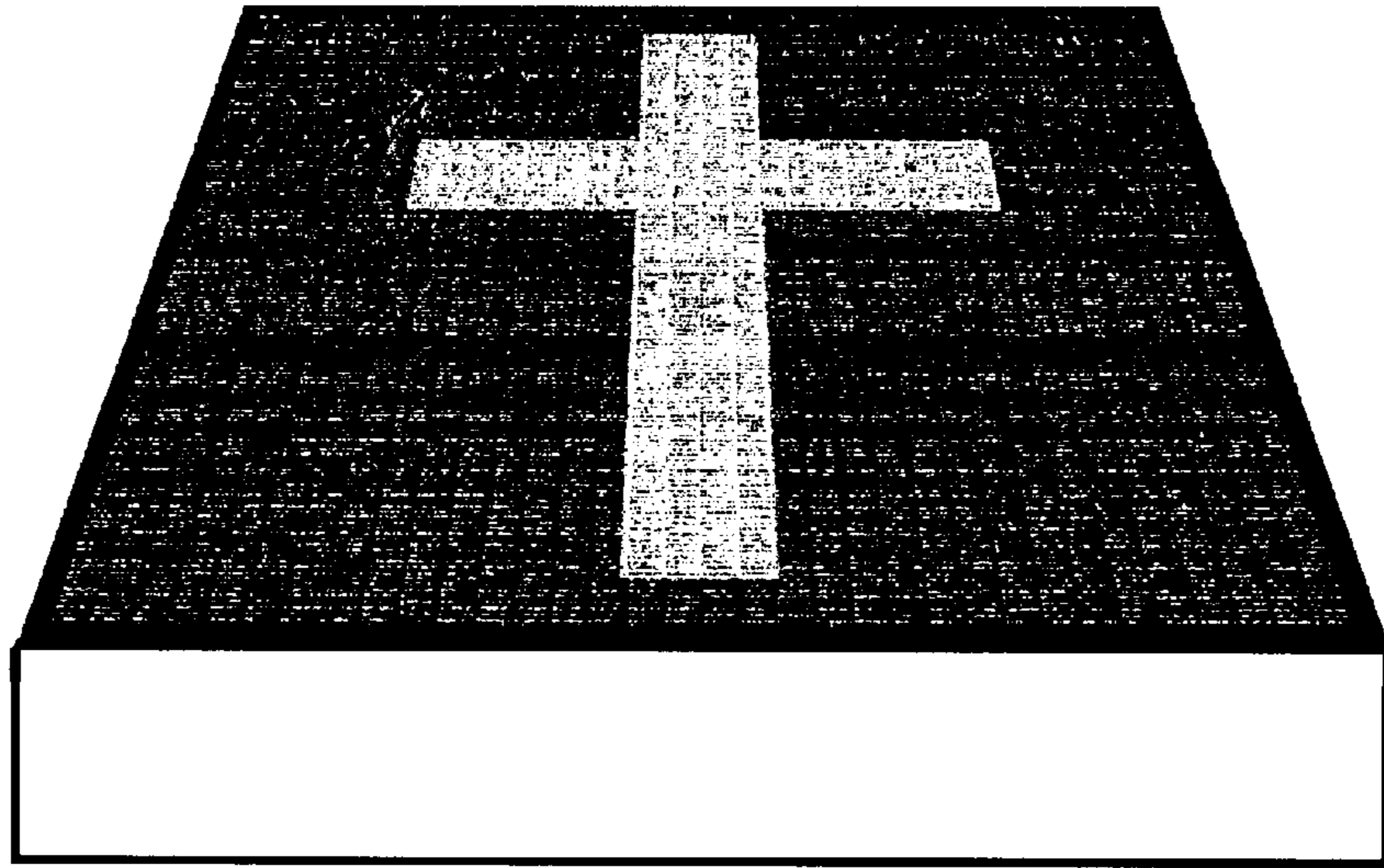


Fig. 1

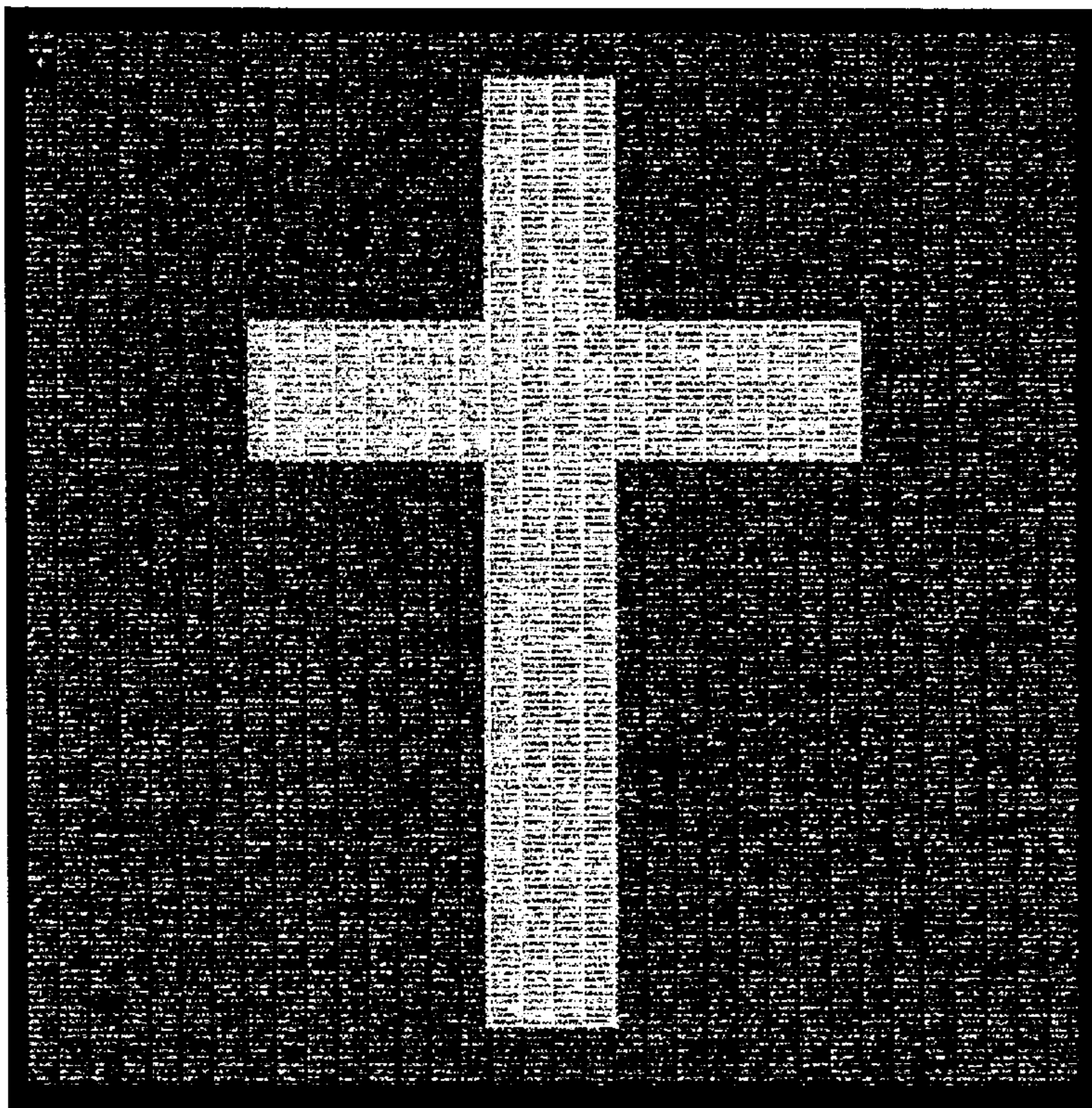


Fig. 2



Fig. 3



Fig. 4

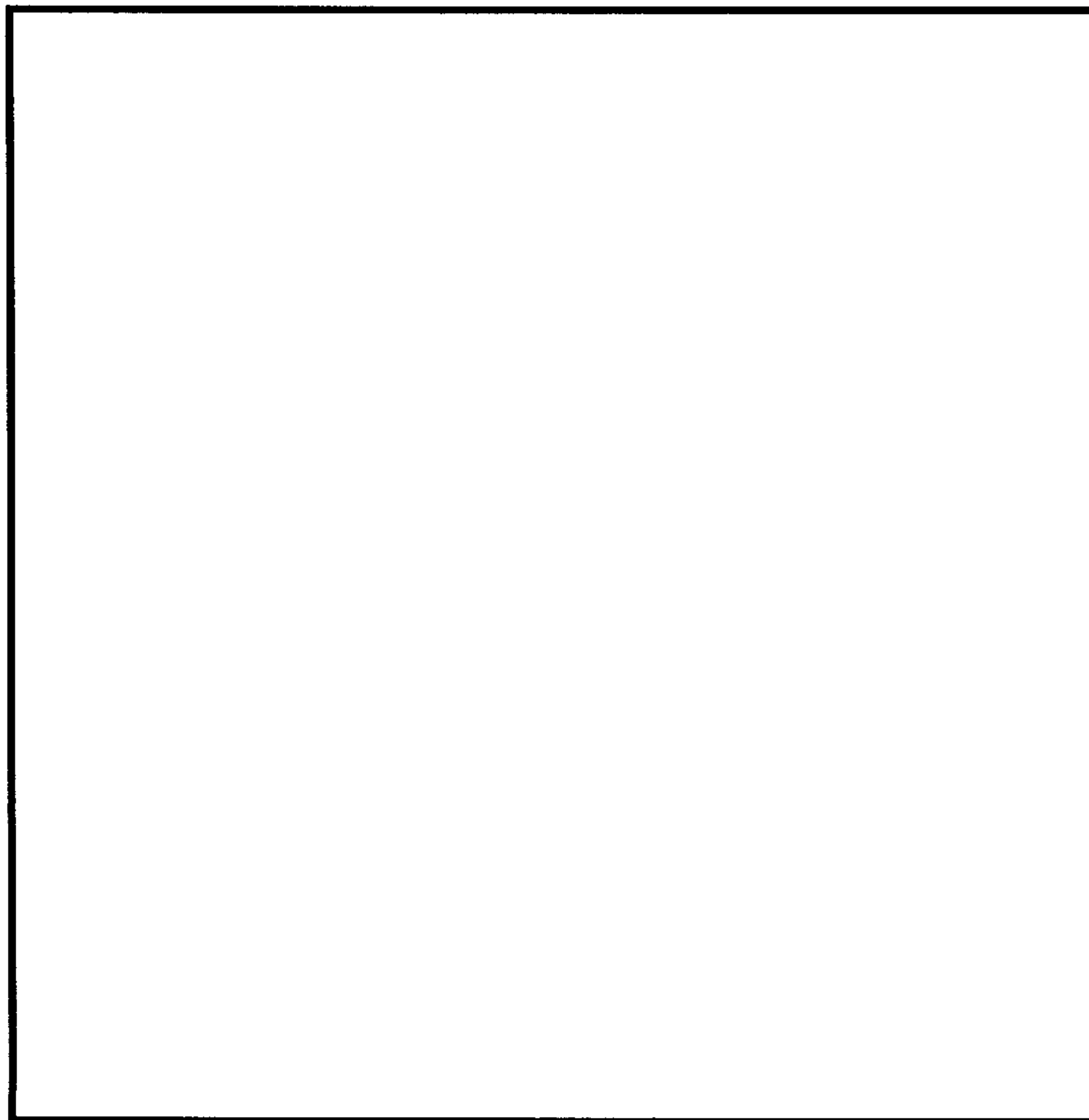


Fig. 5