US00D443253S

(12) **United States Design Patent**
Nagase et al.

(10) **Patent No.: US D443,253 S**
(45) **Date of Patent: ** Jun. 5, 2001**

(54) **TRANSISTOR SUBSTRATE**

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(**) Term: **14 Years**

(21) Appl. No.: **29/116,954**

(22) Filed: **Jan. 13, 2000**

(30) **Foreign Application Priority Data**

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Jul. 14, 1999	(JP)	11-18963
Jul. 14, 1999	(JP)	11-18964

(51) **LOC (7) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Search** D13/182, 184, D13/199; 257/48, 690, 692, 693, 697; 361/395; 324/158.1

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(74) *Attorney, Agent, or Firm*—Morgan & Finnegan, LLP

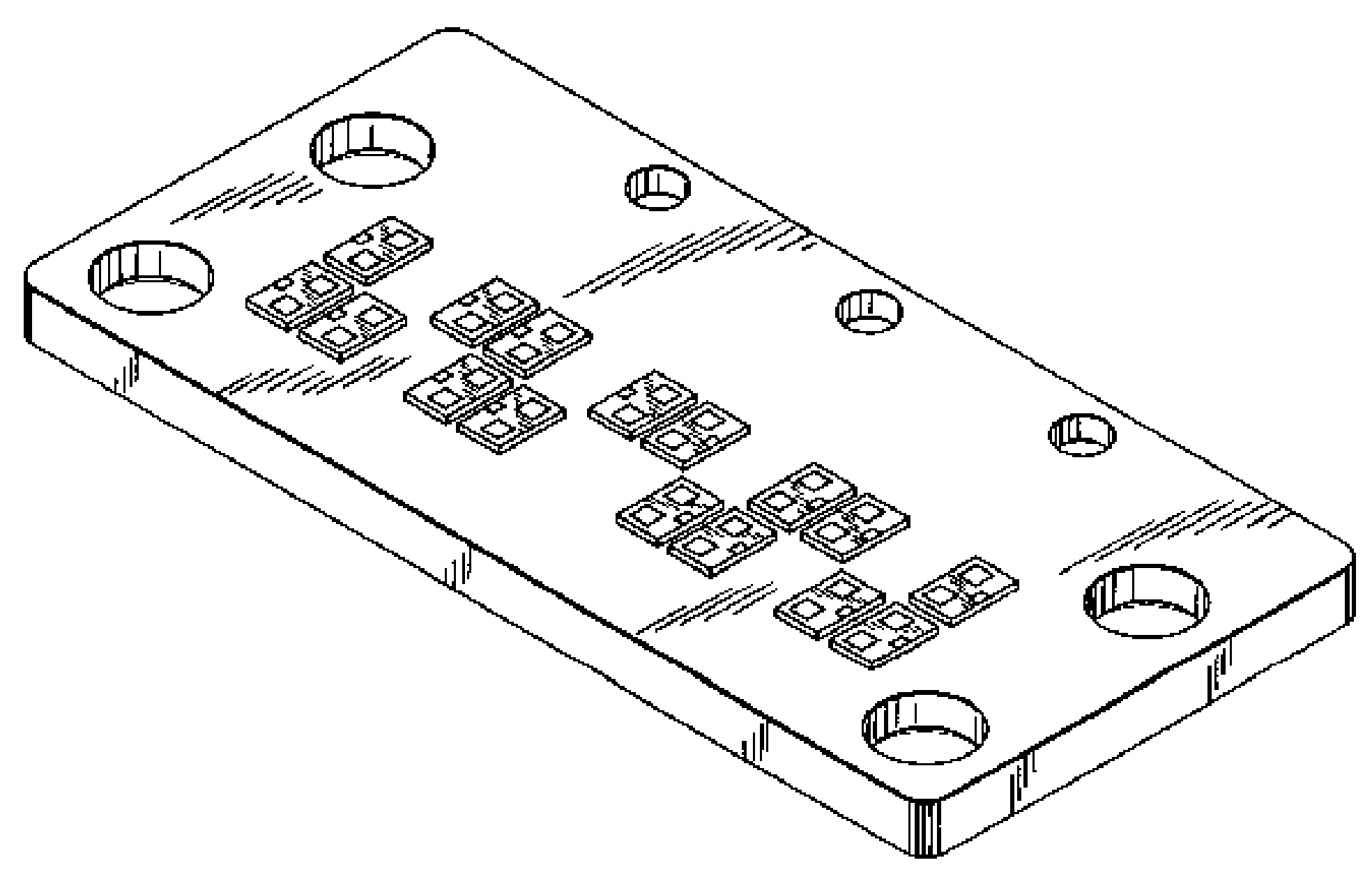
(57) **CLAIM**

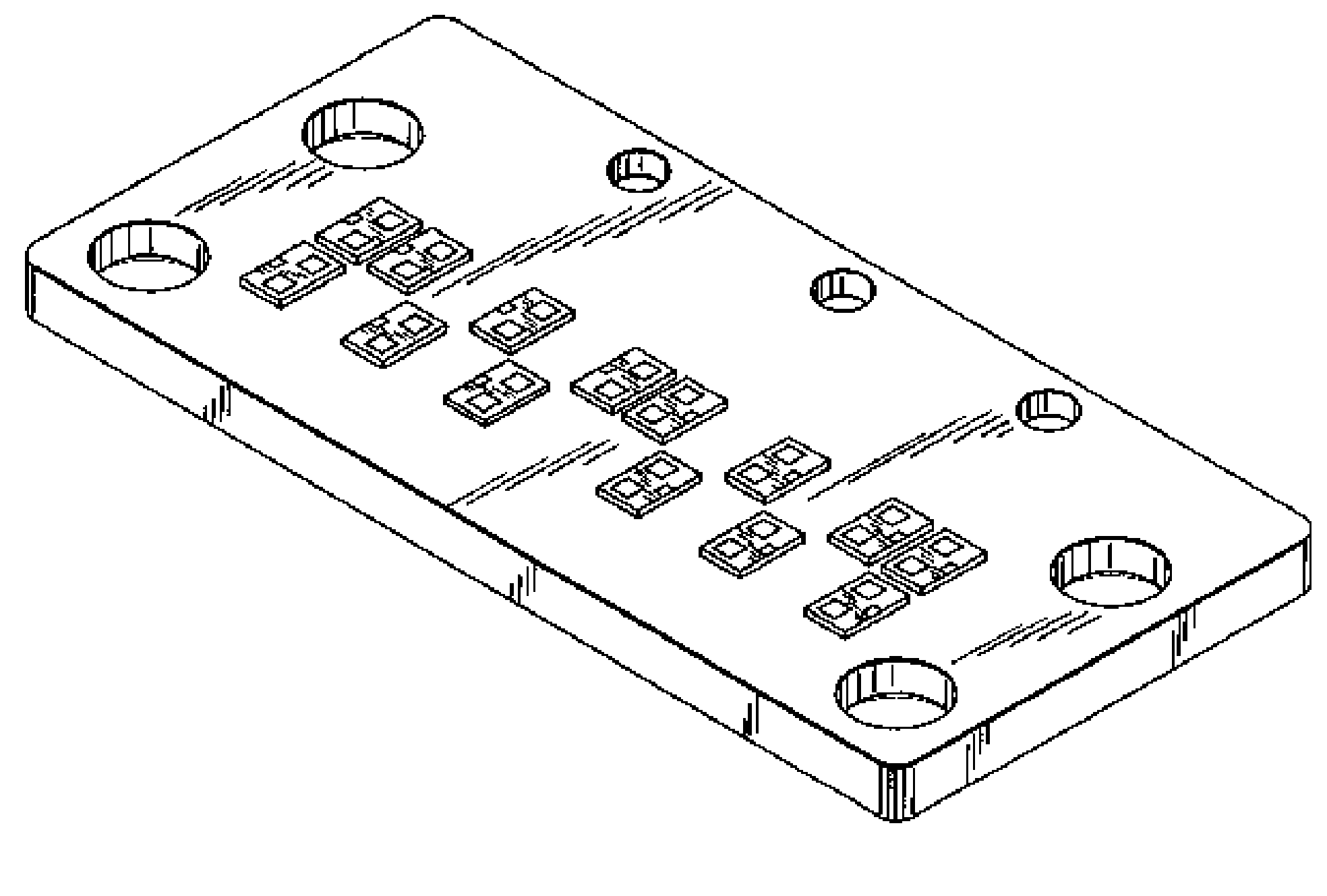
The ornamental design for a transistor substrate, as shown and described.

DESCRIPTION

FIG. **1** is a front elevational view showing a transistor substrate according to a first embodiment of the present invention;
FIG. **2** is a rear elevational view of the substrate of FIG. **1**;
FIG. **3** is a top plan view of the substrate of FIG. **1**;
FIG. **4** is a bottom plan view of the substrate of FIG. **1**;
FIG. **5** is a right side elevational view of the substrate of FIG. **1**, the left side elevational view being a mirror image of the right side elevational view;
FIG. **6** is a top front perspective view of the substrate of FIG. **1**;
FIG. **7** is a top plan view showing a transistor substrate according to a second embodiment of the present invention, wherein the front elevational view, the rear elevational view, the bottom plan view, the right side elevational view and the left side elevational view are identical with those of the first embodiment;
FIG. **8** is a top front perspective view of the substrate of FIG. **7**;
FIG. **9** is a top plan view showing a transistor substrate according to a third embodiment of the present invention, wherein the front elevational view, the rear elevational view, the bottom plan view, the right side elevational view and the left side elevational view are identical with those of the first embodiment;
FIG. **10** is a top front perspective view of the substrate of FIG. **9**;
FIG. **11** is a top plan view showing a transistor substrate according to a fourth embodiment of the present invention, wherein the front elevational view, the rear elevational view, the bottom plan view, the right side elevational view and the left side elevational view are identical with those of the first embodiment; and,
FIG. **12** is a top front perspective view of the substrate of FIG. **11**.

1 Claim, 5 Drawing Sheets





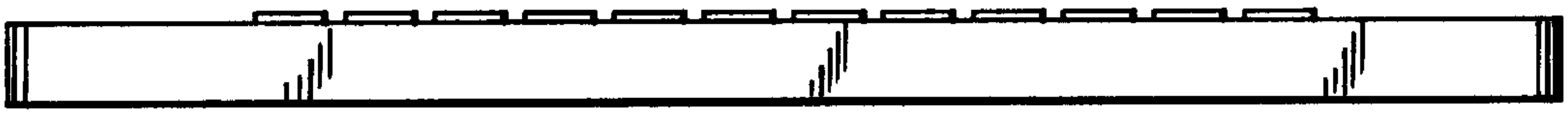


FIG. 1

FIG. 2

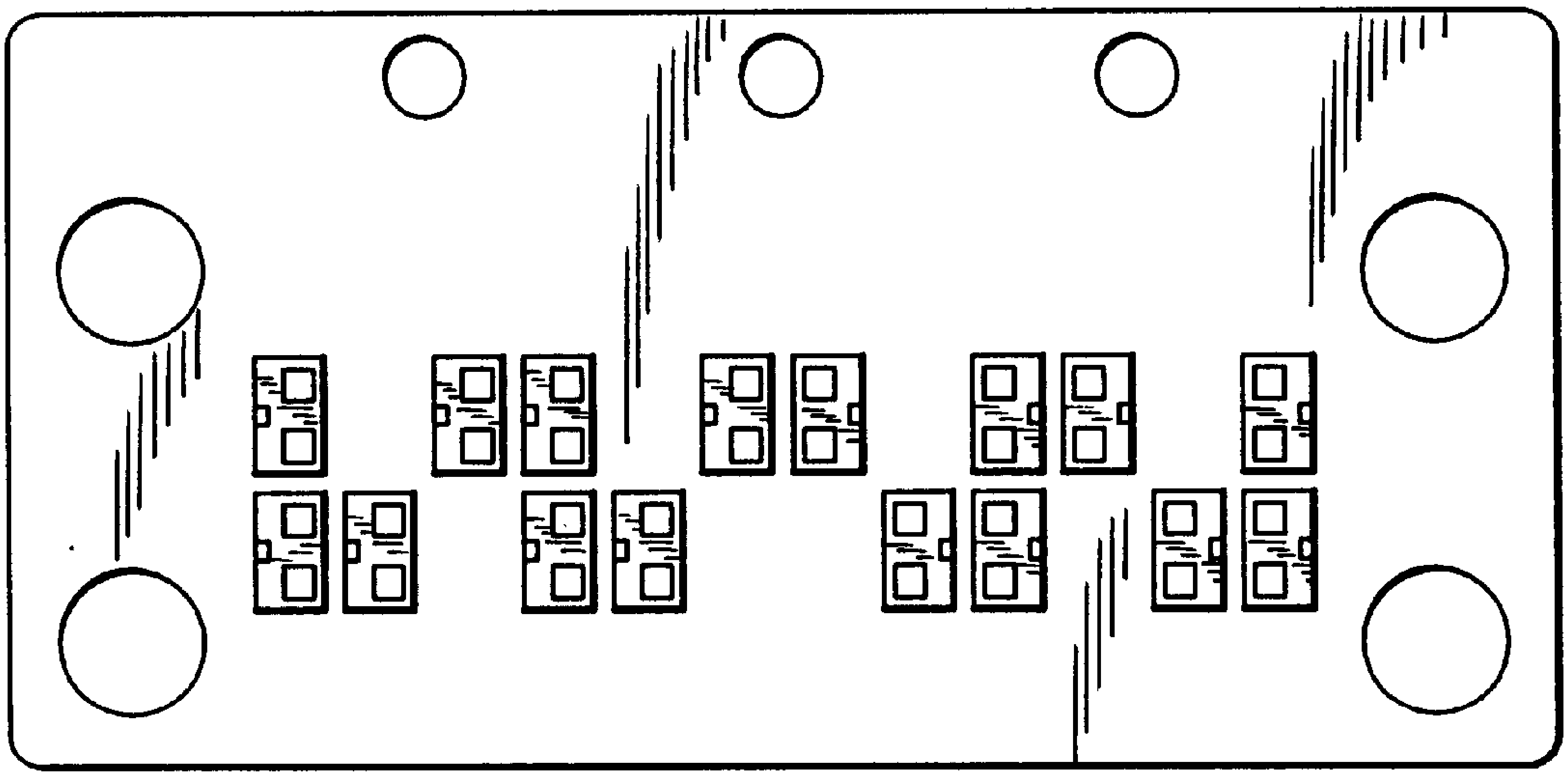


FIG. 3

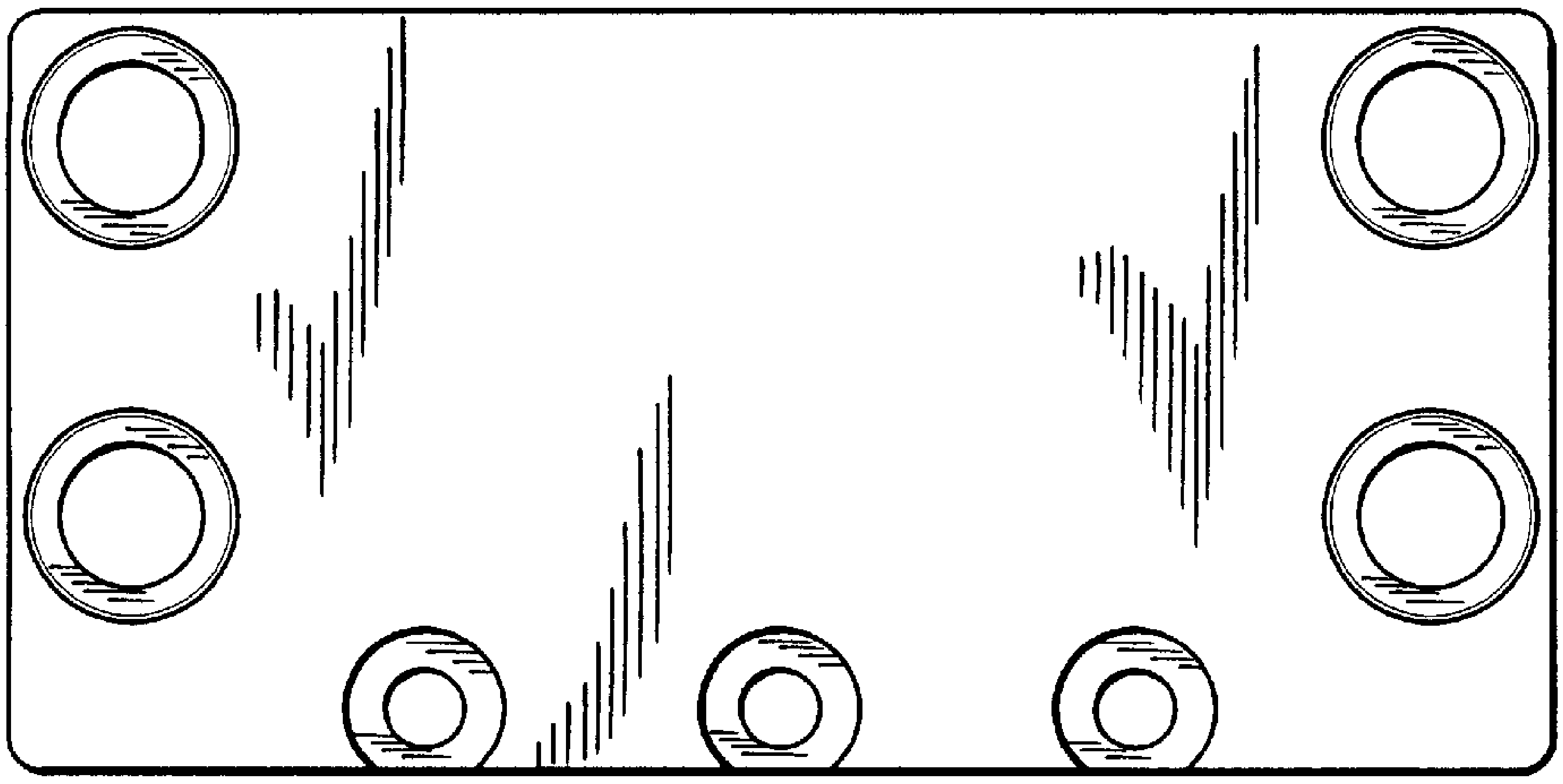


FIG.4

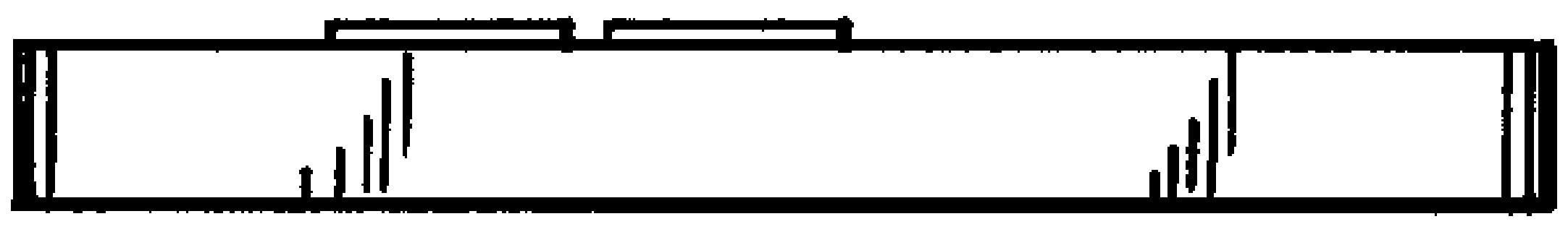


FIG.5

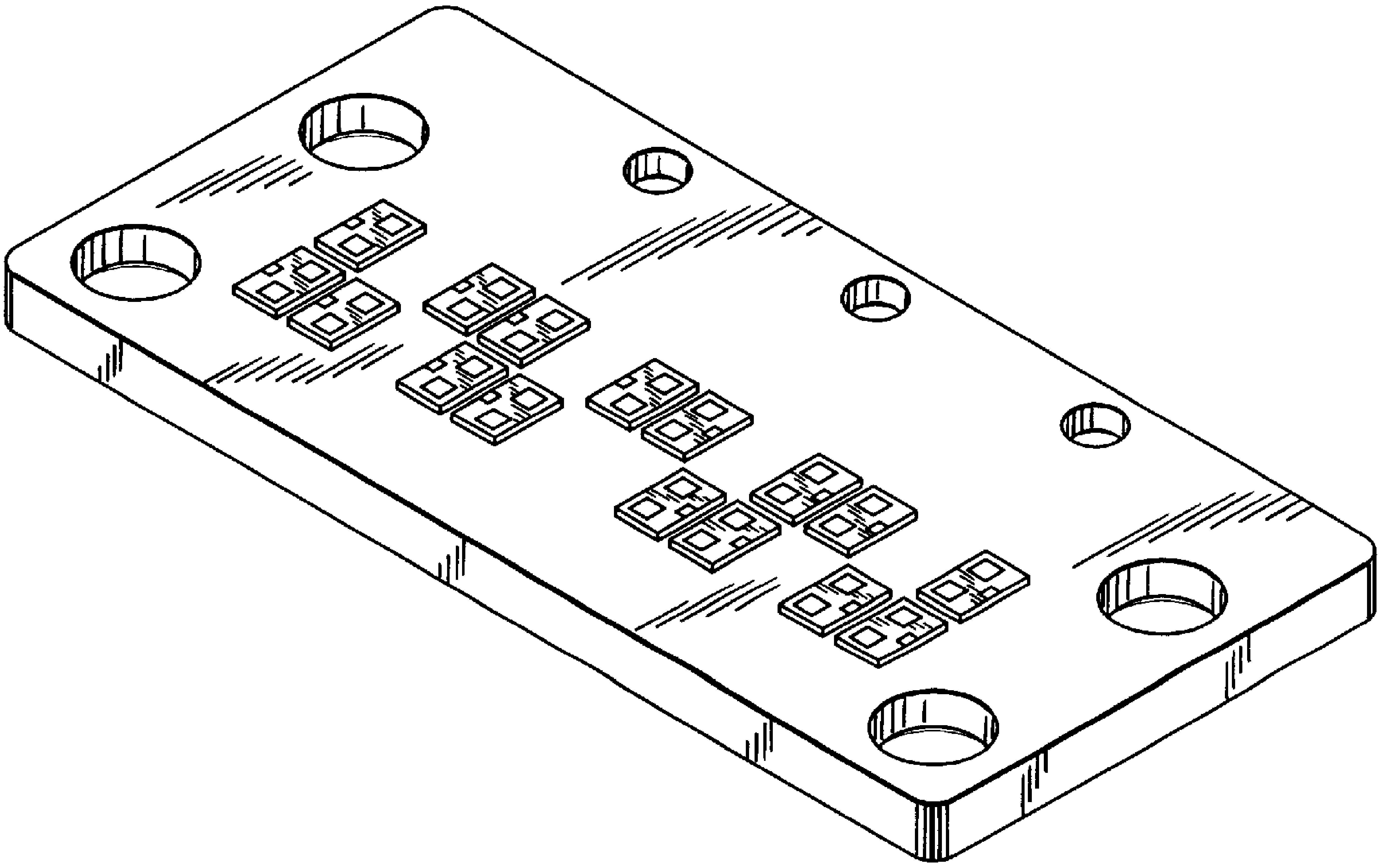


FIG.6

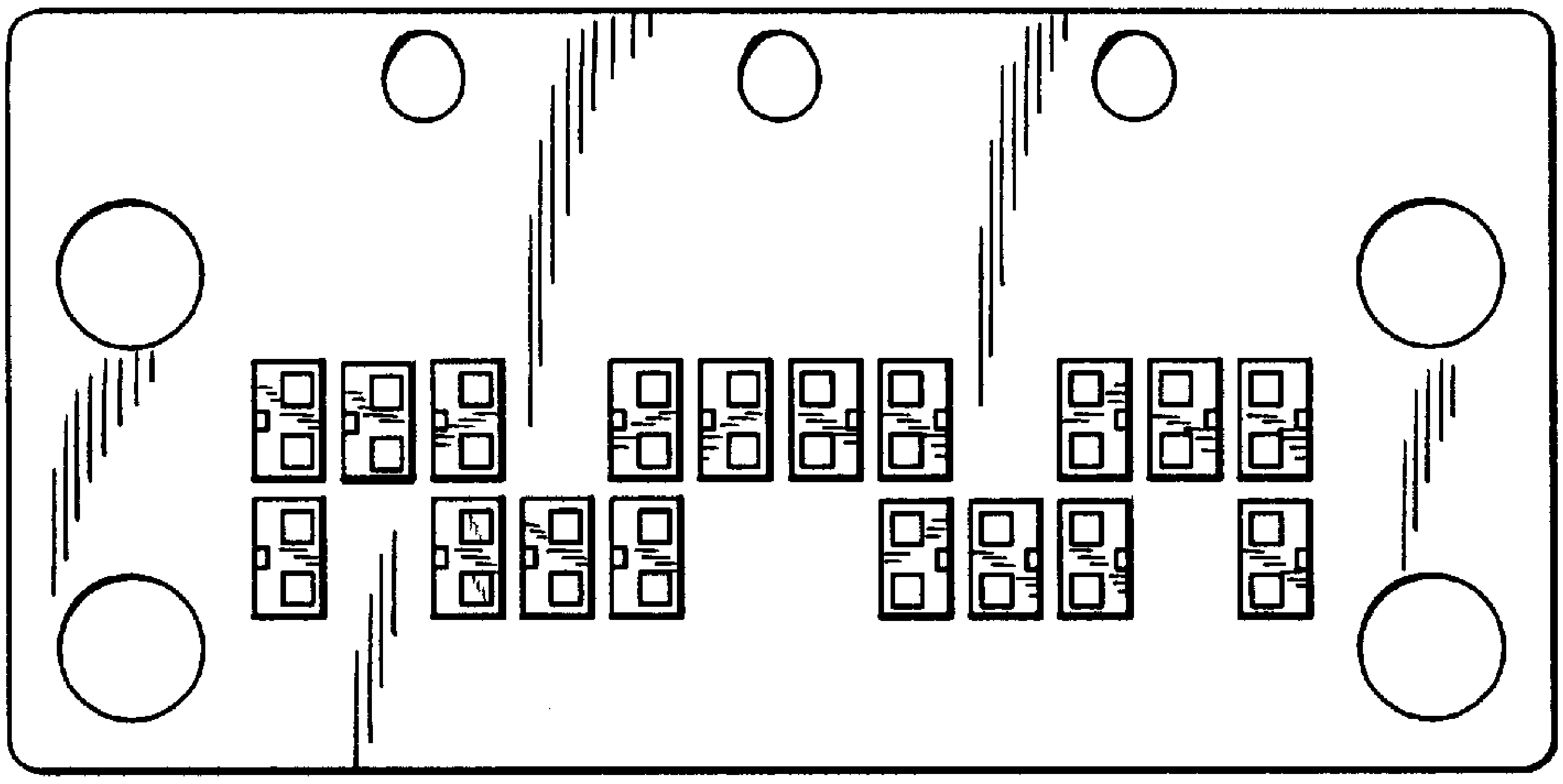


FIG.7

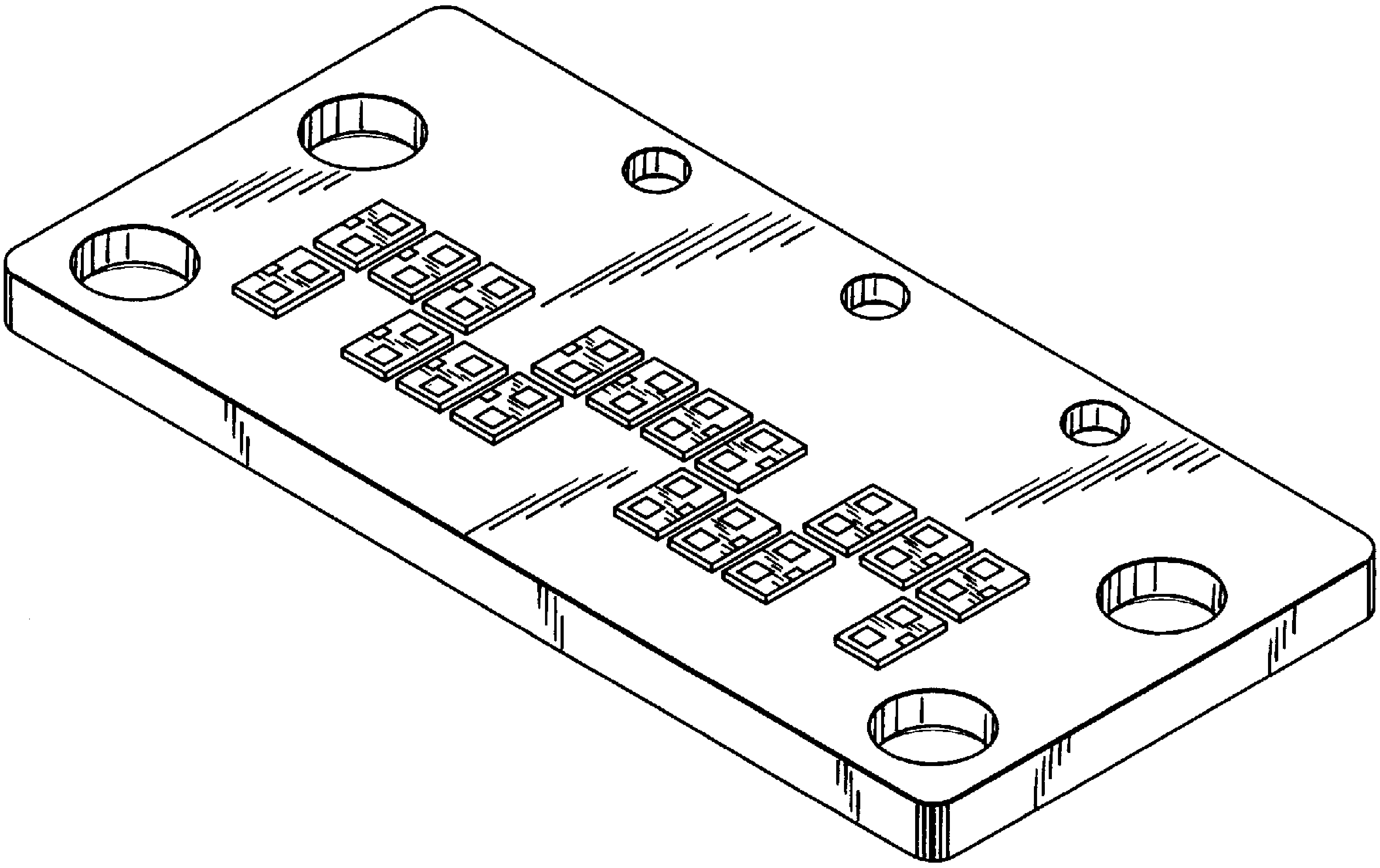


FIG.8

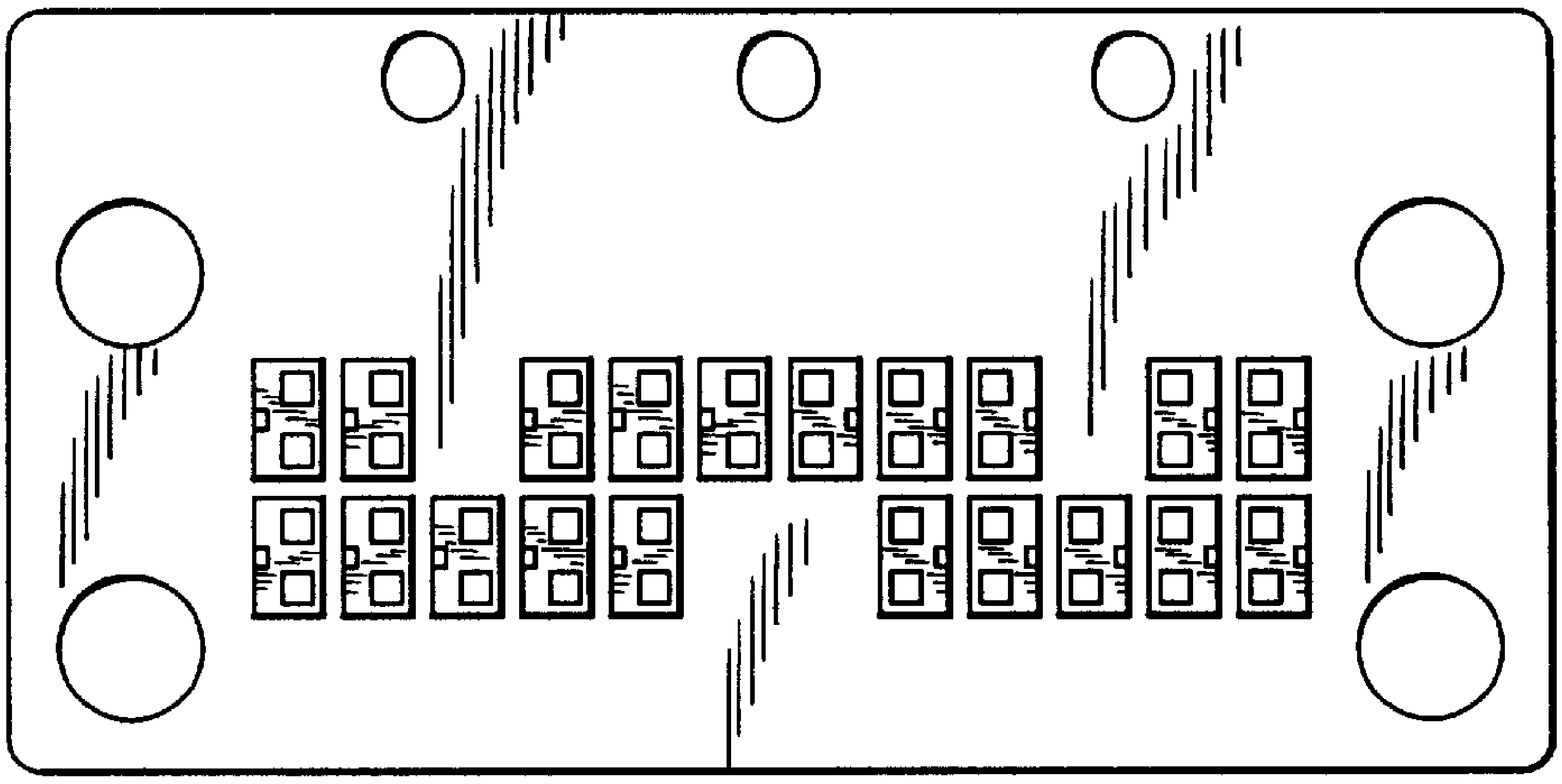


FIG.9

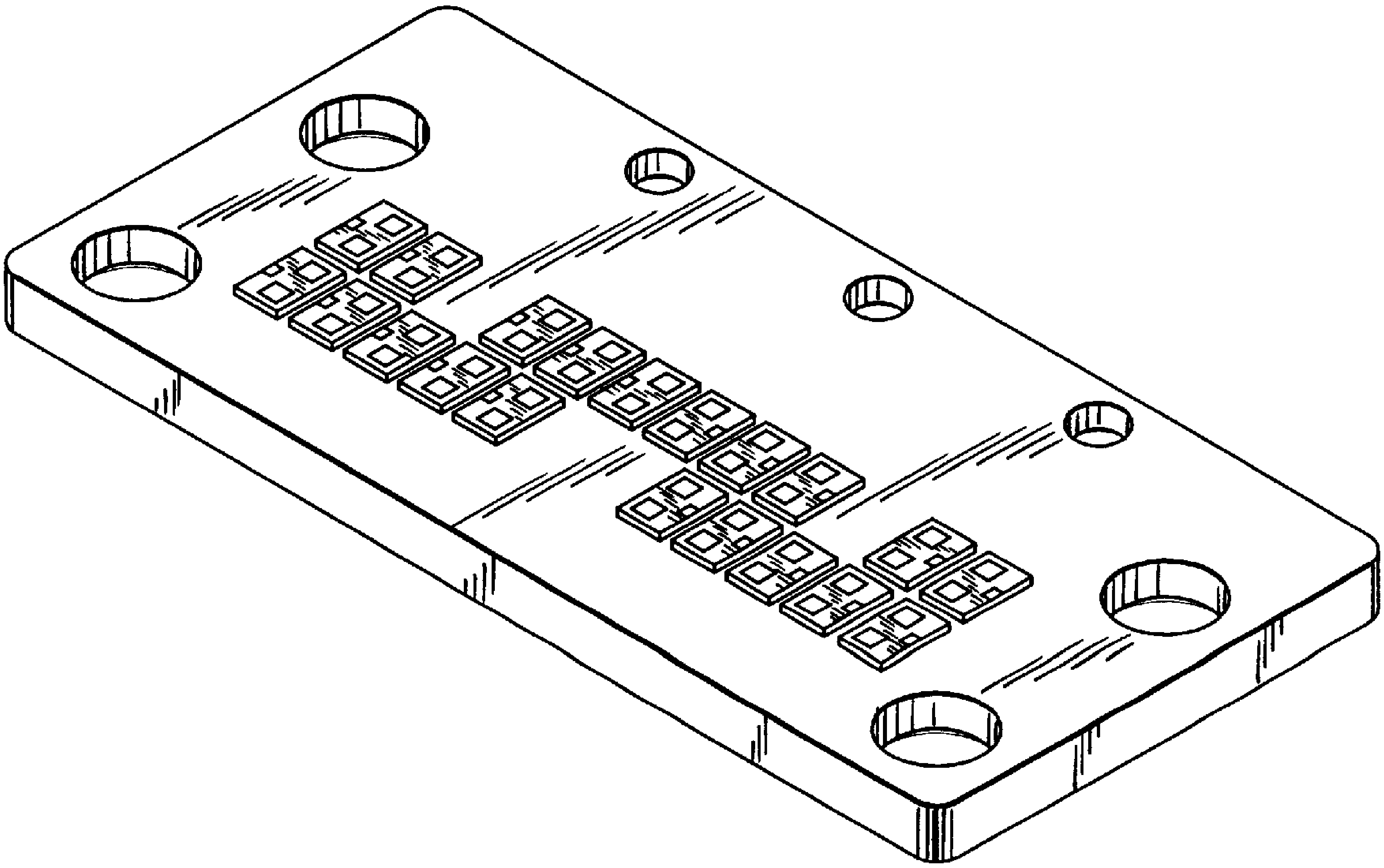


FIG.10

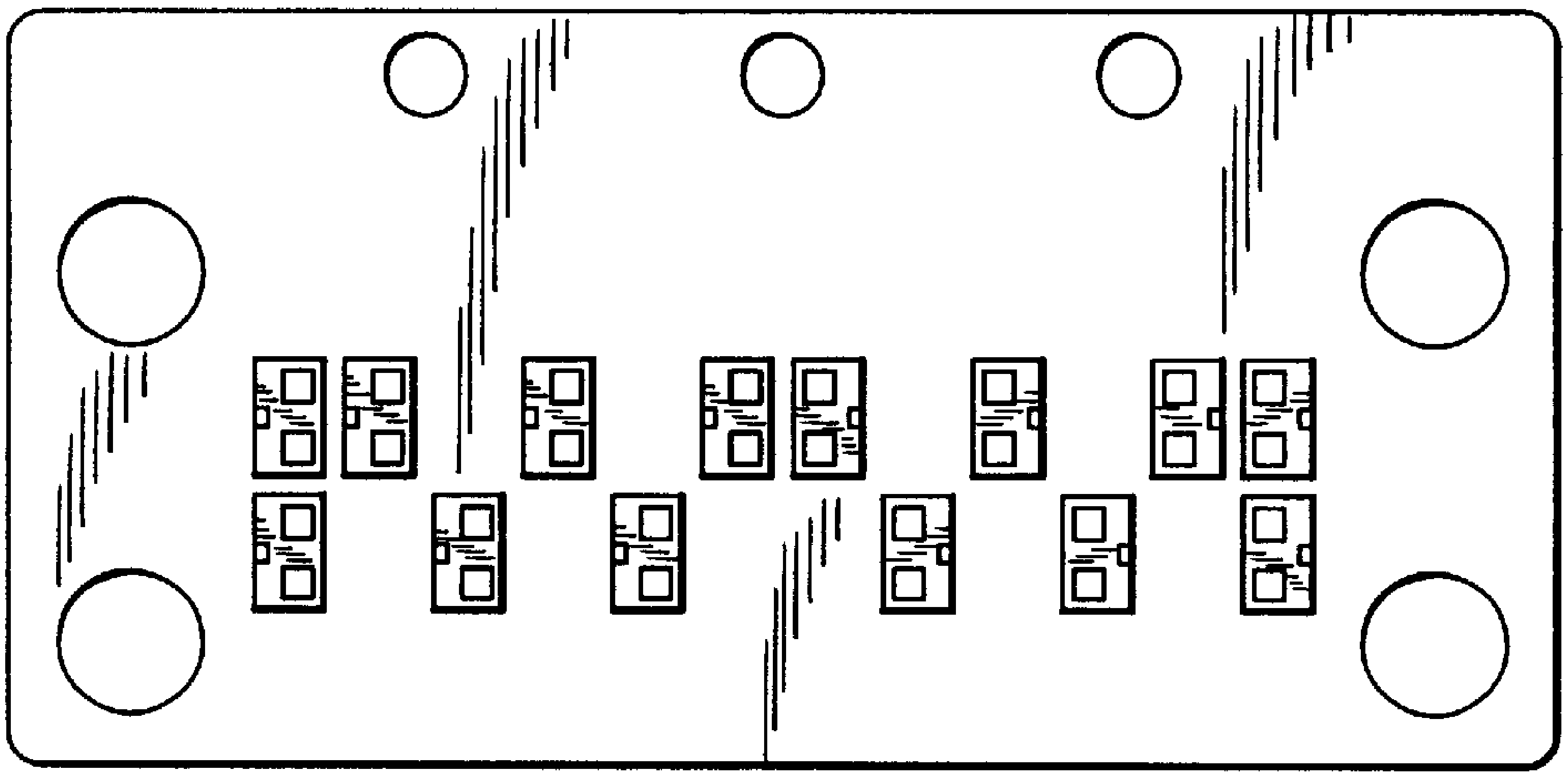


FIG.11

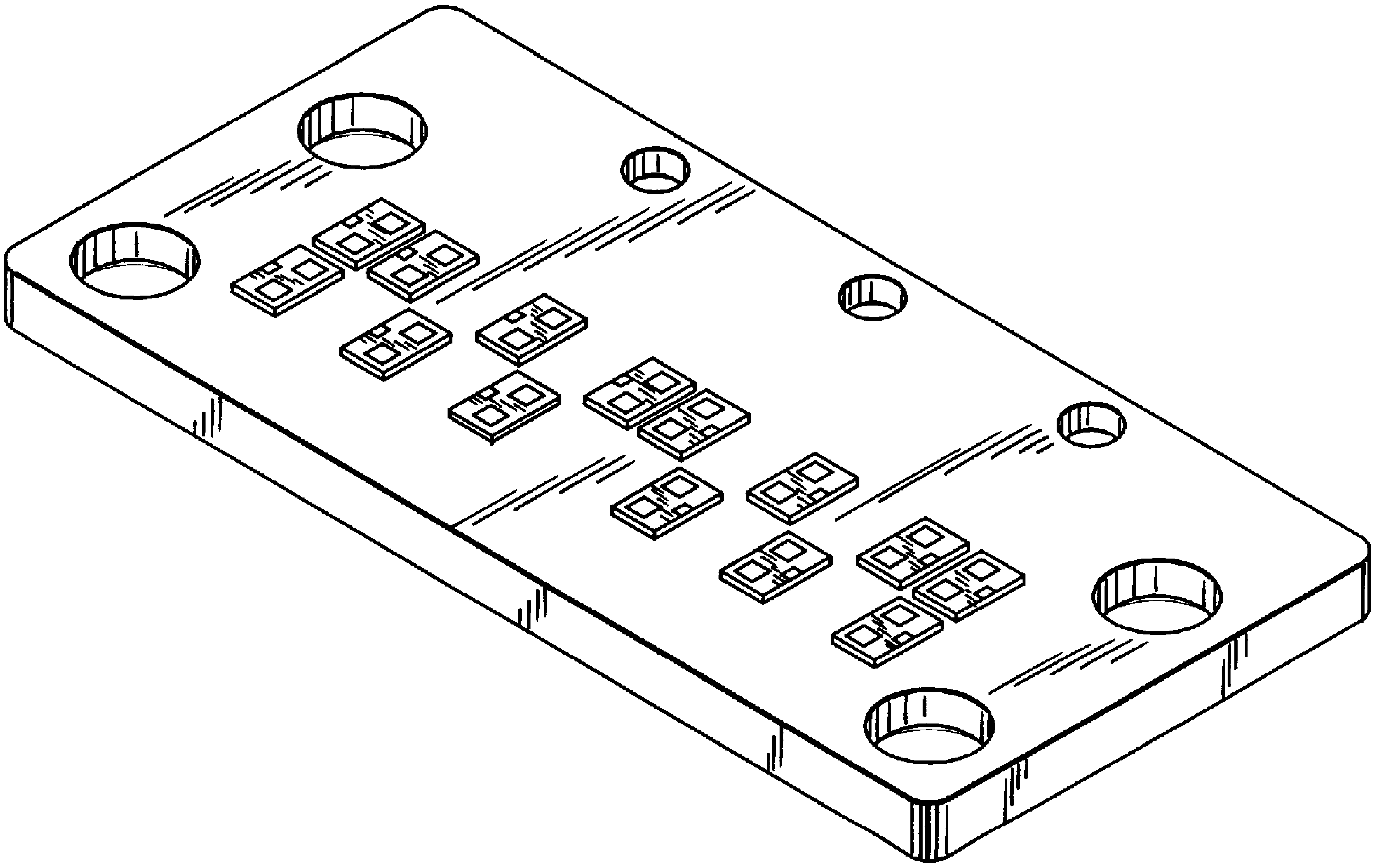


FIG.12