



US00D441730S

(12) **United States Design Patent**
Oba

(10) **Patent No.:** **US D441,730 S**

(45) **Date of Patent:** **** May 8, 2001**

(54) **SEMICONDUCTOR ELEMENT**

5,925,928 * 7/1999 Hafner et al. 257/679

(75) Inventor: **Haruo Oba**, Tokyo (JP)

* cited by examiner

(73) Assignee: **Sony Corporation**, Tokyo (JP)

Primary Examiner—Adir Aronovich

(**) Term: **14 Years**

(74) *Attorney, Agent, or Firm*—Ronald P. Kananen; Rader Fishman & Grauer

(21) Appl. No.: **29/079,664**

(57) **CLAIM**

(22) Filed: **Nov. 20, 1997**

The ornamental design for a semiconductor element, as shown and described.

(30) **Foreign Application Priority Data**

DESCRIPTION

May 21, 1997 (JP) 9-55010

FIG. 1 is a perspective view of a semiconductor element showing my new design;

(51) **LOC (7) Cl.** **14-02**

FIG. 2 is a top plan view thereof;

(52) **U.S. Cl.** **D14/117; D13/182**

FIG. 3 is a left side elevational view thereof;

(58) **Field of Search** D13/182, 199;
D14/117, 114; 84/477 R; 235/380-382,
492; 257/459, 465, 466, 618, 623, 679

FIG. 4 is a front elevational view thereof;

FIG. 5 is a bottom plan view thereof;

FIG. 6 is a right side elevational view thereof;

(56) **References Cited**

FIG. 7 is a rear elevational view thereof; and,

FIG. 8 is reference perspective view thereof in the using condition.

U.S. PATENT DOCUMENTS

Portions in broken lines are for illustrative purposes only and form no part of claimed design.

D. 330,022 * 10/1992 Chen D14/117
5,061,845 * 10/1991 Pinnavaia 235/492
5,400,687 * 3/1995 Ishii 84/477 R

1 Claim, 4 Drawing Sheets

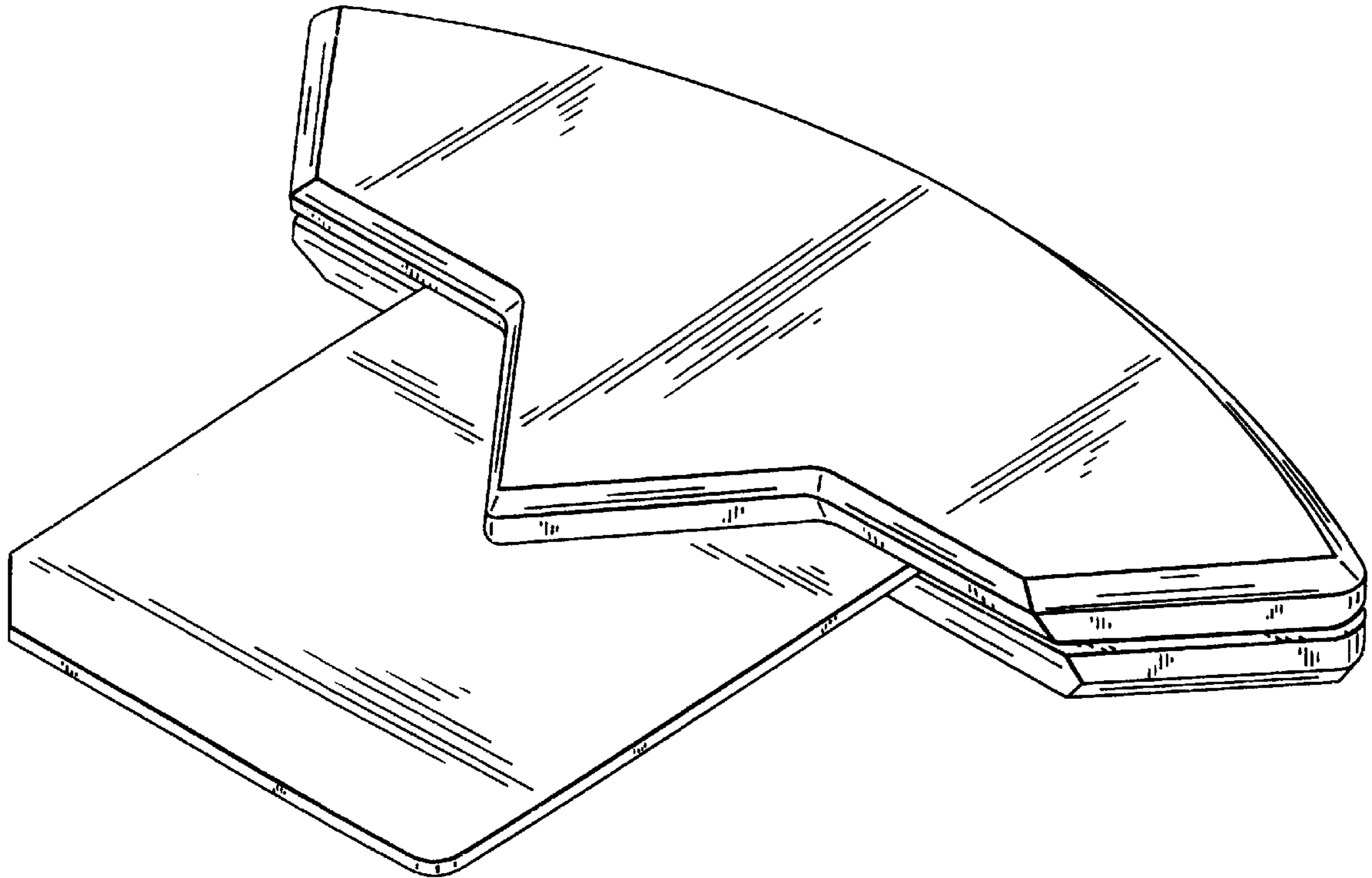


FIG. 1

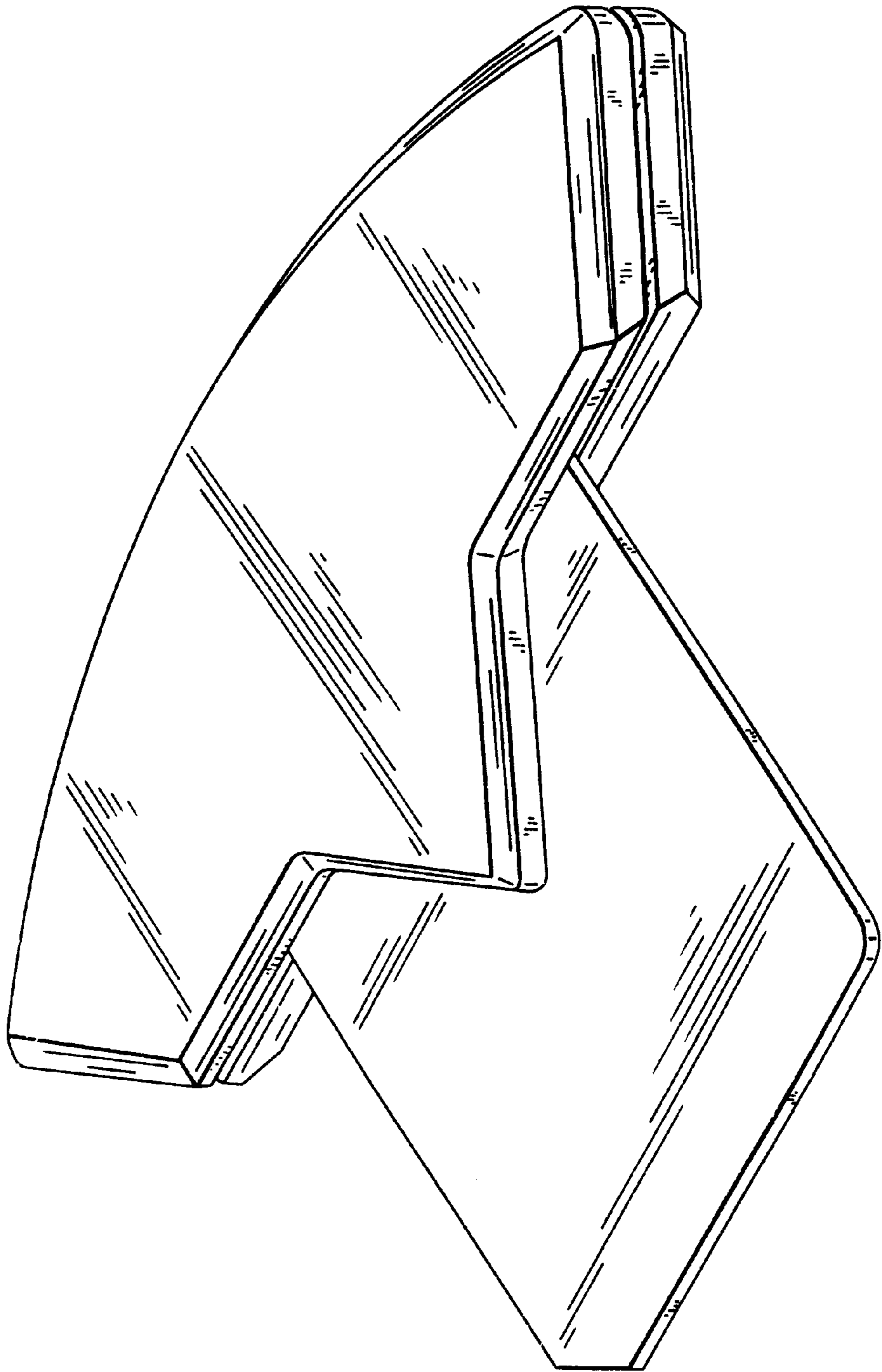


FIG. 2



FIG. 3

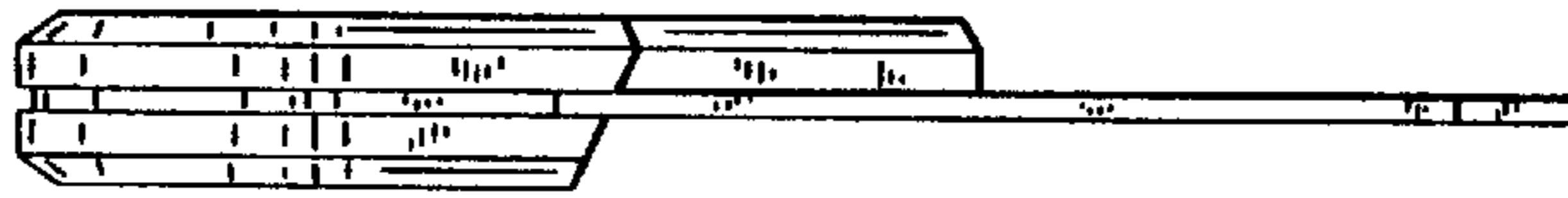


FIG. 6

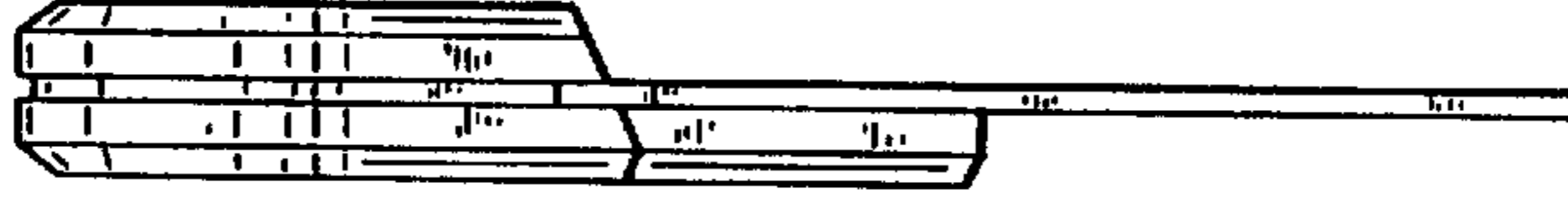


FIG. 5

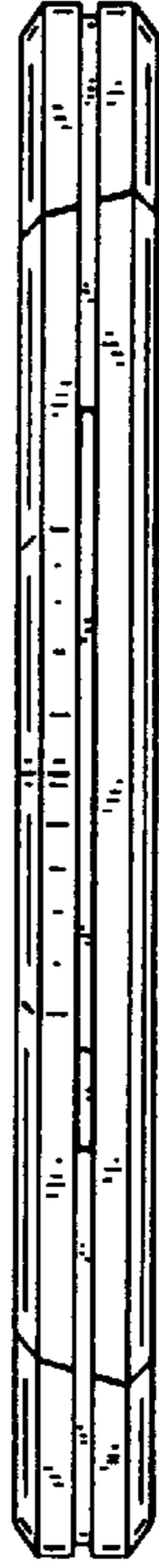


FIG. 7

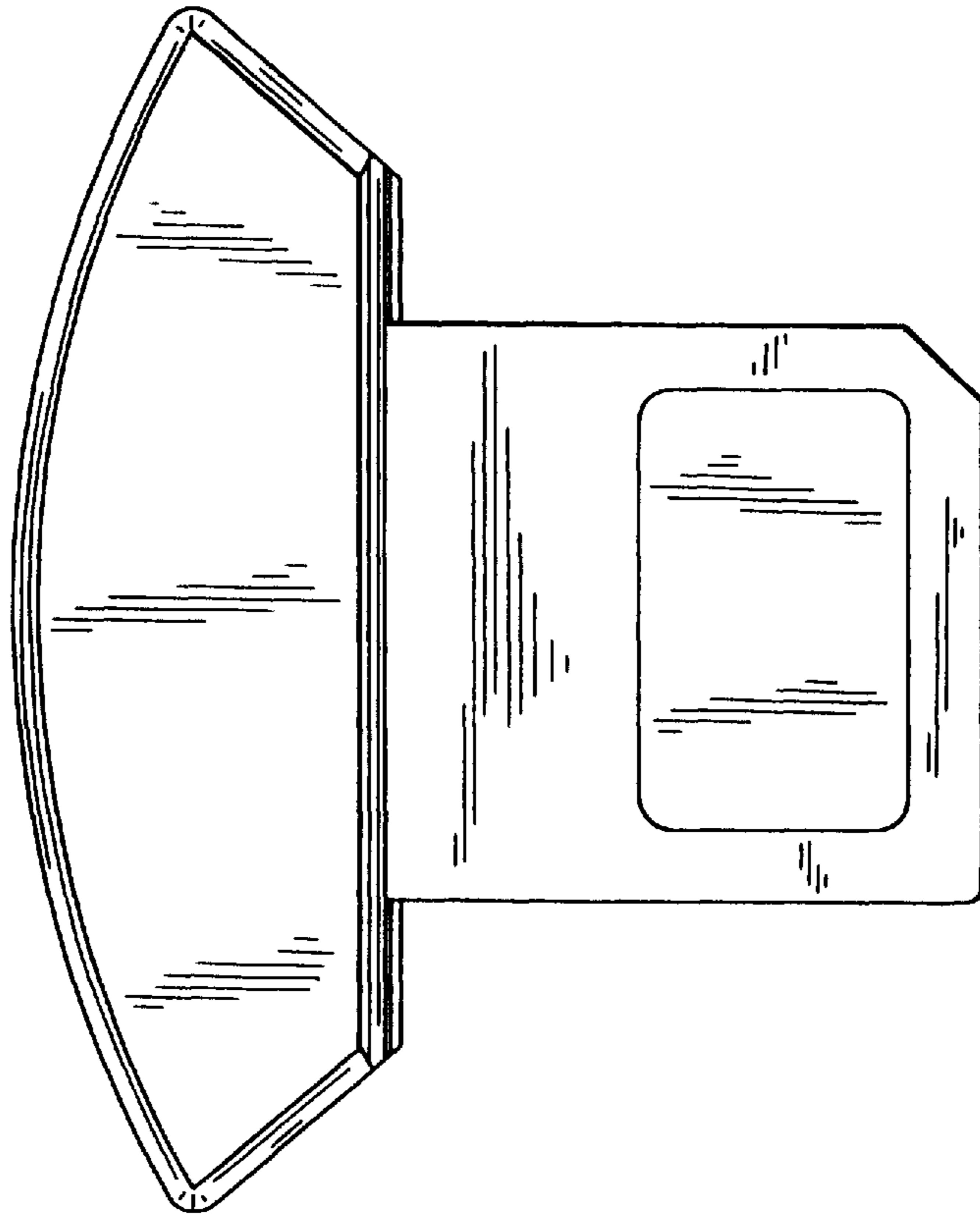


FIG. 4

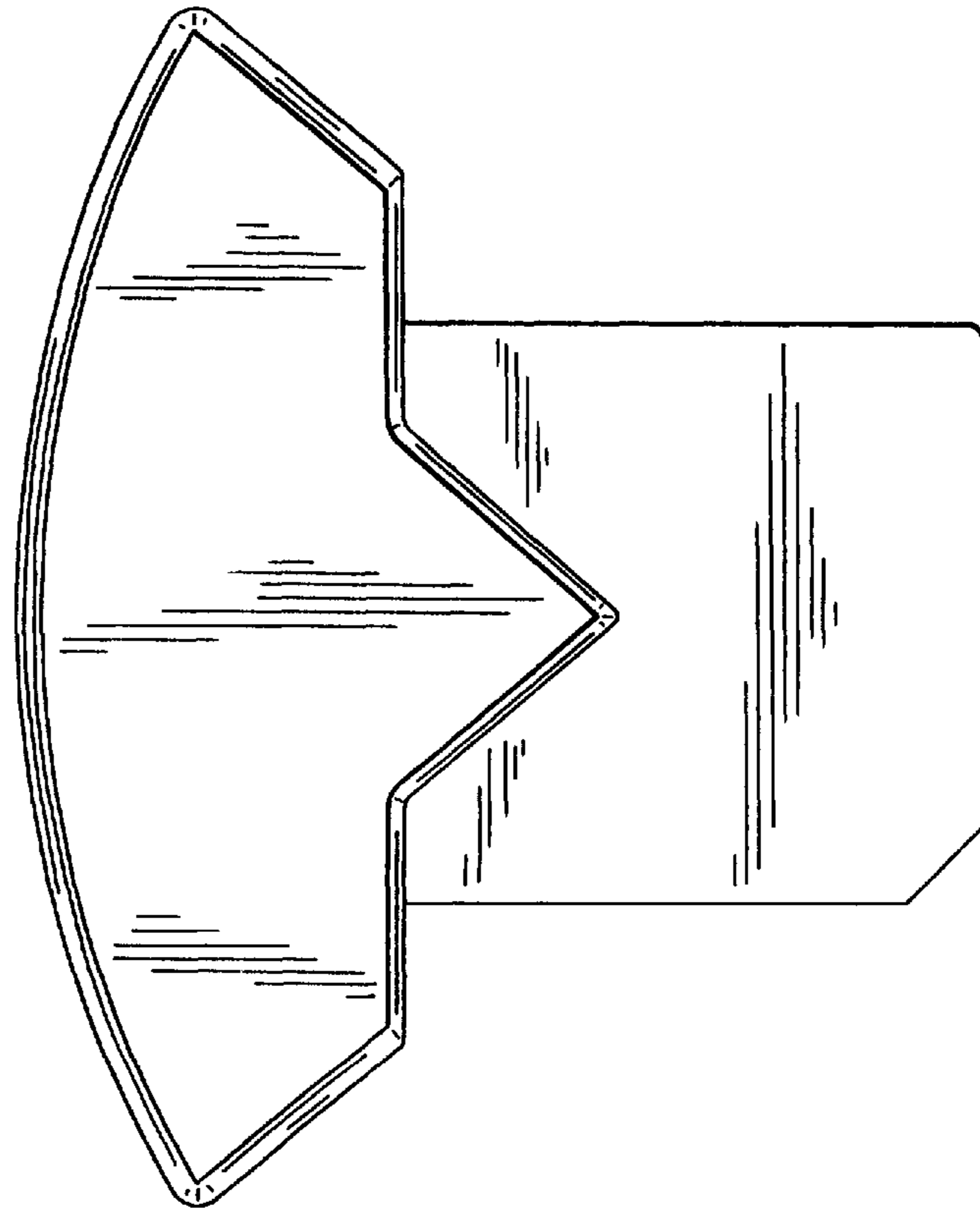


FIG. 8

