



US00D441727S

(12) **United States Design Patent**
Sekimoto

(10) **Patent No.:** **US D441,727 S**

(45) **Date of Patent:** **** May 8, 2001**

(54) **SEMICONDUCTOR ELEMENT**

(75) **Inventor:** **Emiko Sekimoto, Tokyo (JP)**

(73) **Assignee:** **Sony Corporation, Tokyo (JP)**

(**) **Term:** **14 Years**

(21) **Appl. No.:** **29/130,540**

(22) **Filed:** **Oct. 4, 2000**

(51) **LOC (7) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Search** **D13/182; 174/524,**
174/525; 257/690; 361/752, 798, 820

(56) **References Cited**

U.S. PATENT DOCUMENTS

D. 395,423	6/1998	Koyama et al.	D13/182
D. 395,638	6/1998	Koyama et al.	D13/182
D. 396,696	8/1998	Takagi et al.	D13/182
D. 401,567 *	11/1998	Farnworth et al.	D13/182
D. 402,638 *	12/1998	Farnworth et al.	D13/182
D. 427,977 *	7/2000	Takizawa et al.	D13/182
D. 432,097 *	10/2000	Song et al.	D13/182

OTHER PUBLICATIONS

Catalog "Semiconductor '97 Package Manual," "AS-A3," Sony, 1997.

* cited by examiner

Primary Examiner—Brian N. Vinson

(74) *Attorney, Agent, or Firm*—Rader, Fishman & Grauer

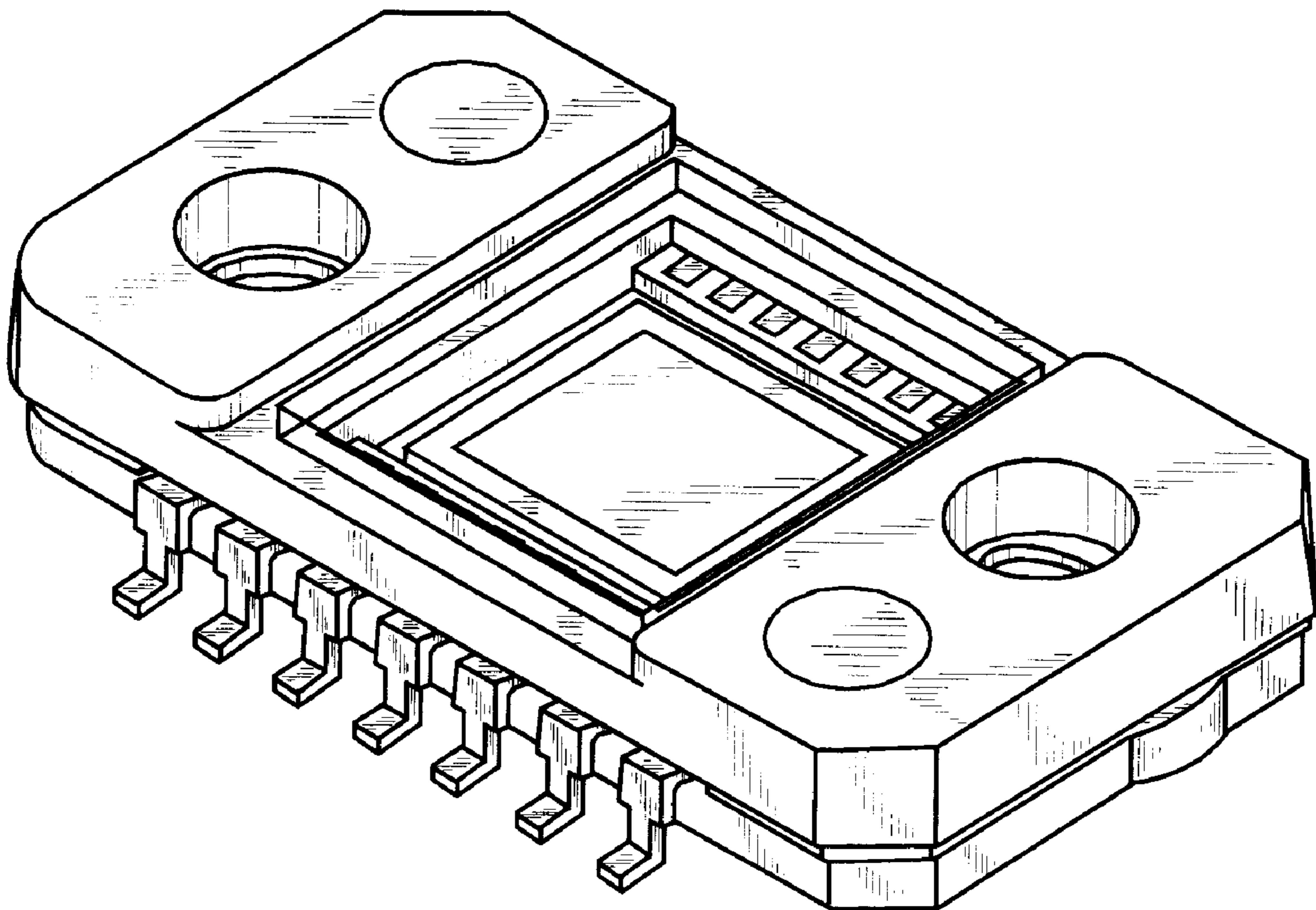
(57) **CLAIM**

The ornamental design for a semiconductor element, as shown and described.

DESCRIPTION

FIG. 1 is a top, front perspective view of a semiconductor element showing my new design;
FIG. 2 is a top plan view thereof;
FIG. 3 is a bottom plan view thereof;
FIG. 4 is a left side elevational view thereof;
FIG. 5 is a right side elevational view thereof;
FIG. 6 is a front elevational view thereof; and,
FIG. 7 is a rear elevational view thereof.

1 Claim, 4 Drawing Sheets



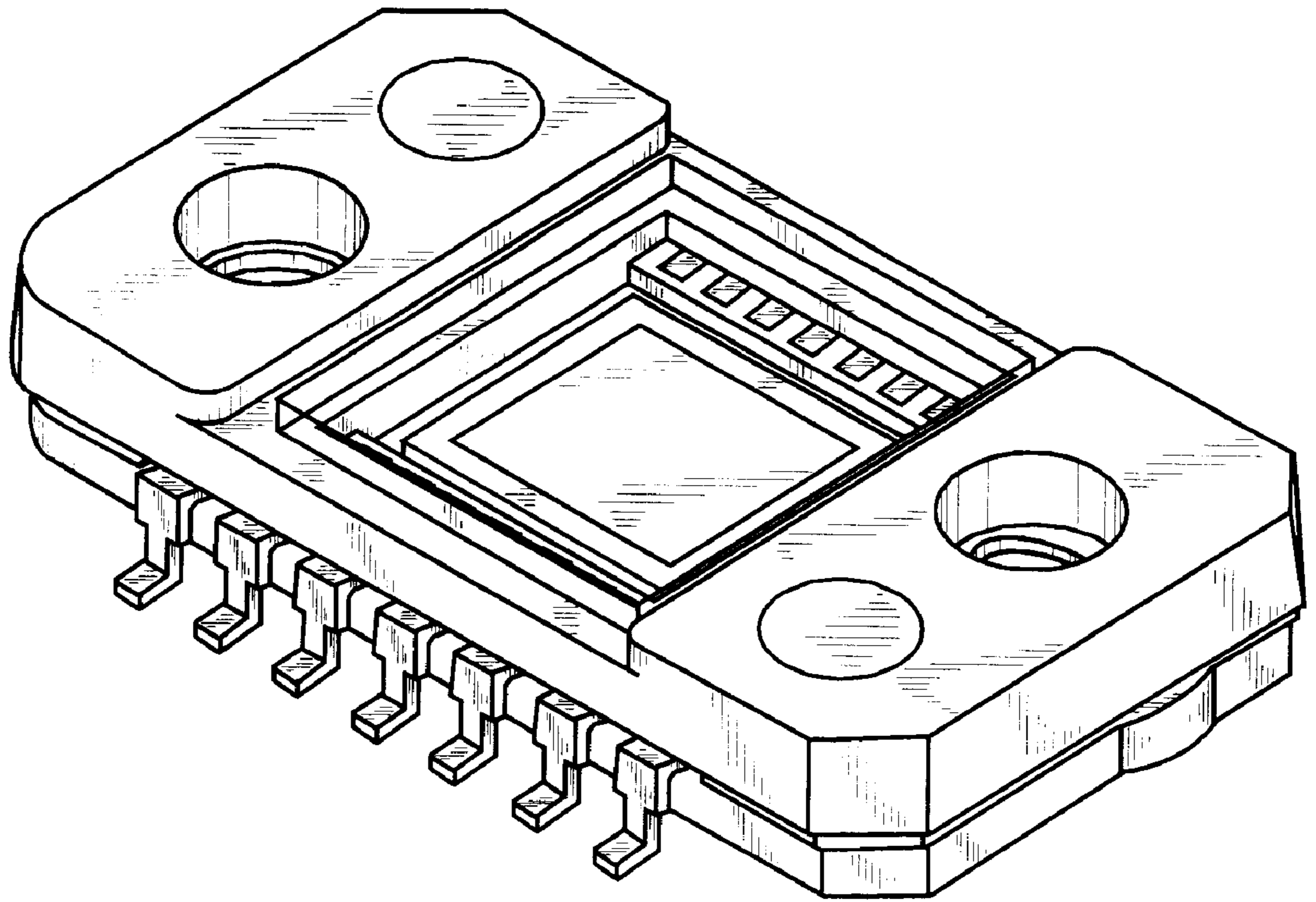


Fig. 1



Fig. 2



Fig. 3



Fig. 4

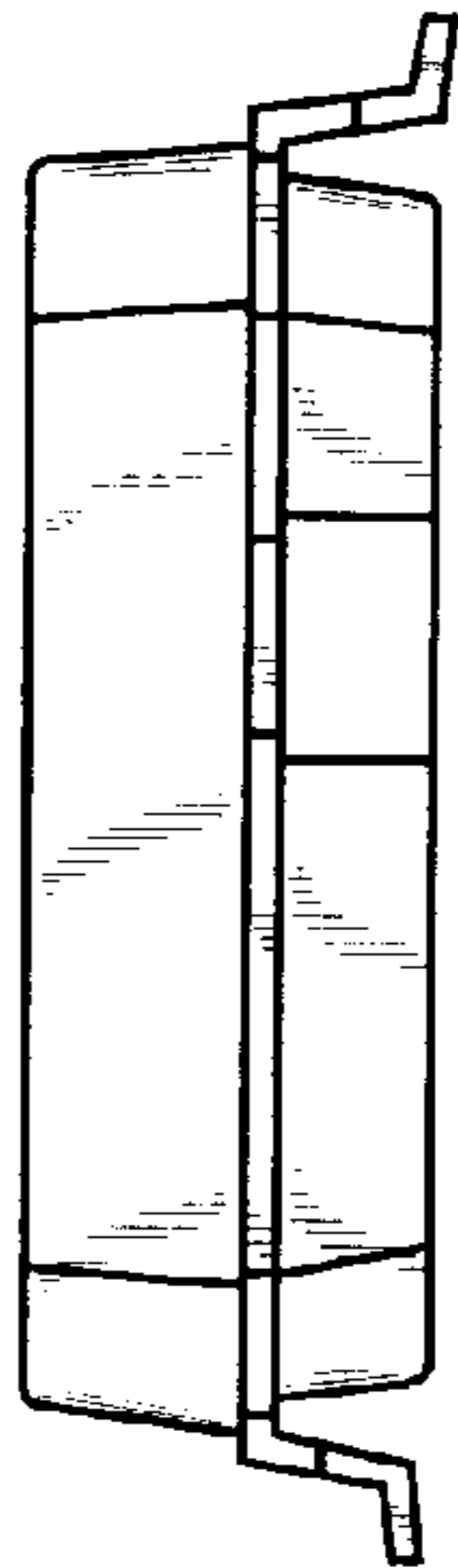


Fig. 5

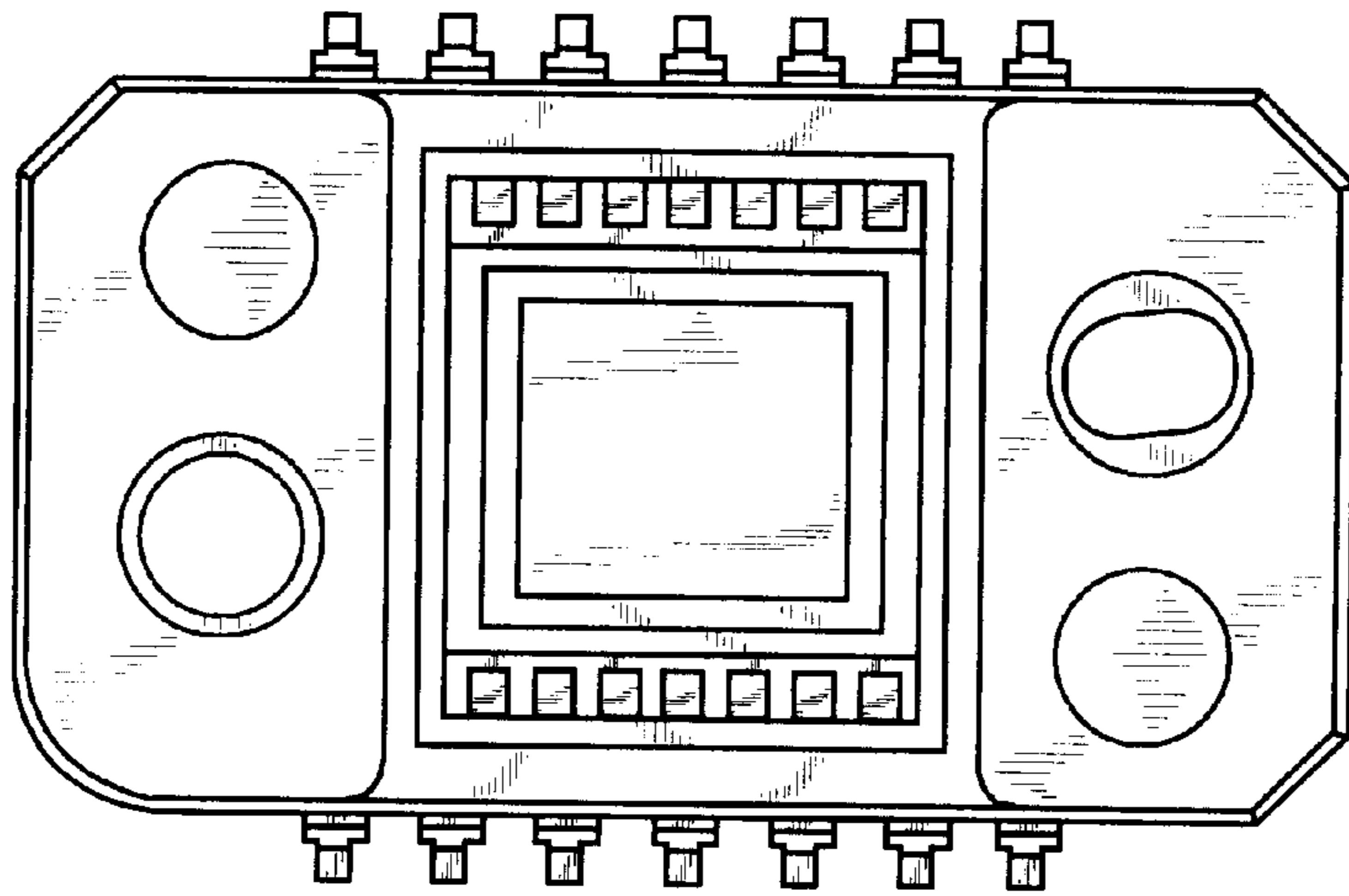


Fig. 6

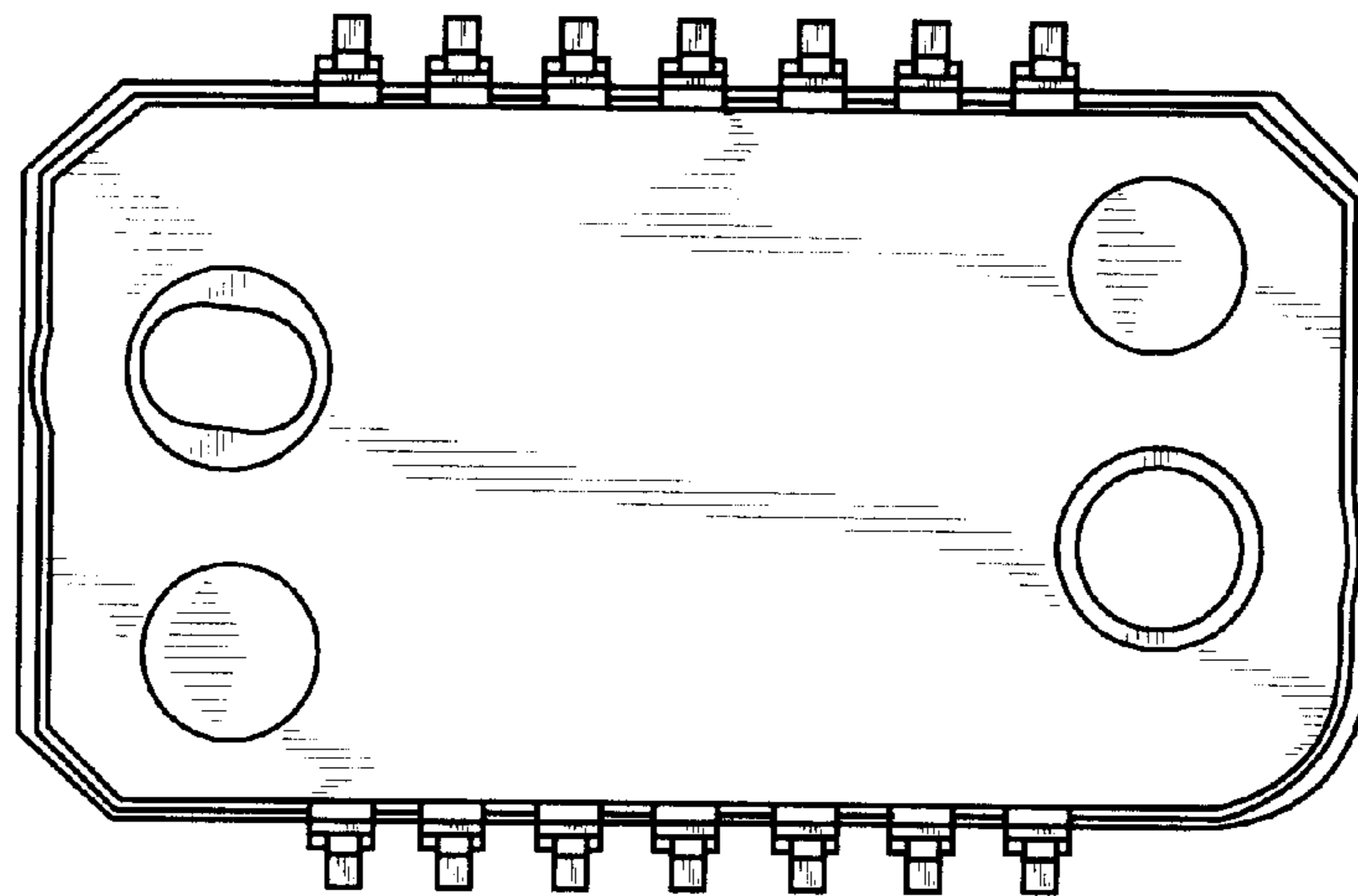


Fig. 7