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(12) United States Design Patent

Sinha et al.

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(54) MINIATURE TABLET

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(**) Term: **14 Years**

(21) Appl. No.: **29/110,989**

(22) Filed: **Sep. 17, 1999**

(51) **LOC (7) Cl.** **11-01**
(52) **U.S. Cl.** **D11/80**
(58) **Field of Search** D11/1, 2, 40, 43–44, D11/48–49, 78, 79, 80–82, 95, 99, 100, 101, 107, 116, 62, 54, 96, 102; 63/13, 14.1, 23

(56) **References Cited**

U.S. PATENT DOCUMENTS

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(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

(57) CLAIM

The ornamental design for miniature tablet, as shown and described.

DESCRIPTION

The depicted miniature tablet is comprised of an ornamental design on a substrate. Semiconductor processes may be used to create the ornamental design on, for example, a semiconductor substrate. The ornamental design comprises columns of text overlaid with a graphic. As geometries of the text in the columns are so minute, the figures cannot accurately portray the content of this text.

This application is being filed concurrently with related U.S. patent applications: Ser. No. 60/154,401, provisional patent entitled "A VLSI-based System for Durable High-density Information Storage"; Ser. No. 29/111,068, design patent entitled "Miniature Tablet"; Ser. No. 29,110,990, design patent entitled "Miniature Tablet"; Ser. No. 29,110,991, design patent entitled "Miniature Tablet", and, Ser. No. 29,110,964, design patent entitled "Miniature Tablet".

FIG. **1** is a front-top perspective view of a miniature tablet showing my new design;

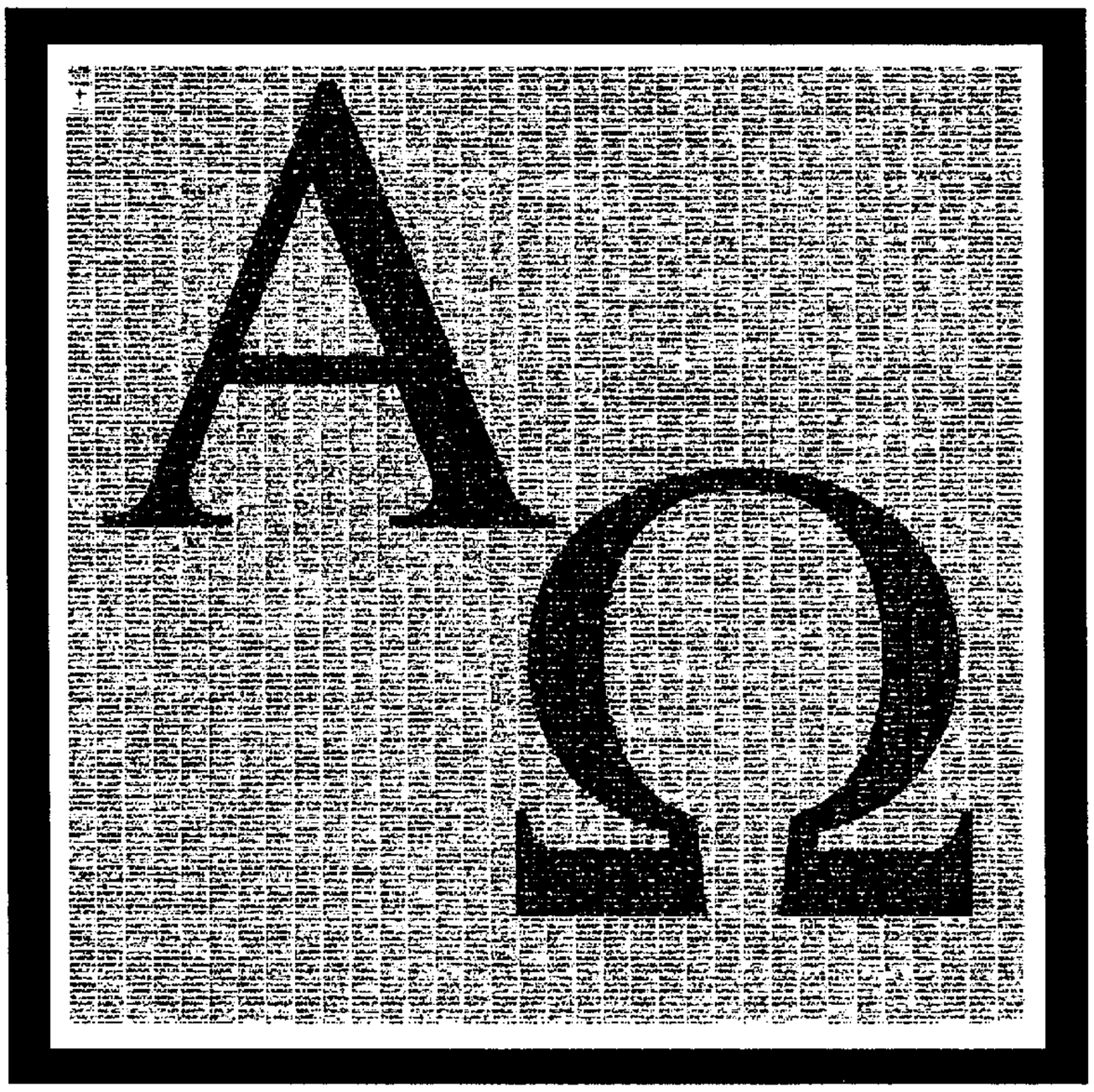
FIG. **2** is a top plan view thereof;

FIG. **3** is a front elevational view, the rear elevational view being a mirror image thereof;

FIG. **4** is a right side elevational view, the left side elevational view being a mirror image thereof; and,

FIG. **5** is a bottom paln view thereof.

1 Claim, 2 Drawing Sheets



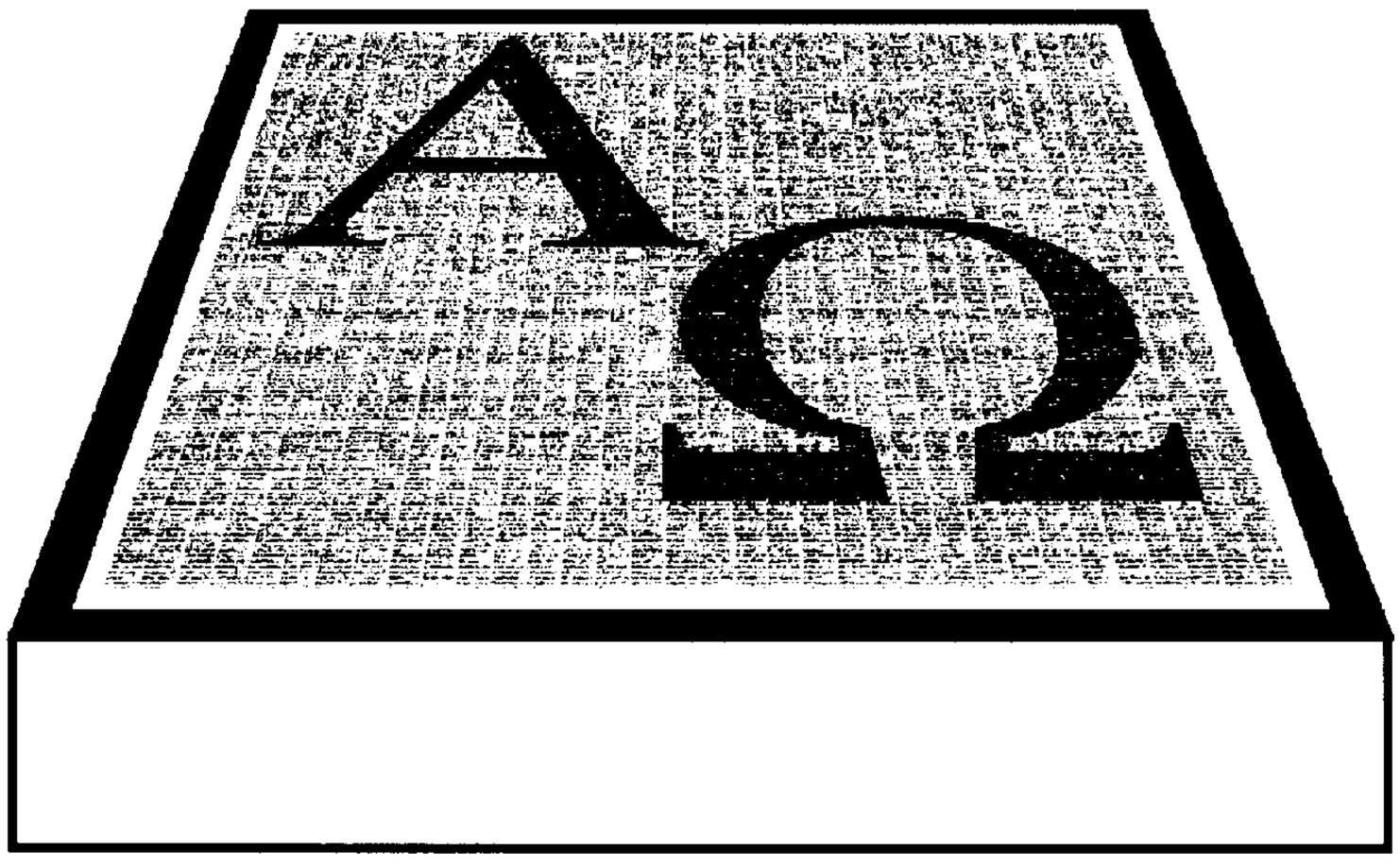


Fig. 1

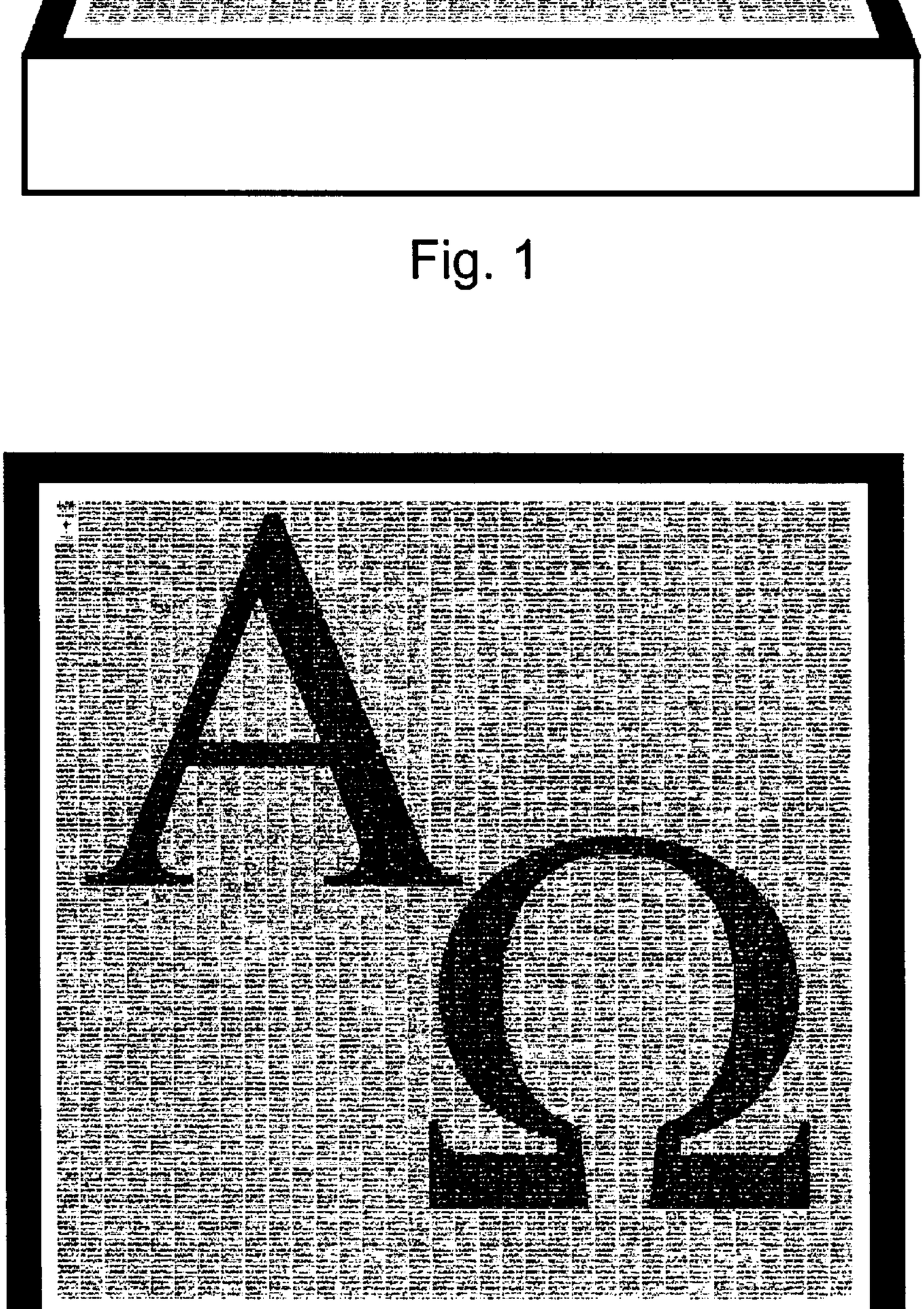


Fig. 2

Fig. 3

Fig. 4

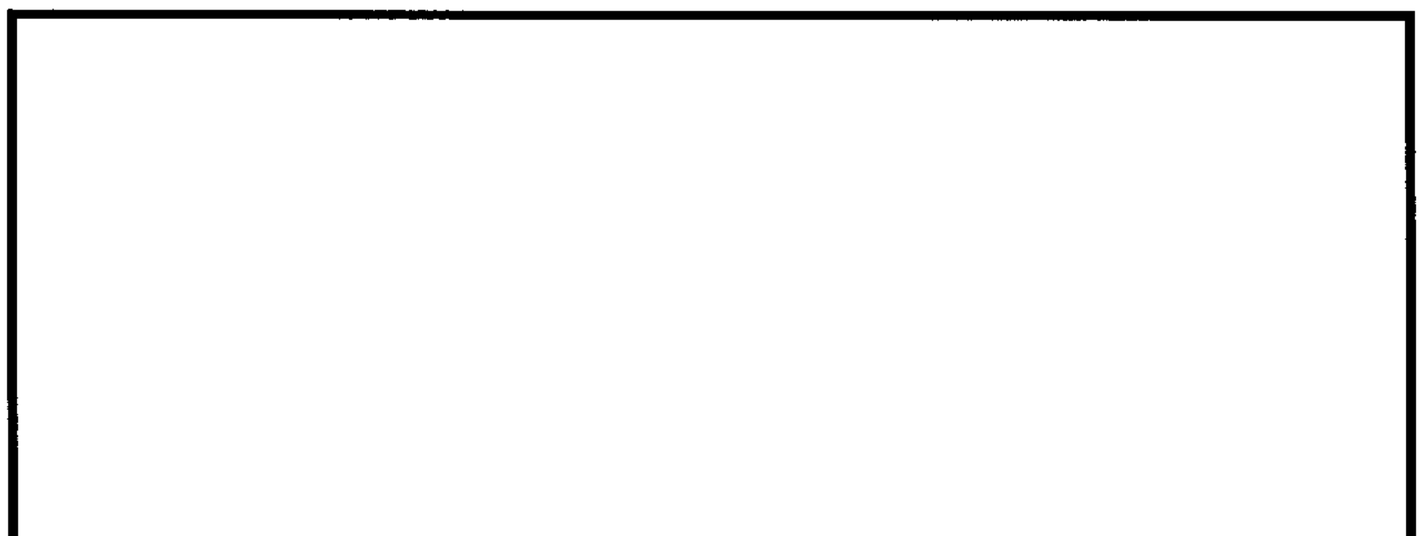


Fig. 5