



US00D435254S

# United States Patent [19] Gaudette et al.

[11] **Patent Number: Des. 435,254**

[45] **Date of Patent: \*\* Dec. 19, 2000**

[54] **PROCESSOR-BASED SYSTEM**

[75] Inventors: **Arthur L. Gaudette; Richard J. Takahashi**, both of Phoenix, Ariz.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[\*\*] Term: **14 Years**

[21] Appl. No.: **29/123,037**

[22] Filed: **May 9, 2000**

[51] **LOC (7) Cl.** ..... **14-02**

[52] **U.S. Cl.** ..... **D14/329**

[58] **Field of Search** ..... D14/336, 337, D14/371, 329, 126-129; 345/104, 156, 168, 173, 901-905, 87, 133; 361/680-686; 364/708.1; 358/249, 254, 255

[56] **References Cited**

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- D. 383,444 9/1997 Han .... D14/337
- D. 427,592 7/2000 Gaudette et al. .... D14/329

*Primary Examiner*—Freda Nunn  
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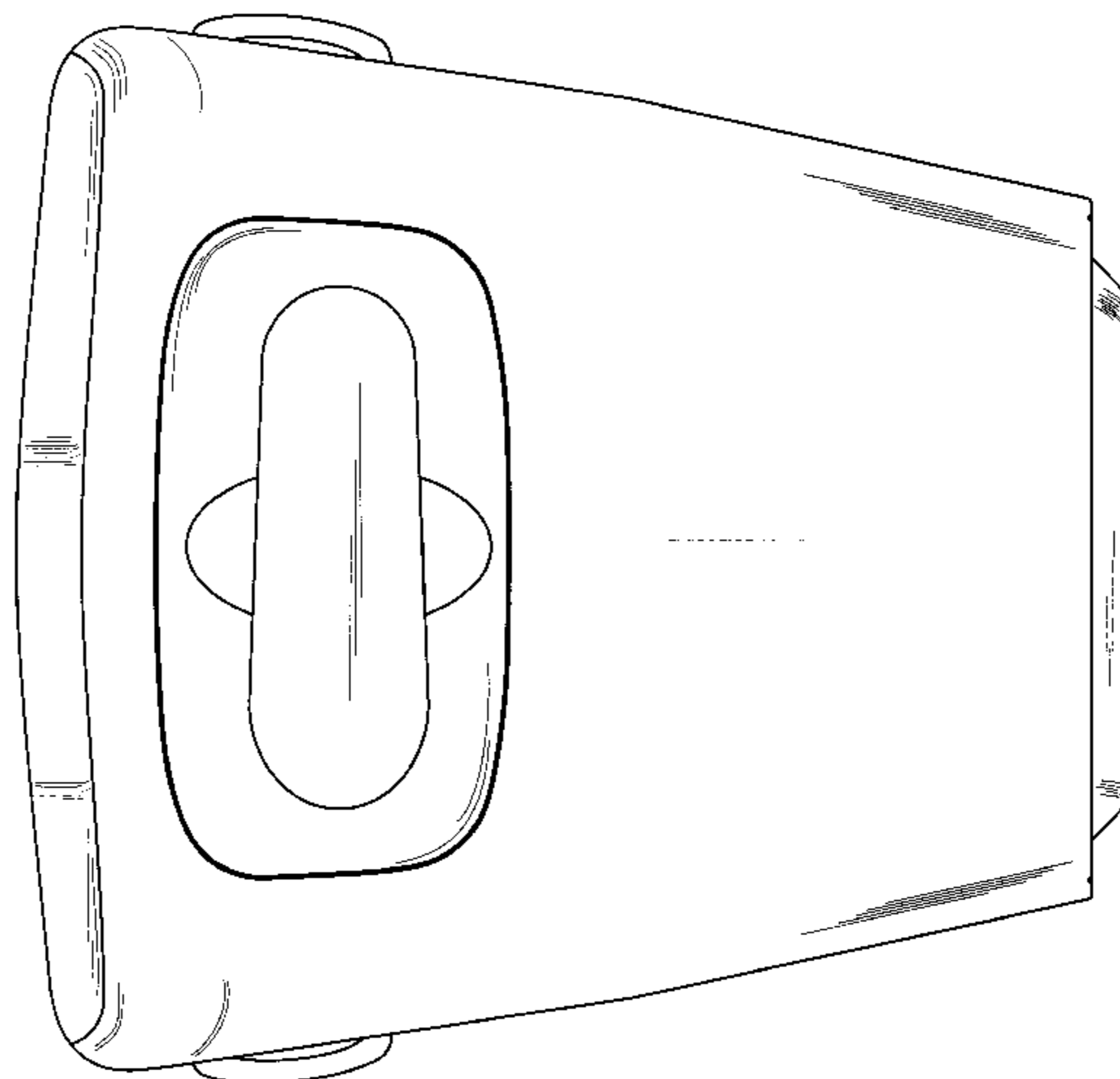
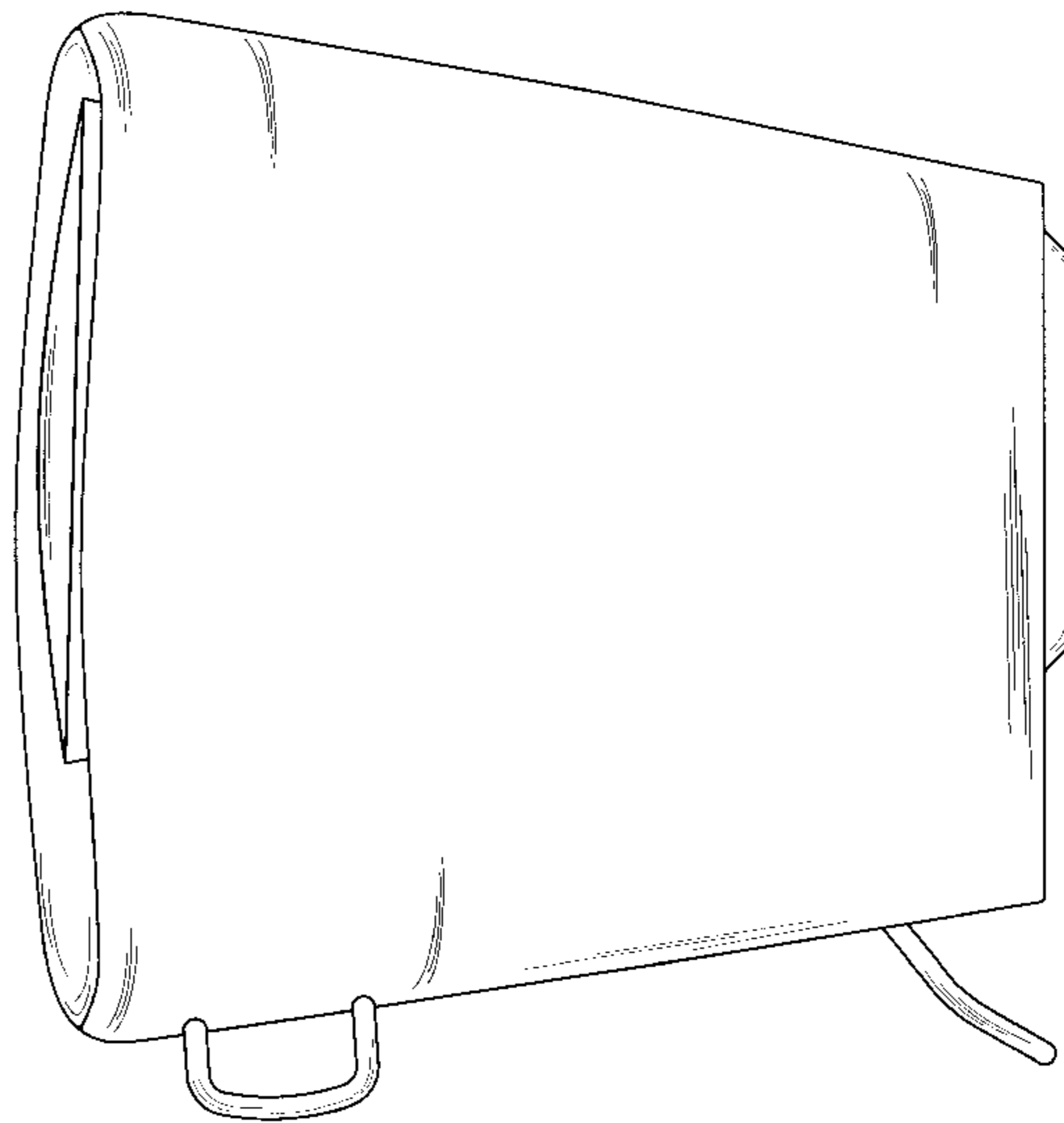
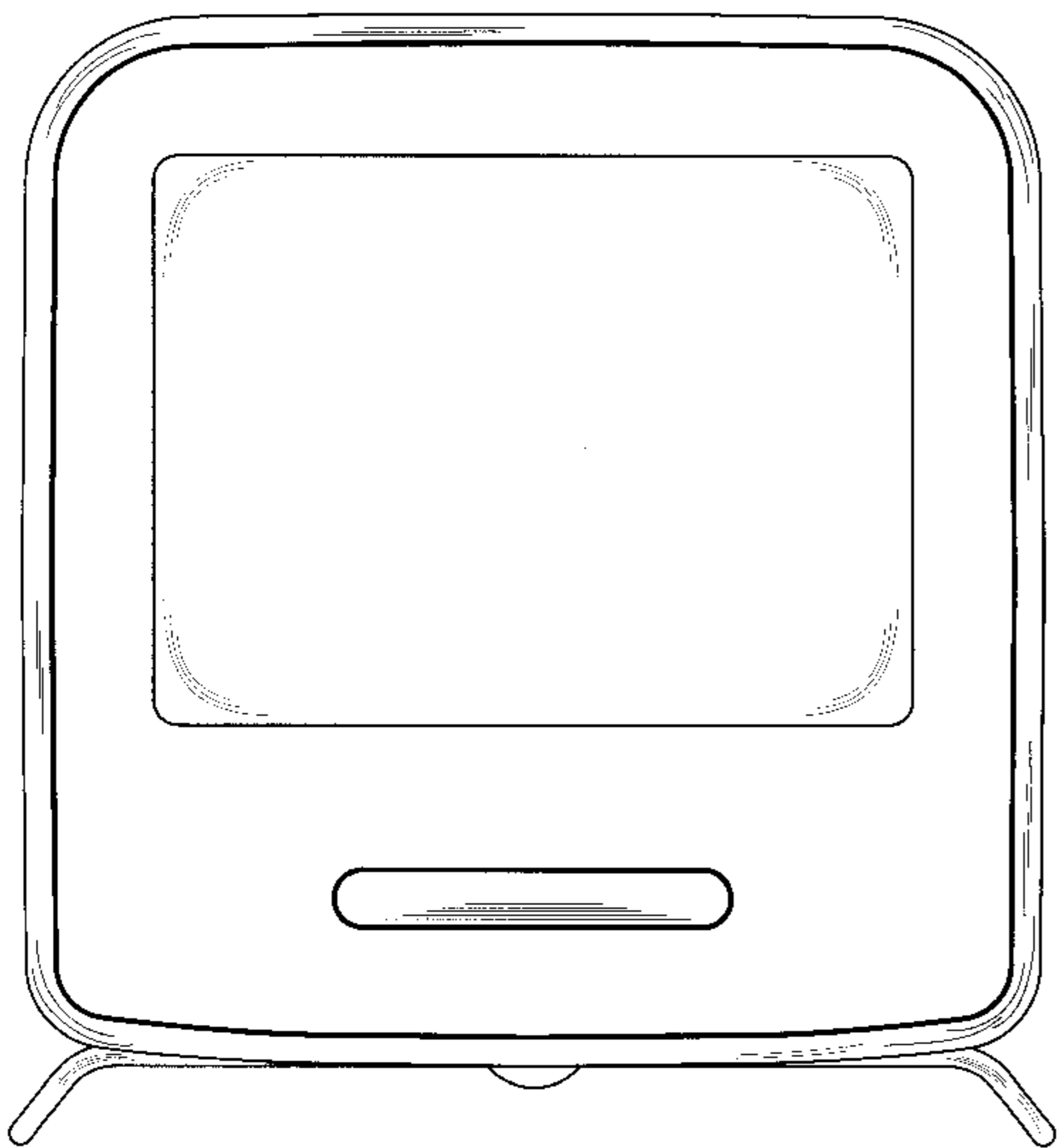
[57] **CLAIM**

The ornamental design for the processor-based system, as shown and described.

**DESCRIPTION**

FIG. 1 is a front view of a processor-based system;  
FIG. 2 is a side view thereof, wherein the right side and the left side are the same;  
FIG. 3 is a top view thereof;  
FIG. 4 is a bottom view thereof; and,  
FIG. 5 is a back view thereof.

**1 Claim, 5 Drawing Sheets**



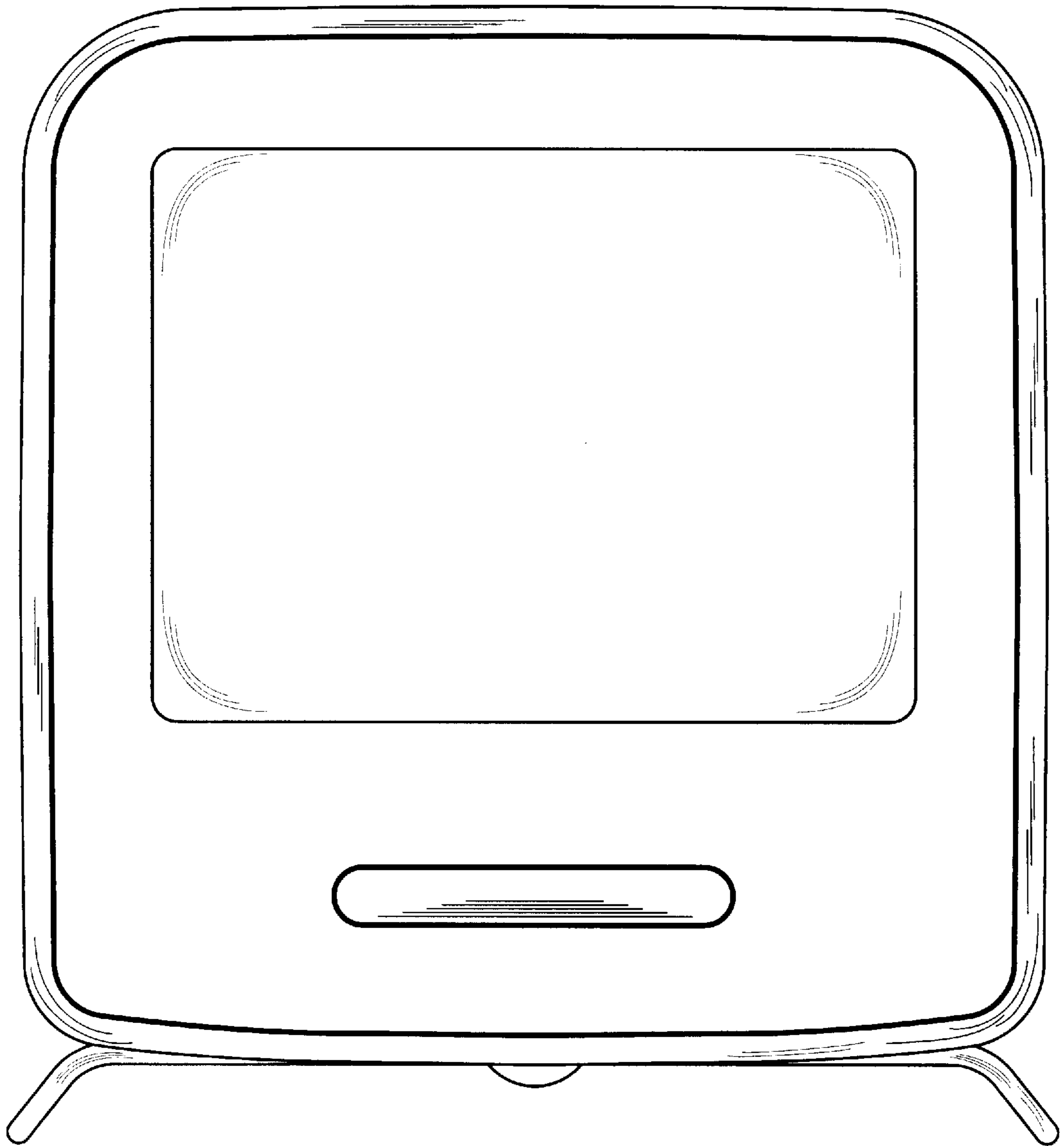


FIG. 1

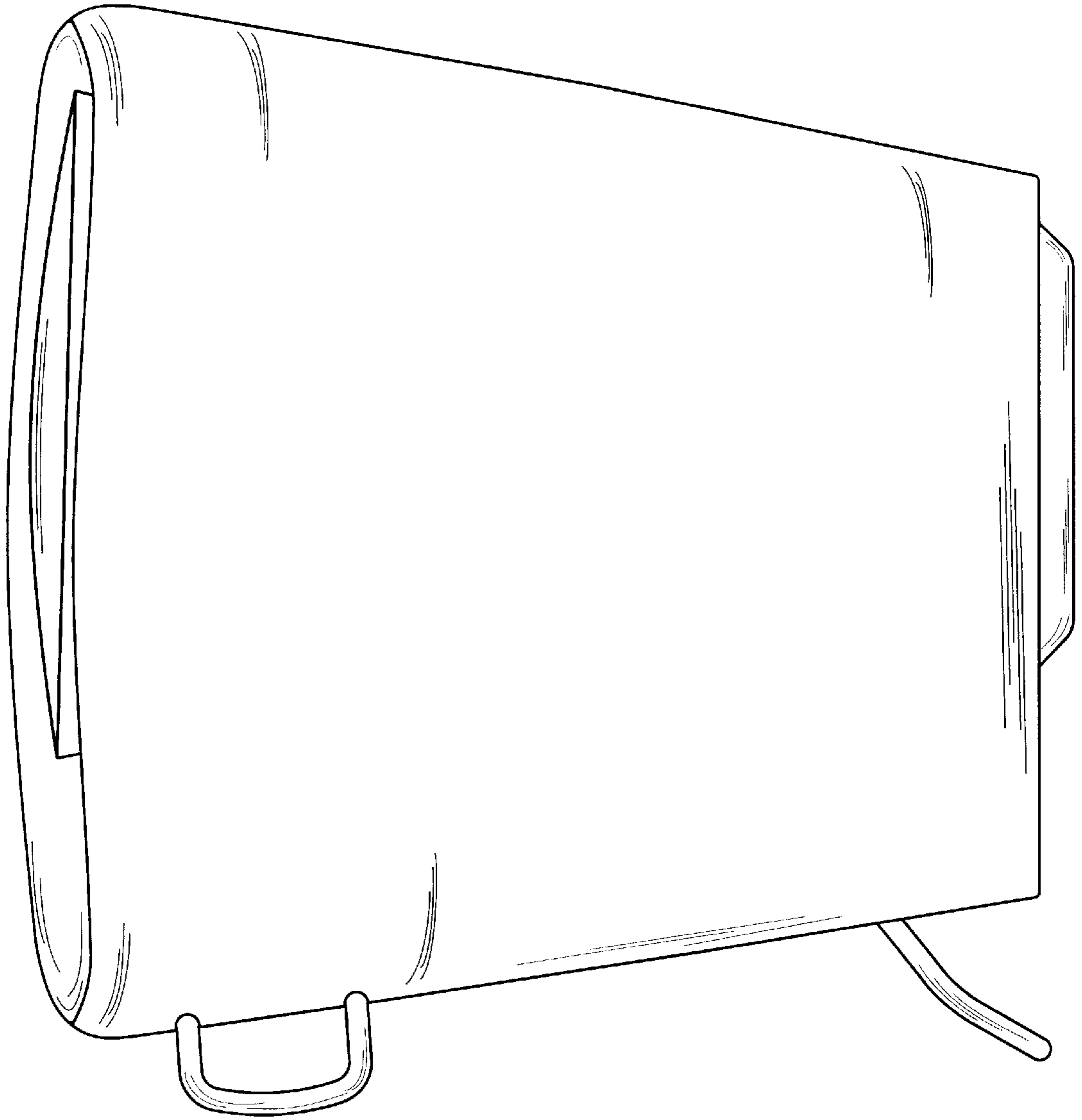


FIG. 2

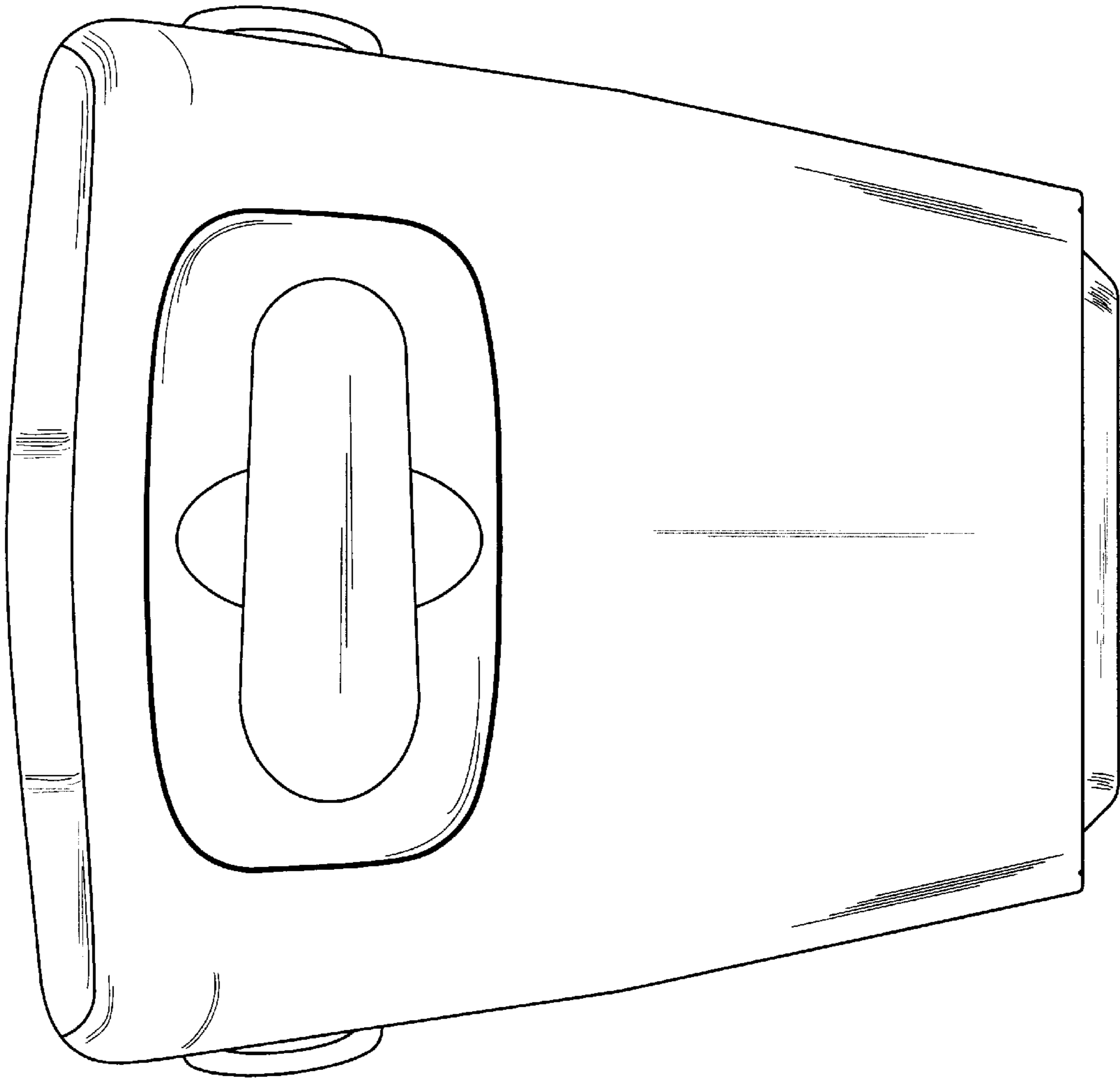


FIG. 3

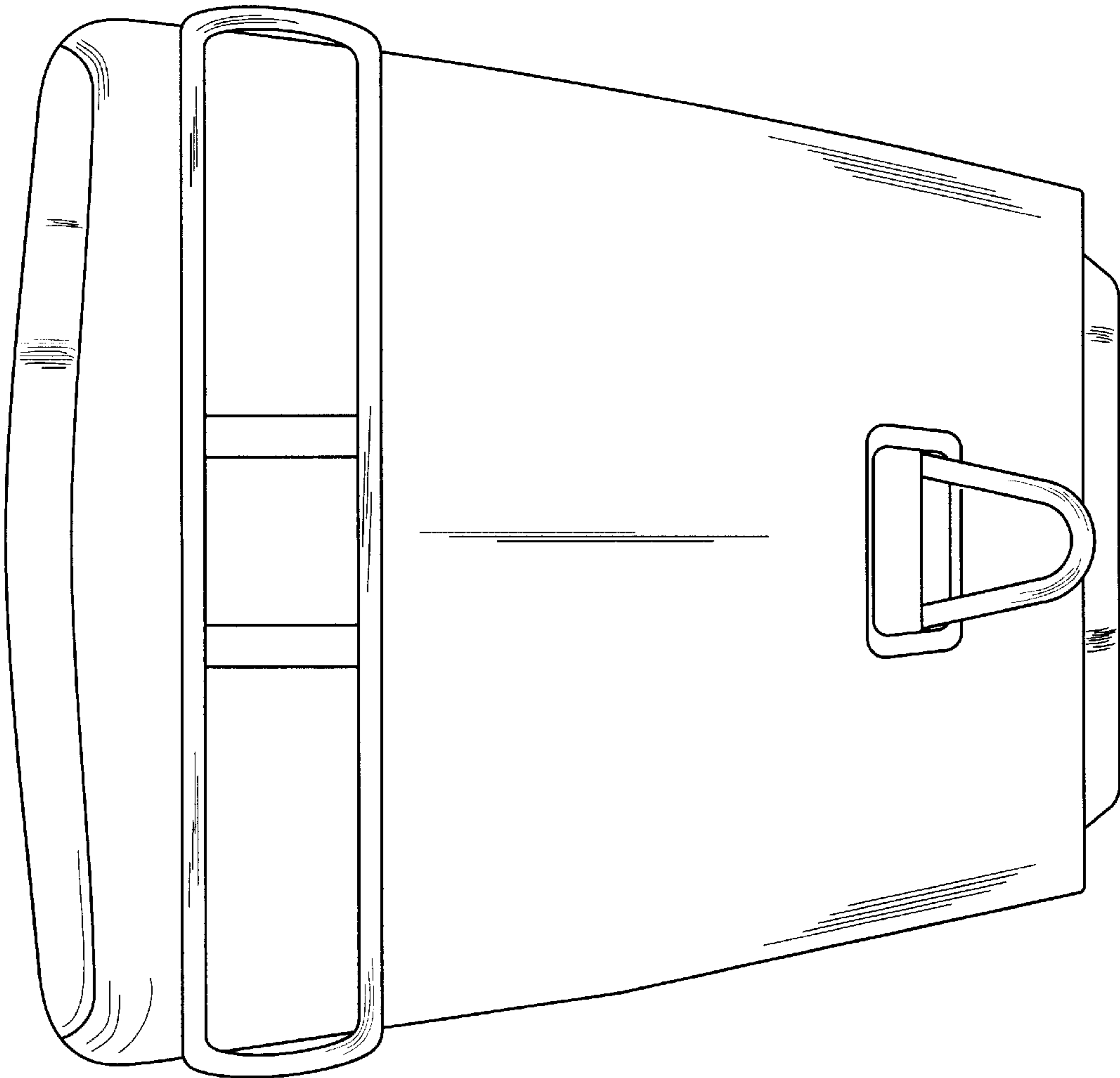


FIG. 4

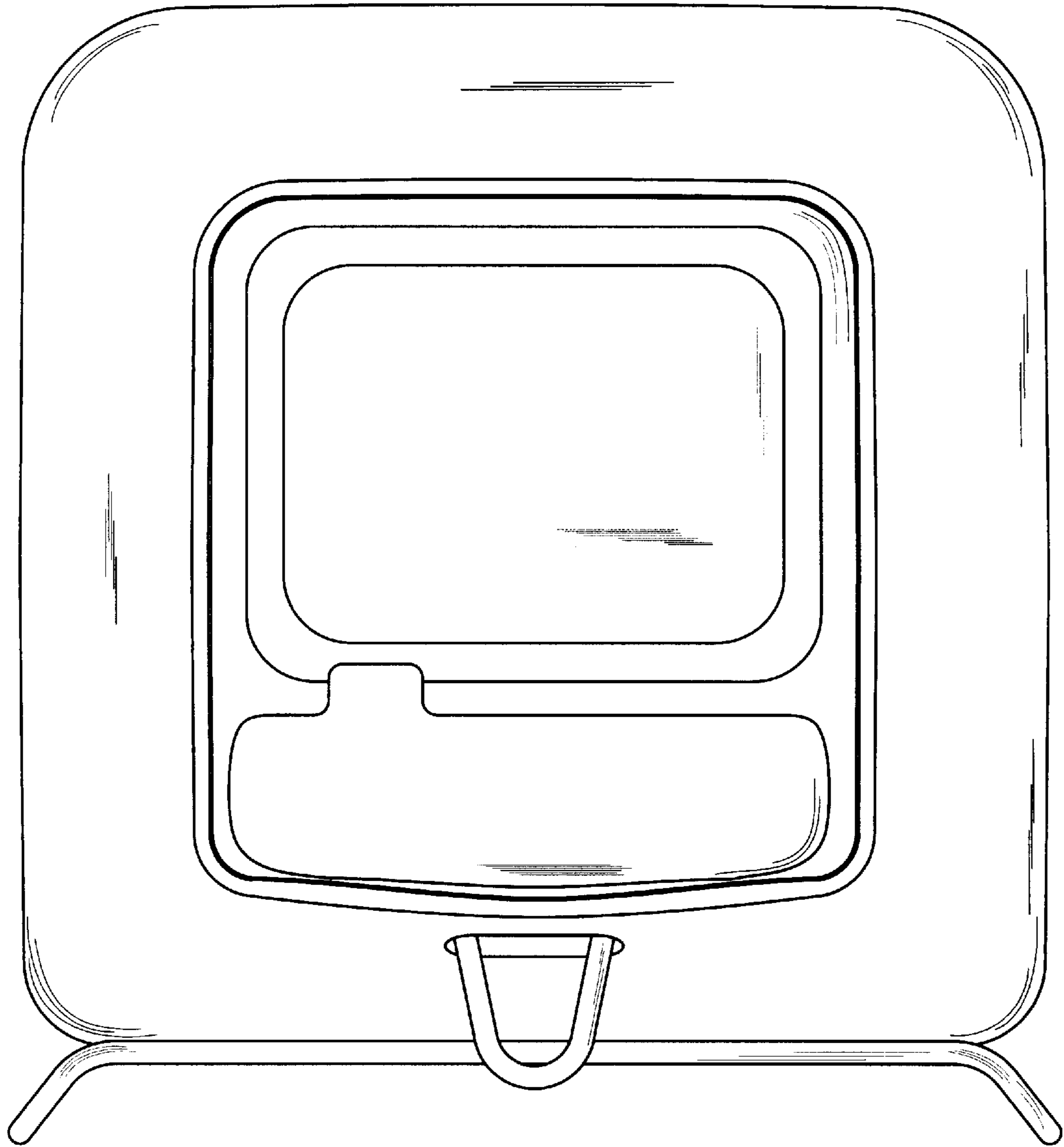


FIG. 5

UNITED STATES PATENT AND TRADEMARK OFFICE  
Certificate

Patent No. D 435,254

Patented: December 19, 2000

On petition requesting issuance of a certificate for correction of inventorship pursuant to 35 U.S.C. 256, it has been found that the above-identified patent, through error and without deceptive intent, improperly sets forth the inventorship.

Accordingly, it is hereby certified that the correct inventorship of this patent is: Arthur L. Gaudette, Richard J. Takahashi, Christopher D. Lucero and Rico L. Zorkendorfer.

Signed and Sealed this First Day of May, 2001.

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