



US00D434418S

**United States Patent** [19]  
**Shinada**

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[45] **Date of Patent: \*\* Nov. 28, 2000**

[54] **IC MODULE**

[75] **Inventor: Satoshi Shinada, Nagano, Japan**

[73] **Assignee: Seiko Epson Corporation, Tokyo, Japan**

[\*\*] **Term: 14 Years**

[21] **Appl. No.: 29/111,928**

[22] **Filed: Oct. 6, 1999**

[30] **Foreign Application Priority Data**

Apr. 6, 1999 [JP] Japan ..... 11-8901

[51] **LOC (7) Cl. .... 14-02**

[52] **U.S. Cl. .... D14/436**

[58] **Field of Search ..... D14/432, 435-438; 361/686, 728, 737, 736; D13/182; D19/9-10**

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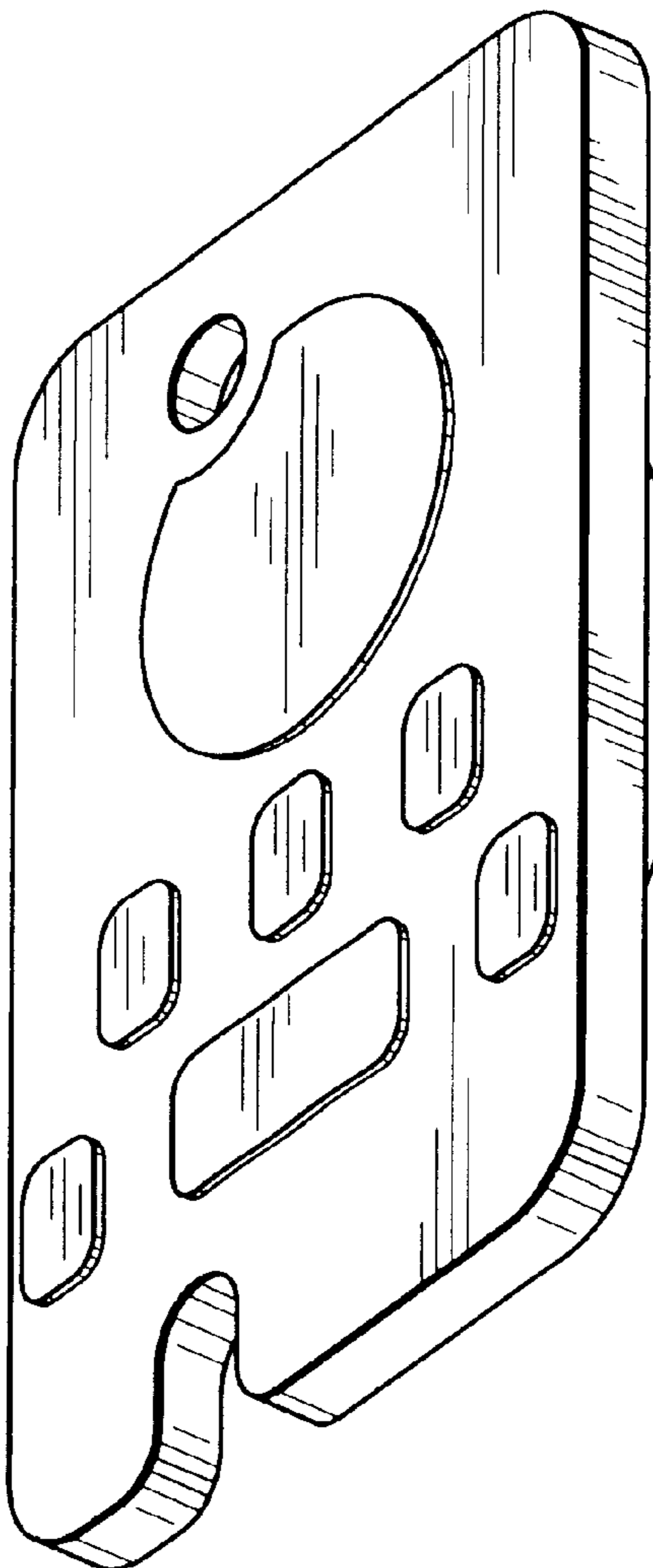
[57] **CLAIM**

The ornamental design for an IC module, as shown and described.

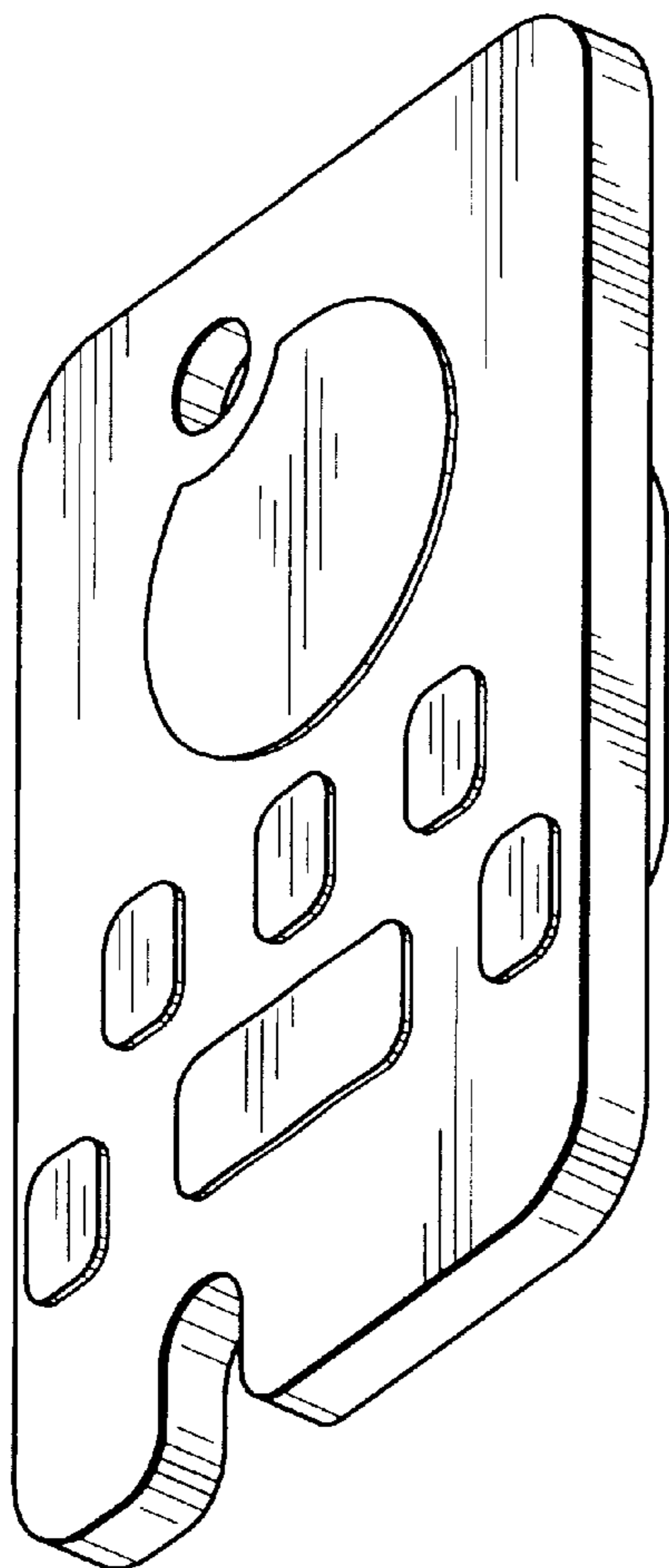
**DESCRIPTION**

FIG. 1 is a perspective view of the front, bottom and right side of an IC module showing my new design;  
 FIG. 2 is a perspective view of the rear, bottom and left side thereof;  
 FIG. 3 is a top plan view thereof;  
 FIG. 4 is a bottom plan view thereof;  
 FIG. 5 is a front elevational view thereof;  
 FIG. 6 is a right side elevational view thereof;  
 FIG. 7 is a rear elevational view thereof; and,  
 FIG. 8 is a left side elevational view thereof.

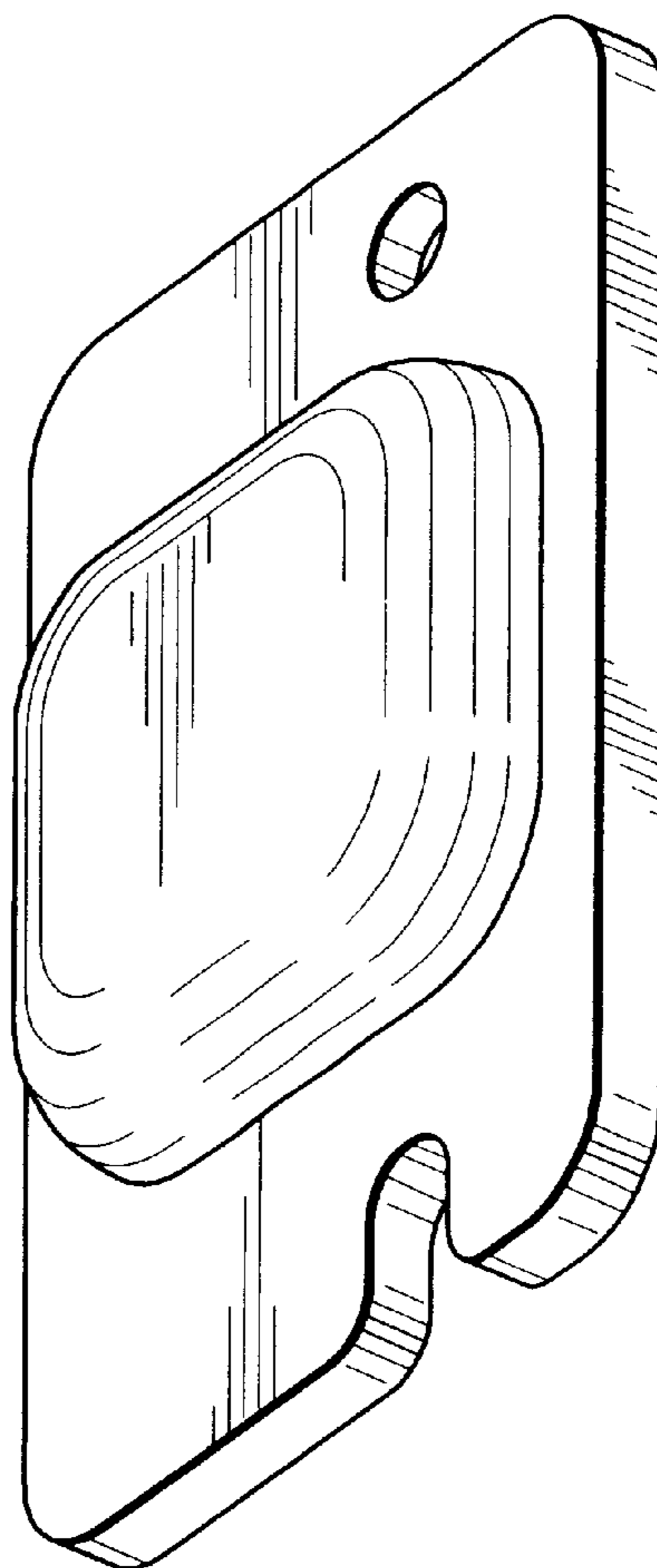
**1 Claim, 2 Drawing Sheets**



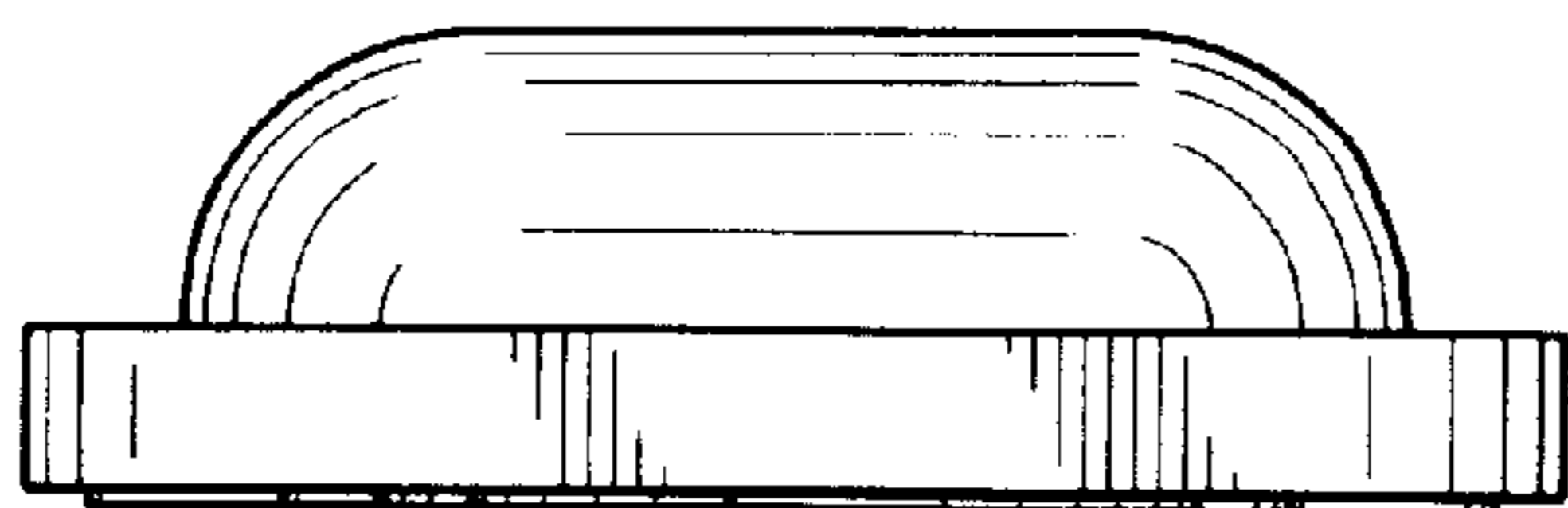
*FIG. 1*



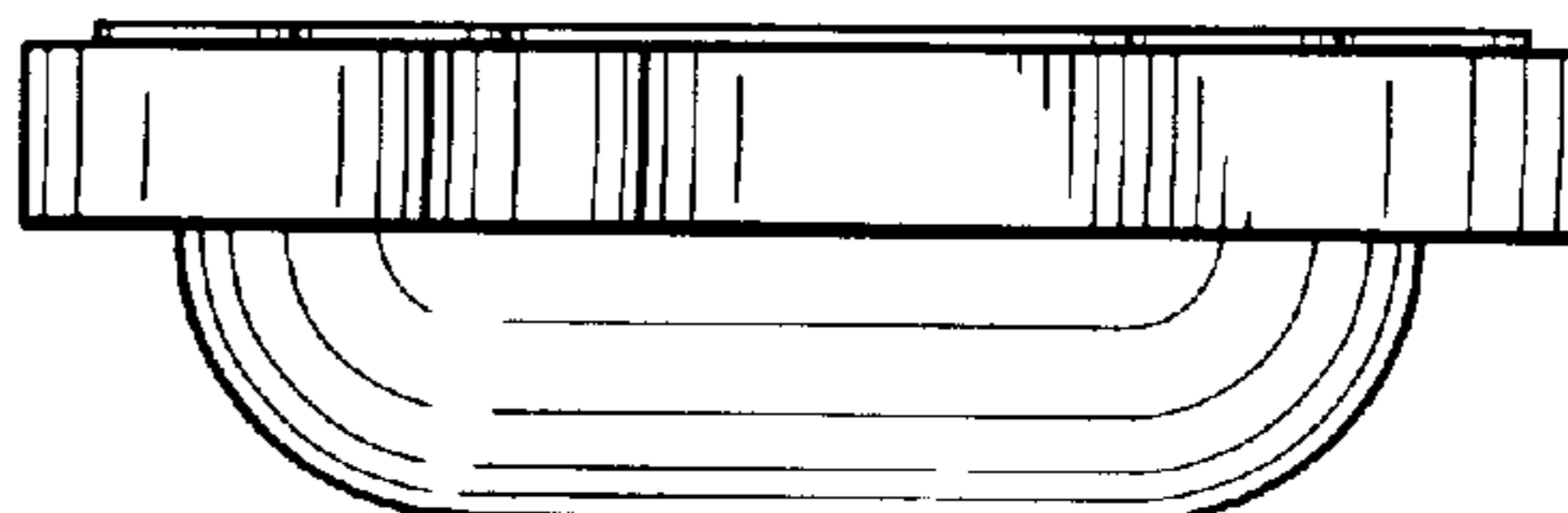
*FIG. 2*



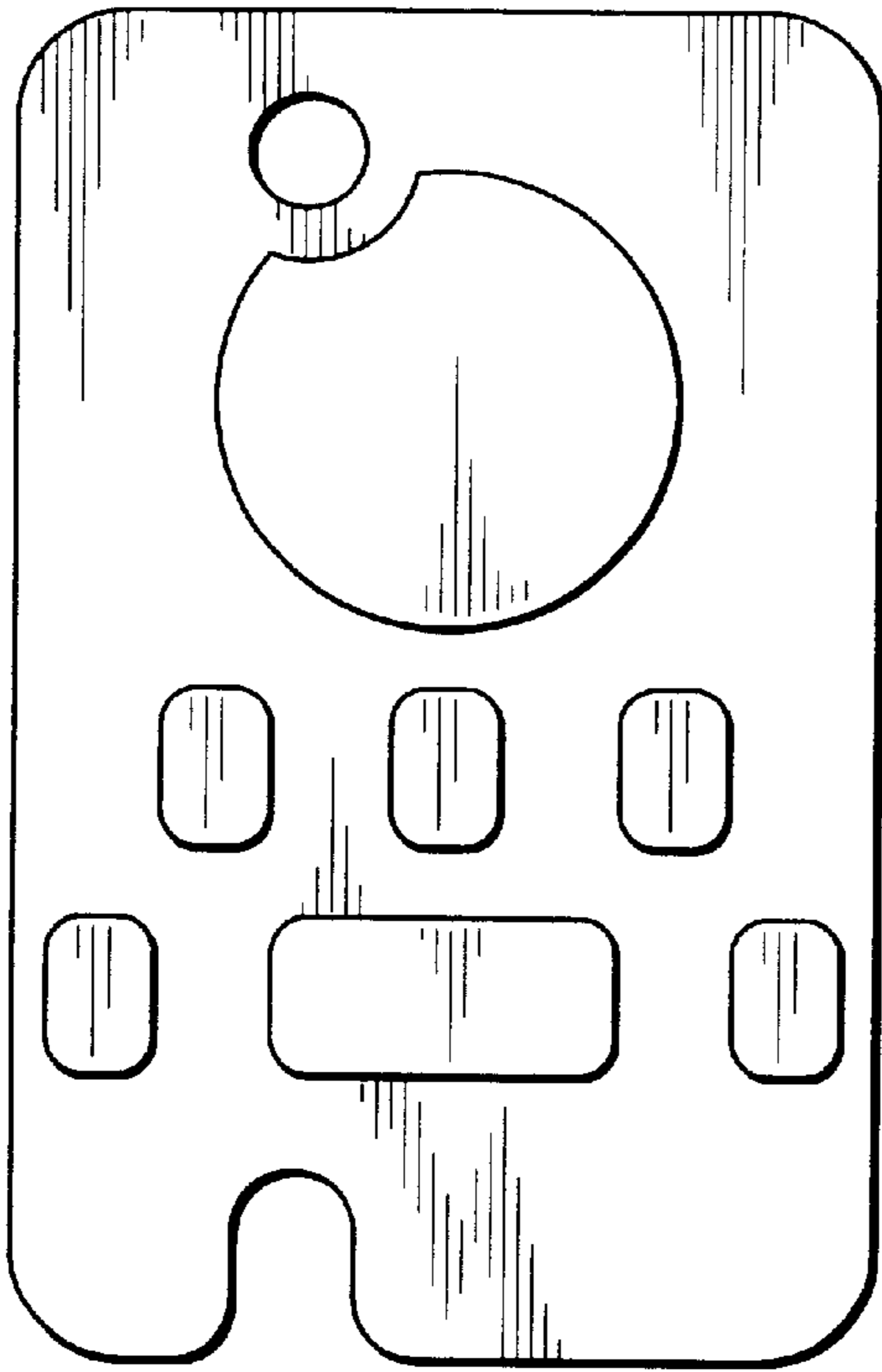
*FIG. 3*



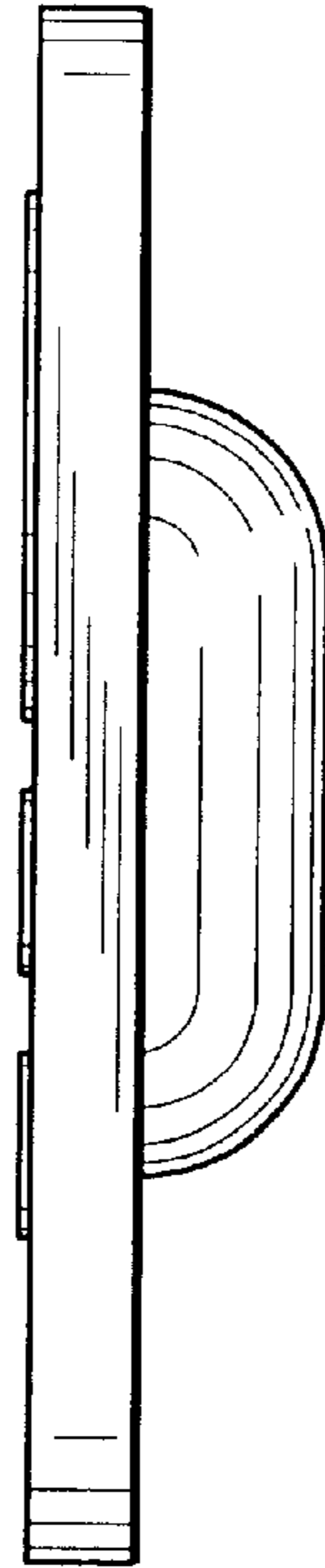
*FIG. 4*



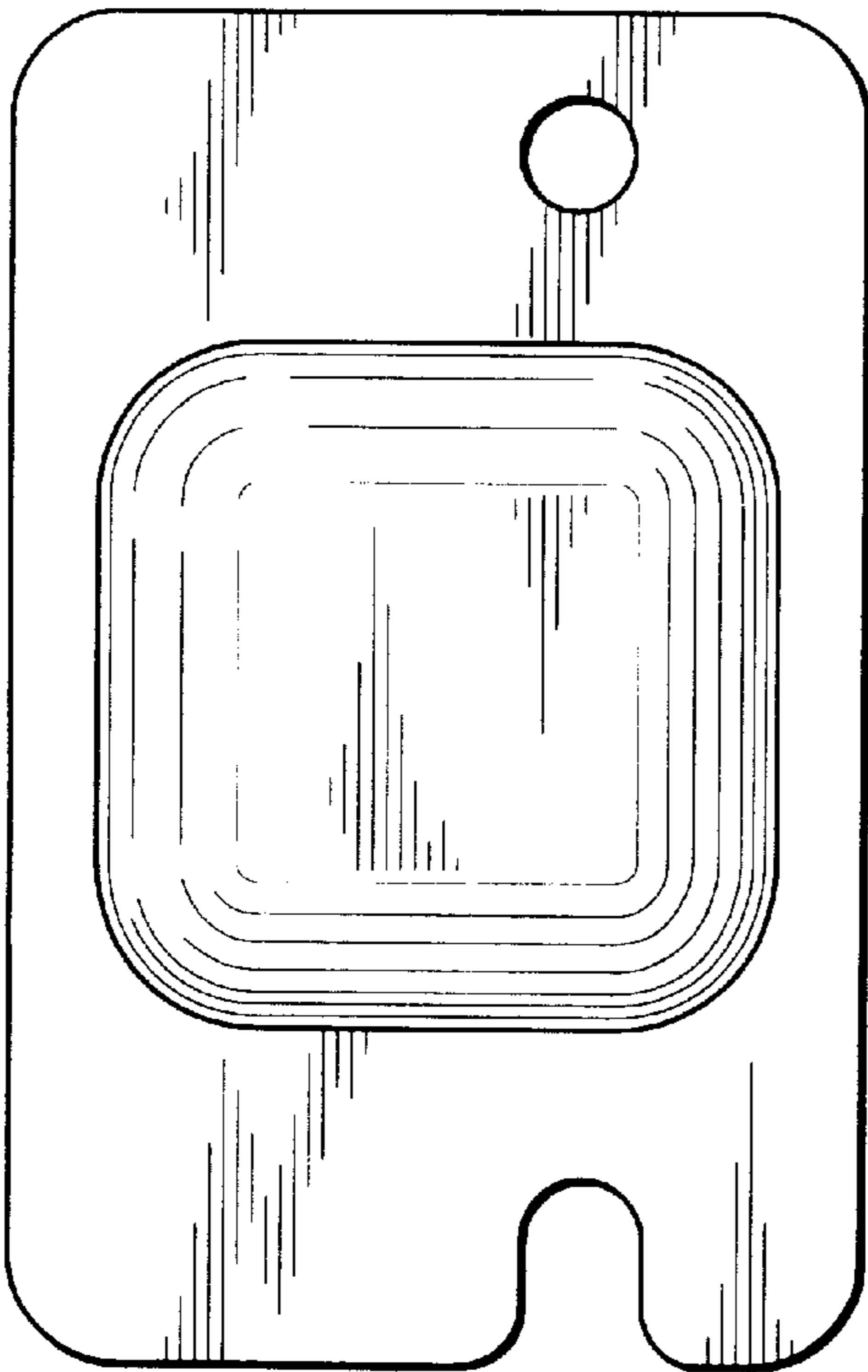
**FIG. 5**



**FIG. 6**



**FIG. 7**



**FIG. 8**

