



US00D429225S

United States Patent [19] Halliday

[11] Patent Number: **Des. 429,225**

[45] Date of Patent: **** Aug. 8, 2000**

[54] **ELECTRONICS HOUSING**

[75] Inventor: **William Muir Halliday**, Bowden, Australia

[73] Assignee: **Gerard Industries PTY LTD**, South Australia, Australia

[**] Term: **14 Years**

[21] Appl. No.: **29/115,738**

[22] Filed: **Dec. 17, 1999**

[30] **Foreign Application Priority Data**

Jun. 18, 1999 [AU] Australia 1910/99

[51] **LOC (7) Cl.** **13-99**

[52] **U.S. Cl.** **D13/184**

[58] **Field of Search** D13/184, 179;
361/656, 724, 728, 684, 687; 379/441,
419, 420, 428

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 387,333 12/1997 Pellow et al. D13/184

D. 402,641 12/1997 Hejnen D13/184
4,557,225 12/1985 Sagues et al. 361/684 X
5,446,617 8/1995 Blocker et al. 361/687 X

Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—Klauber & Jackson

[57] **CLAIM**

The ornamental design for an electronics housing, as shown.

DESCRIPTION

FIG. 1 is a top left hand perspective view, showing the electronics housing of my new design;

FIG. 2 is a top plan view thereof;

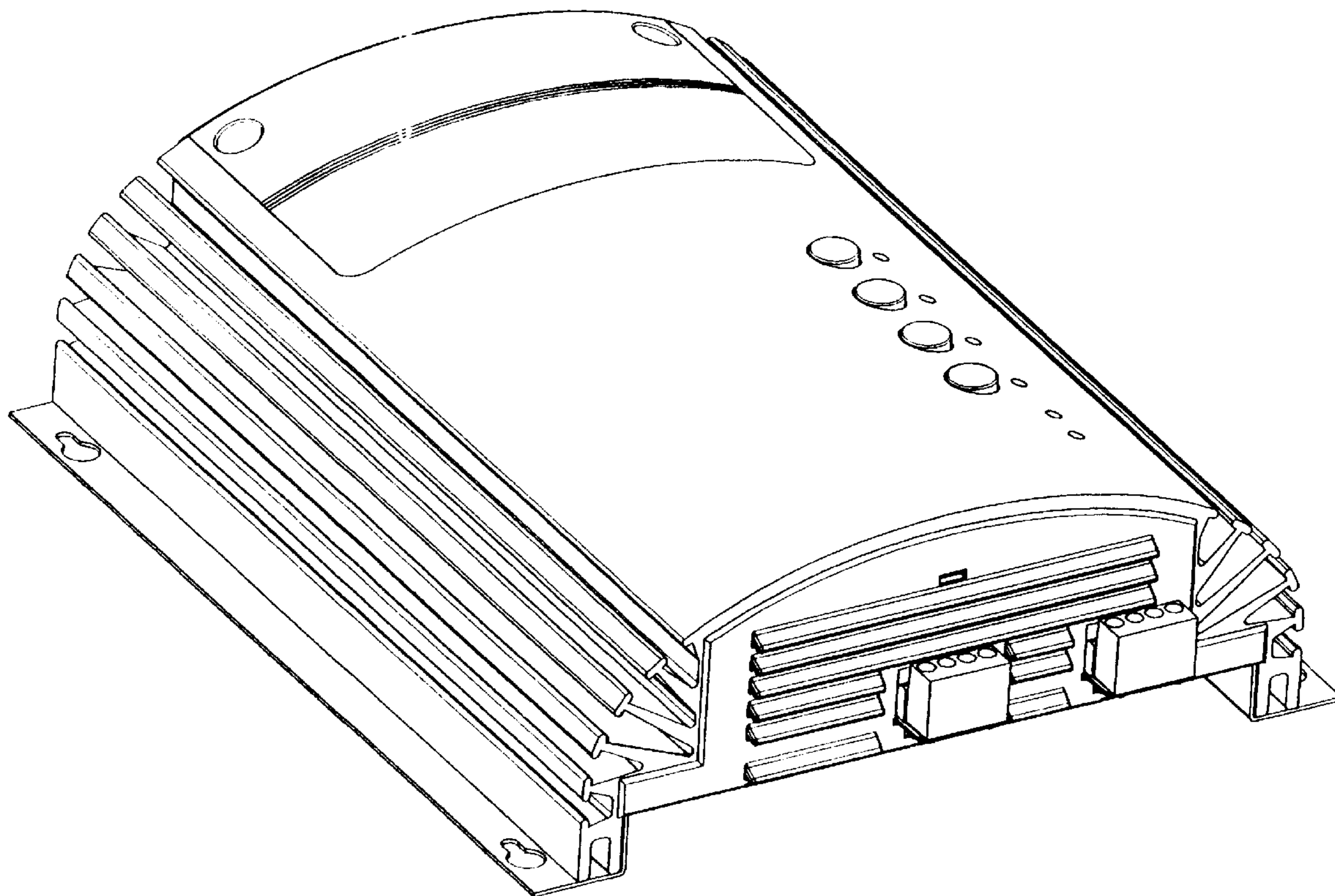
FIG. 3 is a left side elevational view thereof;

FIG. 4 is a front view thereof; and,

FIG. 5 is a rear view thereof.

No claim is made to the bottom of the said electronics housing.

1 Claim, 4 Drawing Sheets



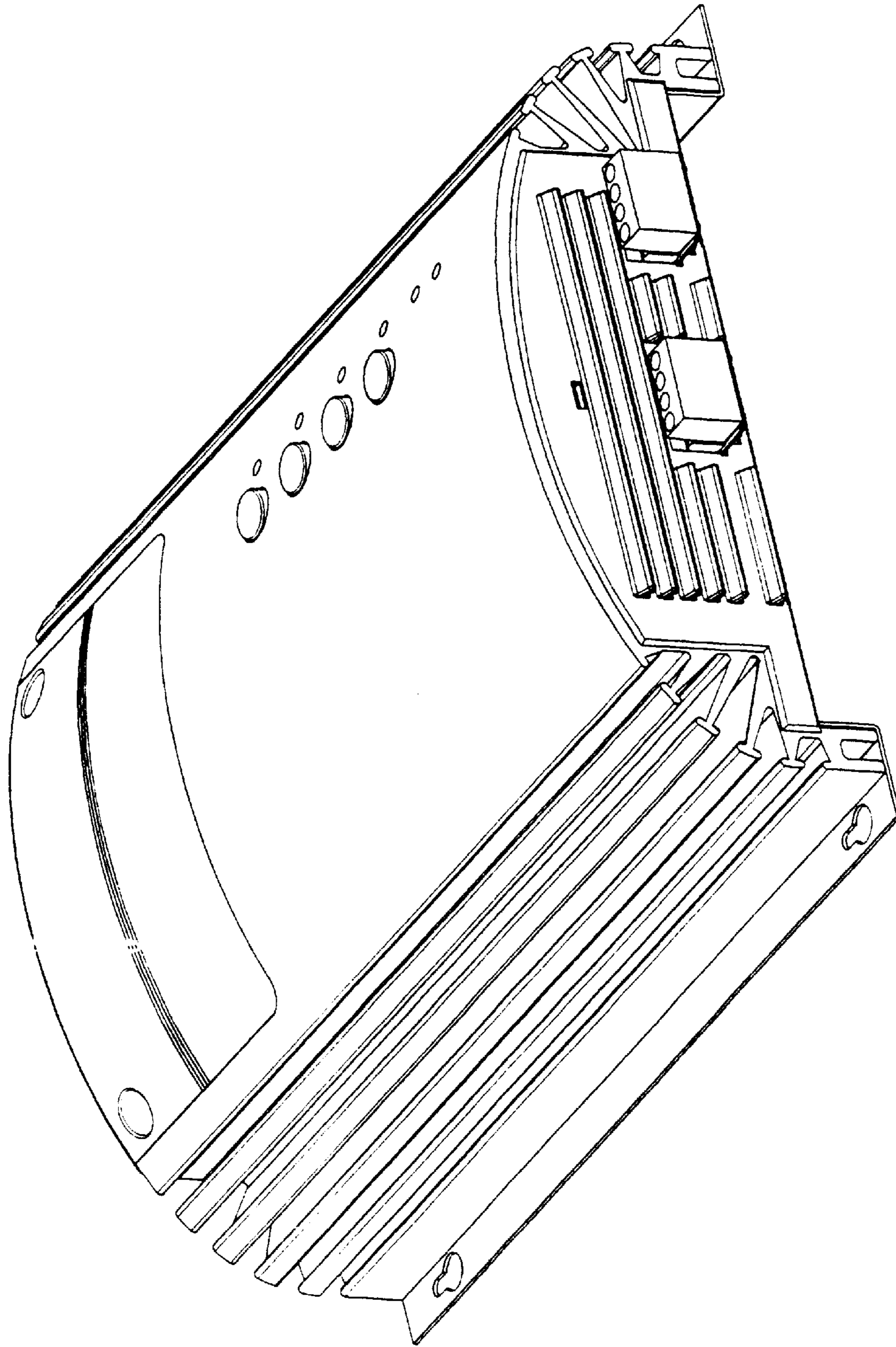


Fig 1

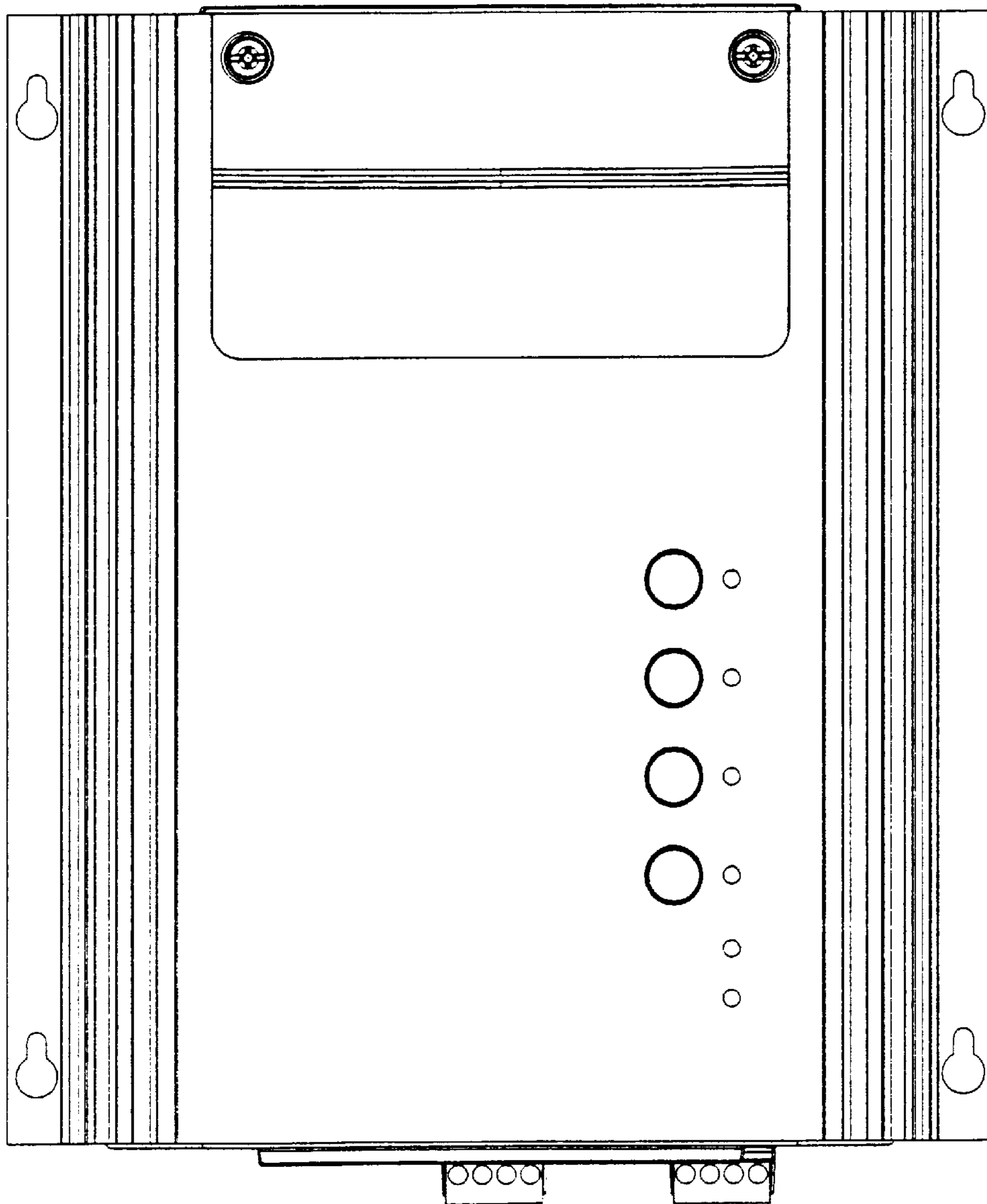


Fig 2

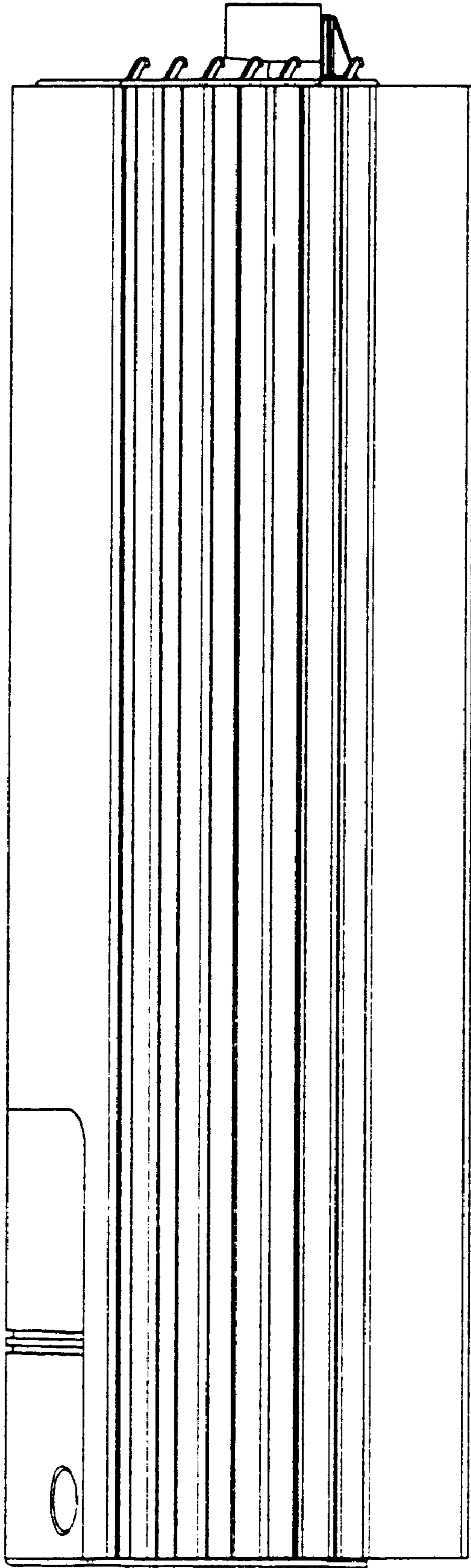


Fig 3

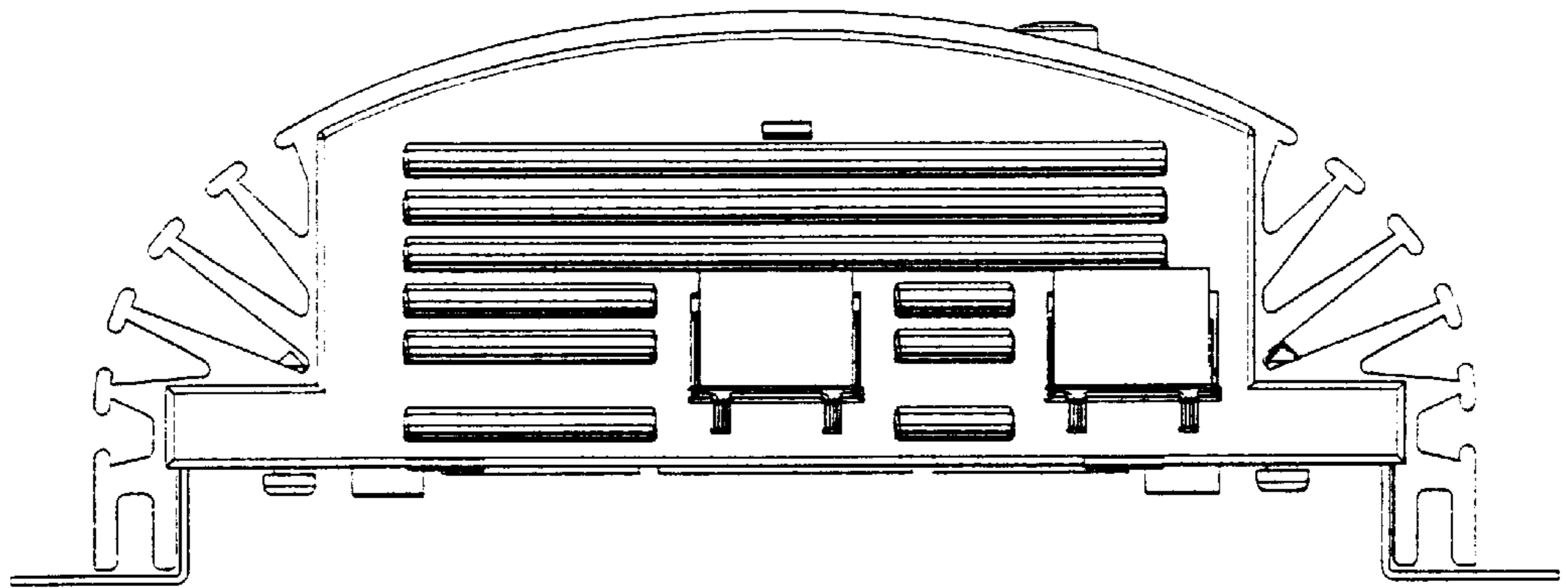


Fig 4

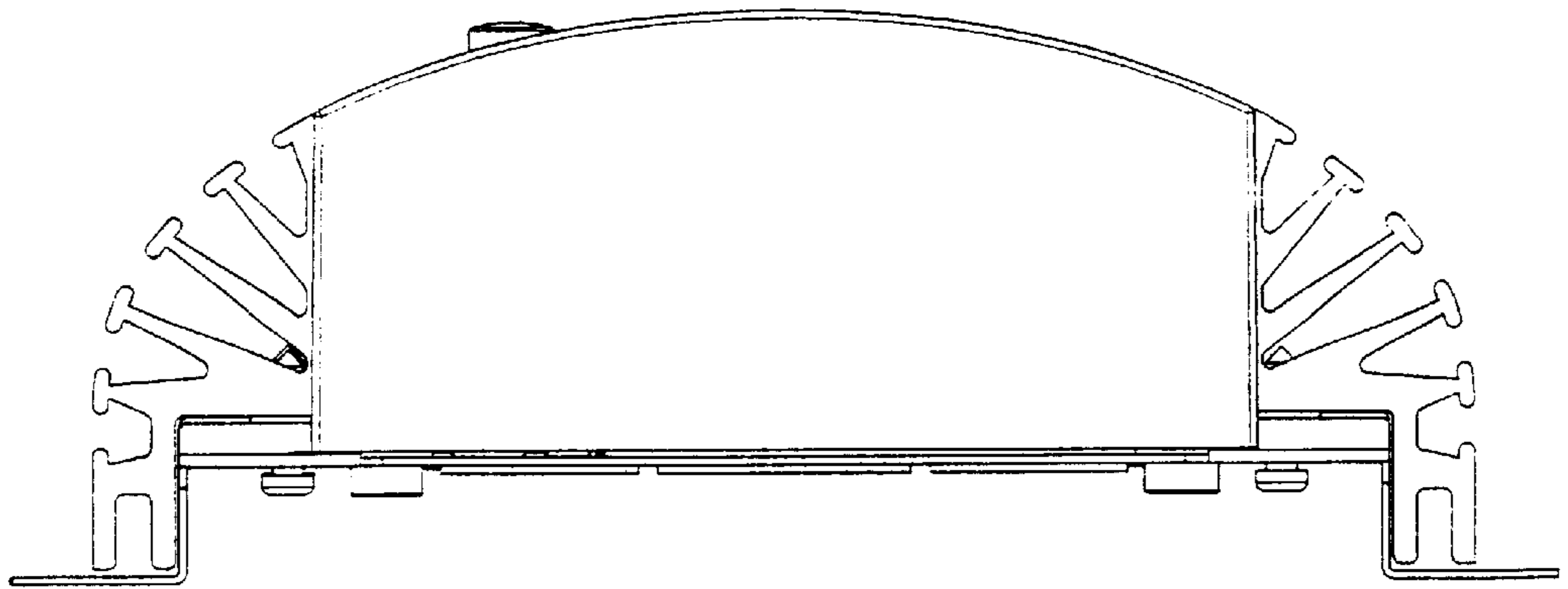


Fig 5