



US00D428600S

**United States Patent** [19]  
**Futami et al.**

[11] **Patent Number: Des. 428,600**  
[45] **Date of Patent: \*\* Jul. 25, 2000**

- [54] **I/O (INPUT/OUTPUT) MODULE**
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- [73] Assignee: **Yamatake Corporation**, Tokyo, Japan
- [\*\*] Term: **14 Years**
- [21] Appl. No.: **29/108,945**
- [22] Filed: **Aug. 9, 1999**
- [30] **Foreign Application Priority Data**  
Feb. 15, 1999 [JP] Japan ..... 11-3346
- [51] **LOC (7) Cl.** ..... **13-03**
- [52] **U.S. Cl.** ..... **D13/162; D13/123**
- [58] **Field of Search** ..... D13/123, 162, D13/162.1, 147, 151; 439/709, 712, 715, 716; 361/637, 823

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[57] **CLAIM**

The ornamental design for an I/O (input/output) module, as shown and described.

**DESCRIPTION**

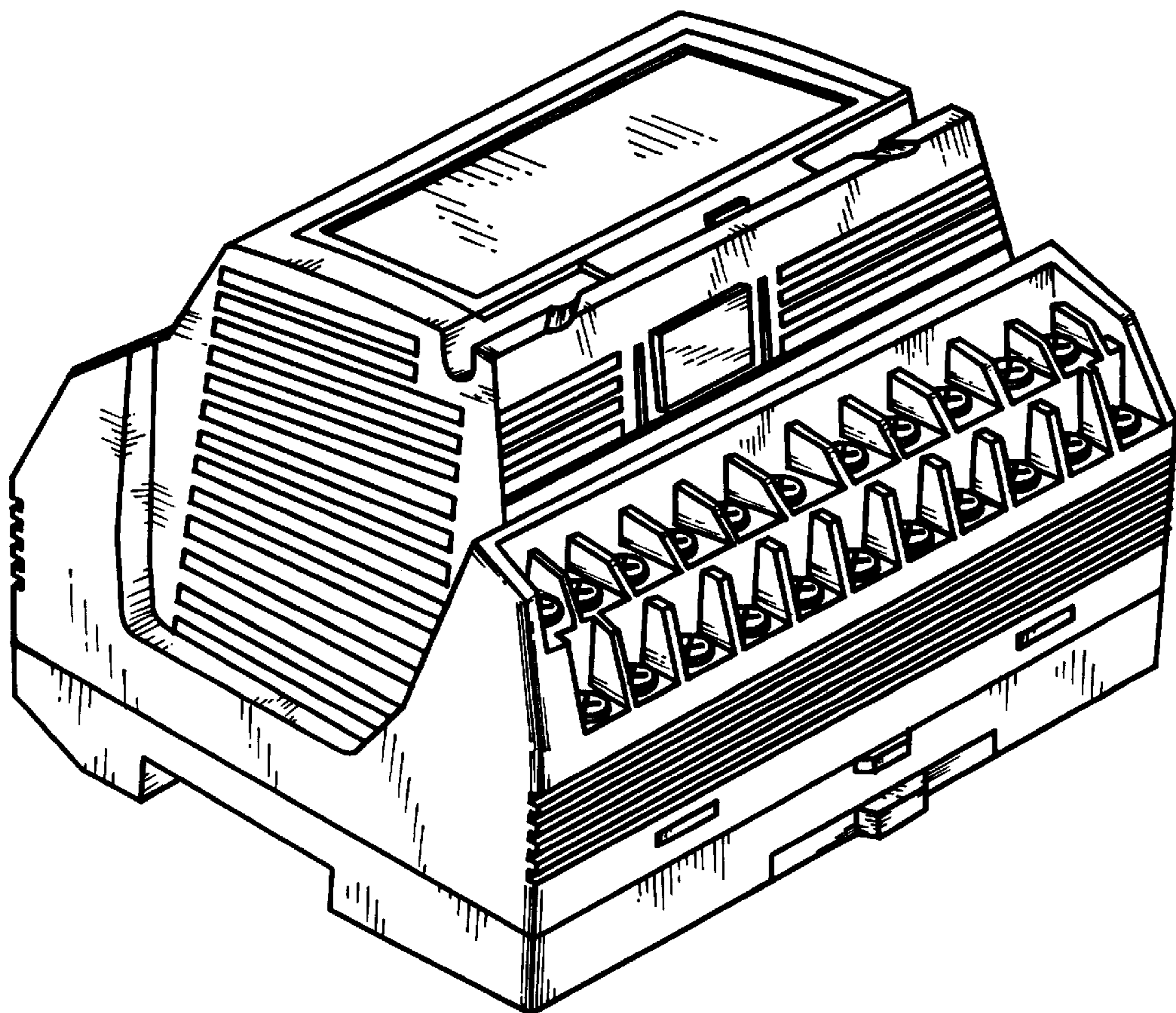
FIG. 1 is a perspective view of an I/O (input/output) module of the design according to the present invention; FIG. 2 is a front view of the I/O (input/output) module of FIG. 1 according to the present invention; FIG. 3 is a rear view of the I/O (input/output) module of FIG. 1 according to the present invention; FIG. 4 is a top plan view of the I/O (input/output) module of FIG. 1 according to the present invention; FIG. 5 is a bottom plan view of the I/O (input/output) module of FIG. 1 according to the present invention; FIG. 6 is a side view of the I/O (input/output) module from the left of FIG. 2 according to the present invention; and, FIG. 7 is a side view of the I/O (input/output) module from the right of FIG. 2 according to the present invention.

[56] **References Cited**

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**1 Claim, 4 Drawing Sheets**



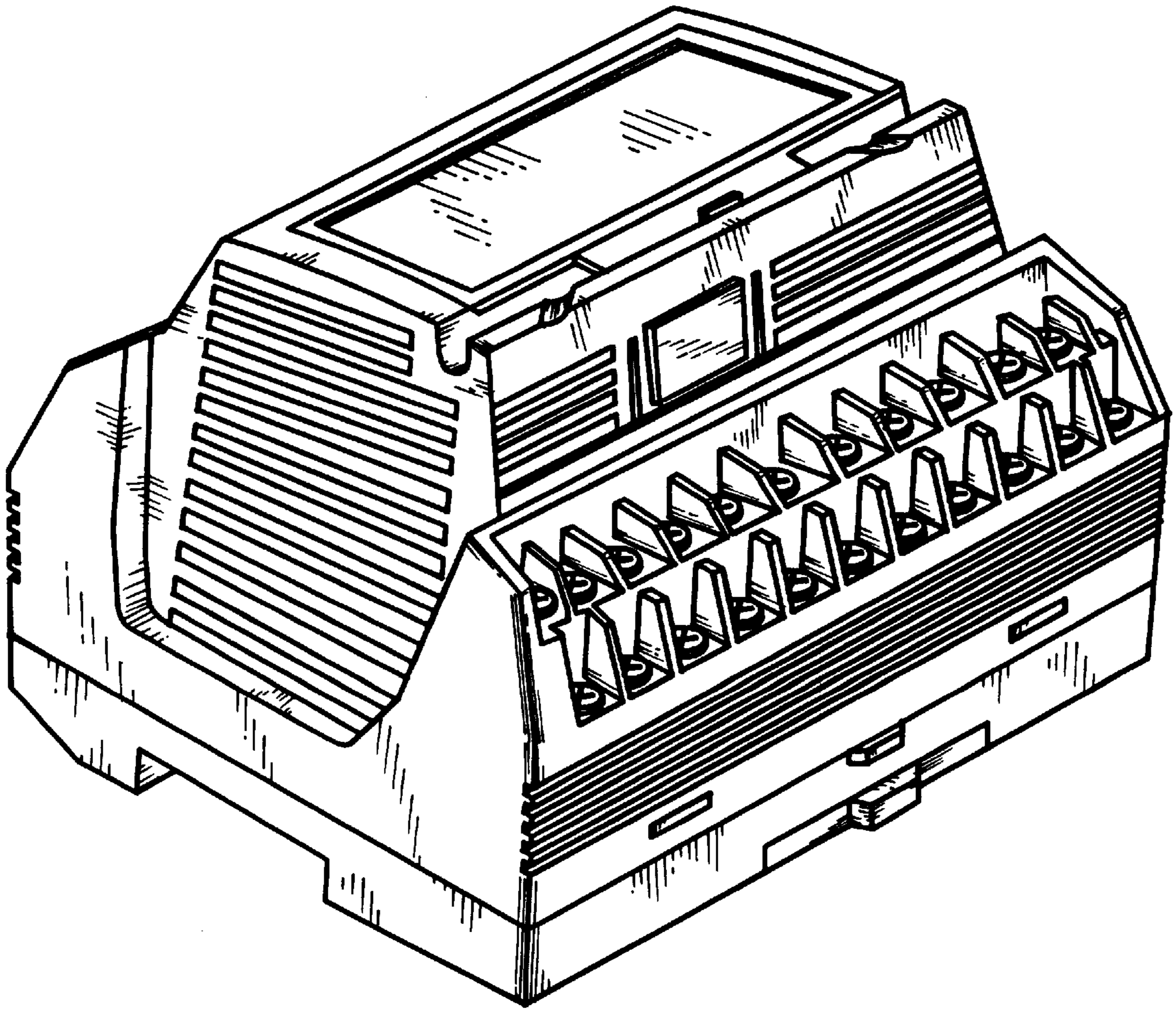


FIG.1



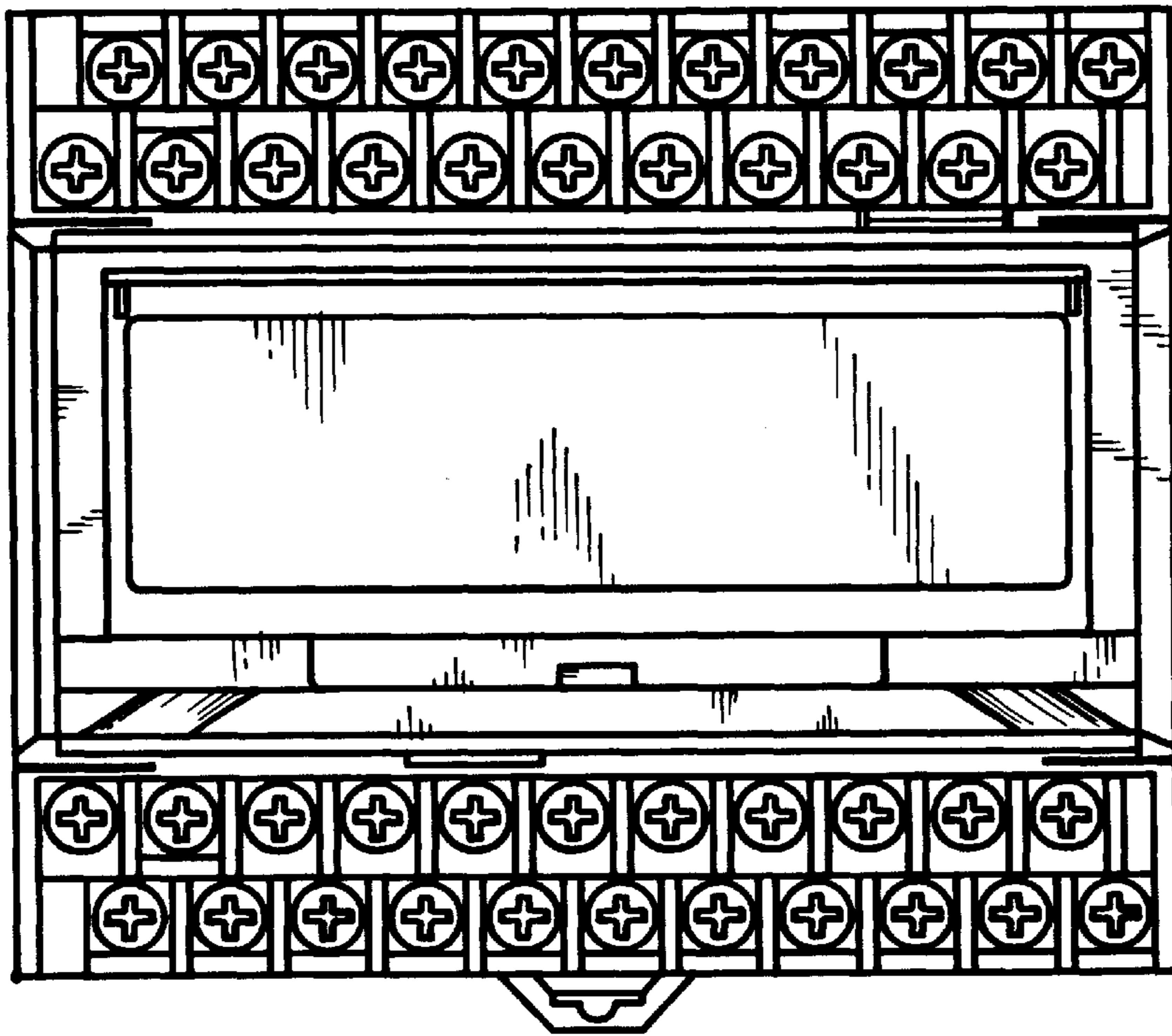


FIG. 2

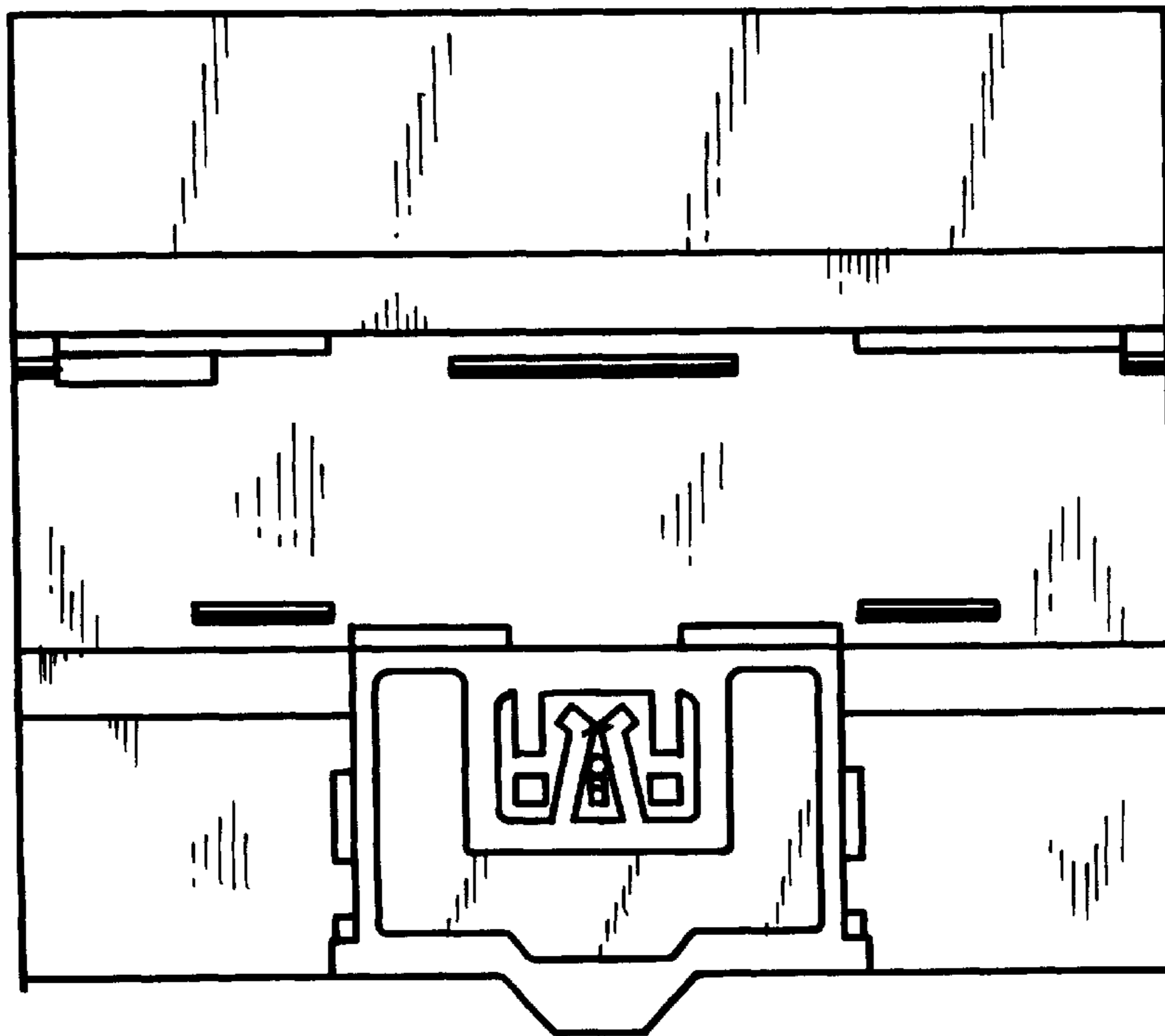


FIG. 3

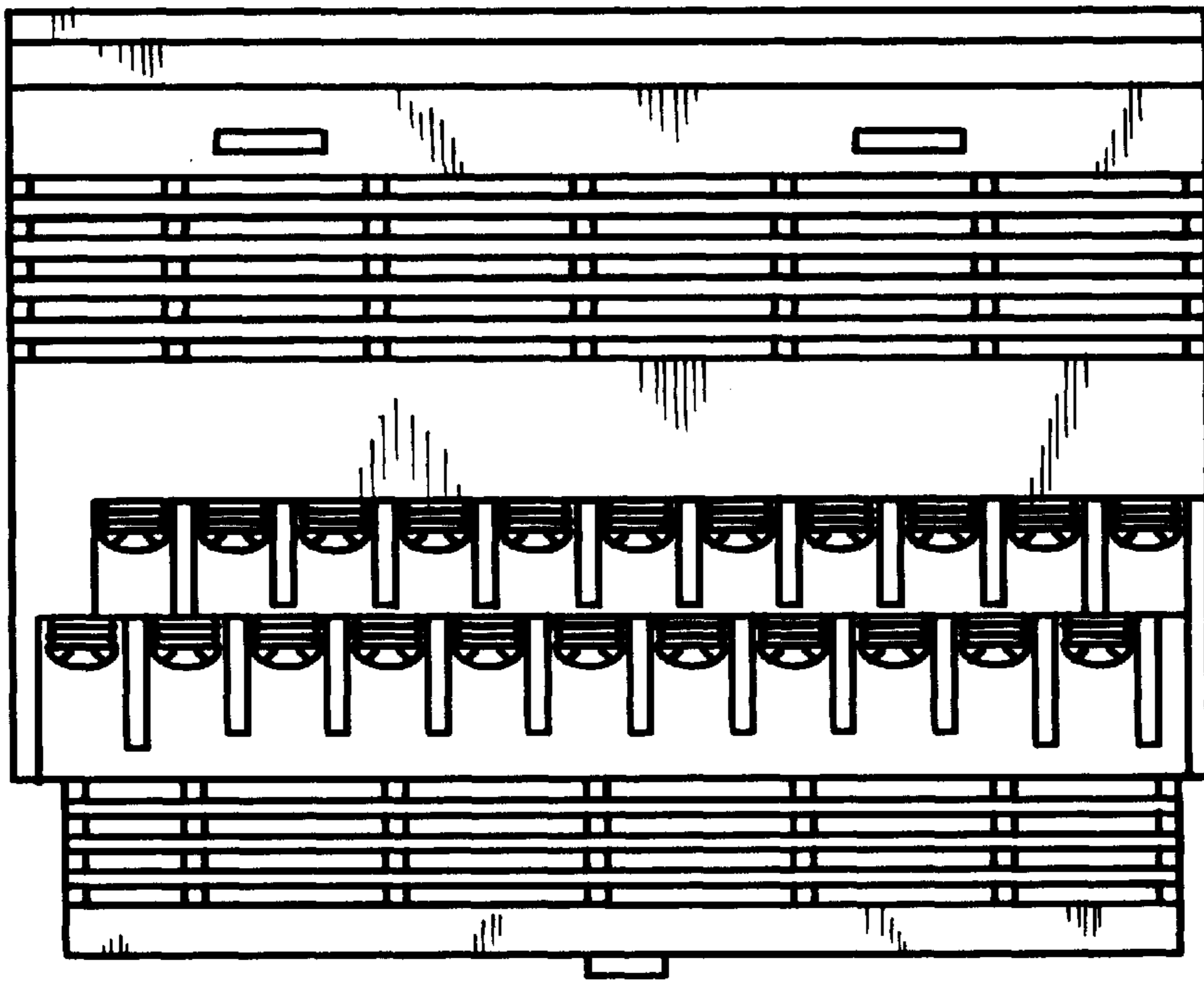


FIG. 4

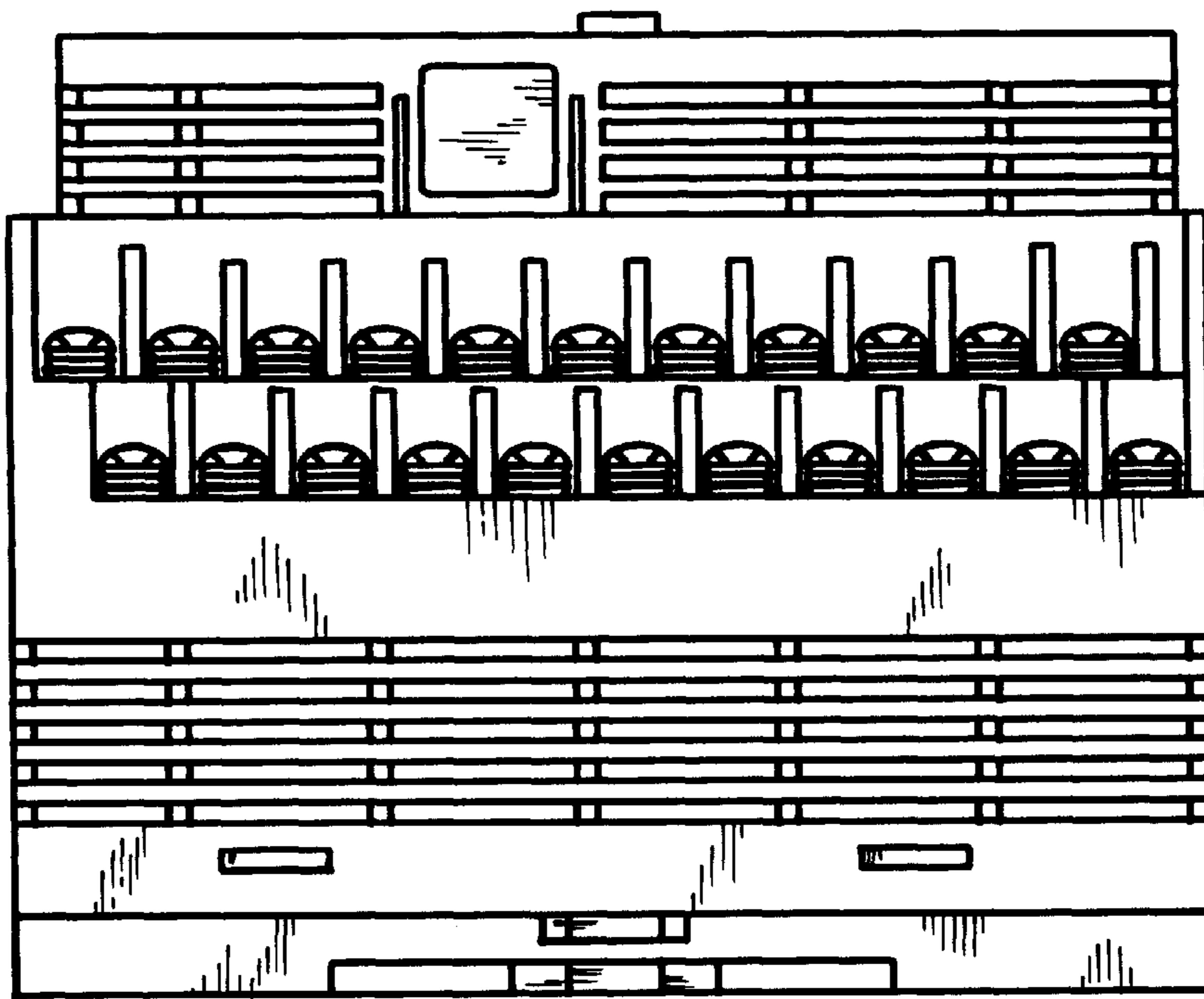


FIG. 5

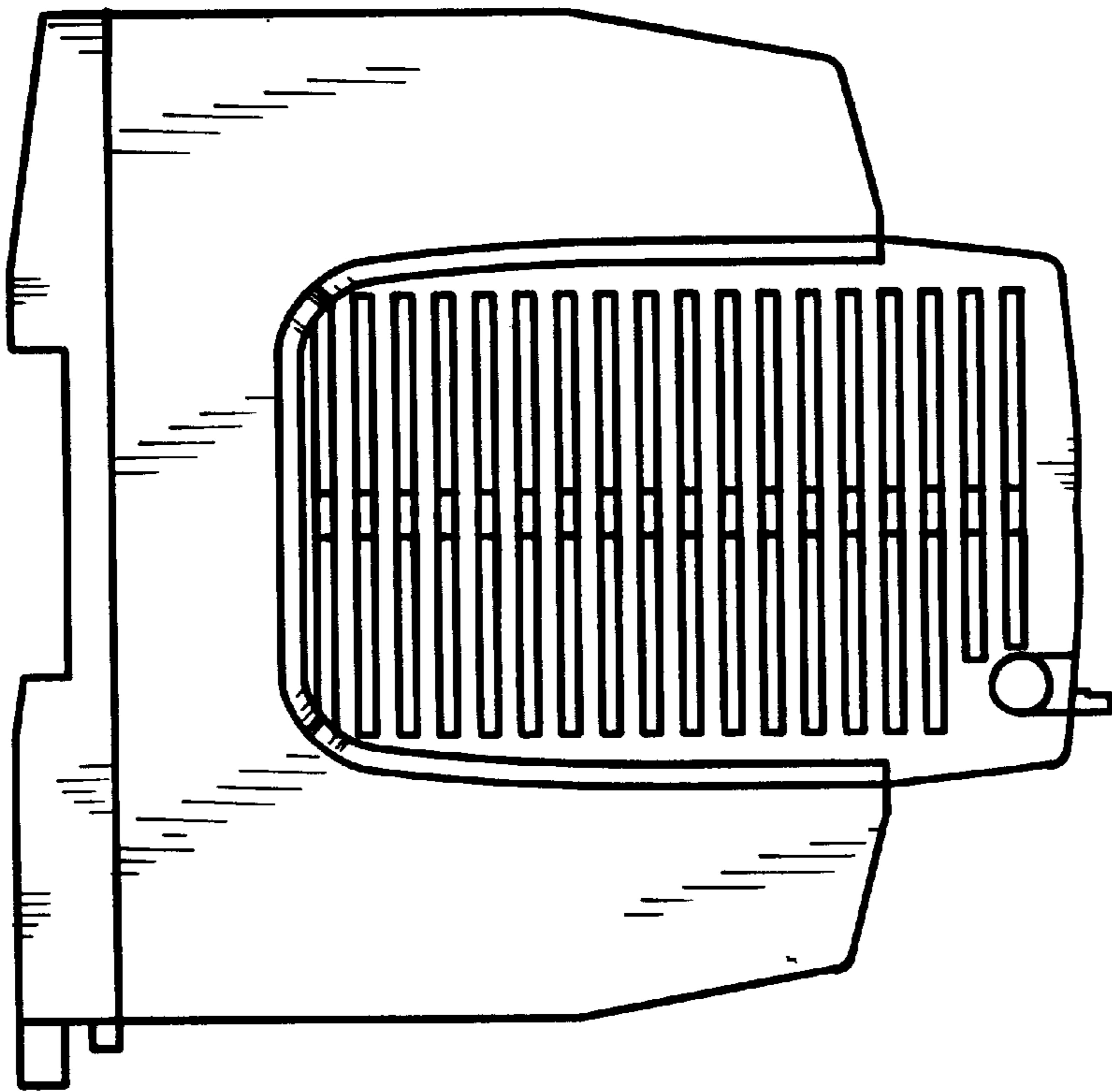


FIG. 6

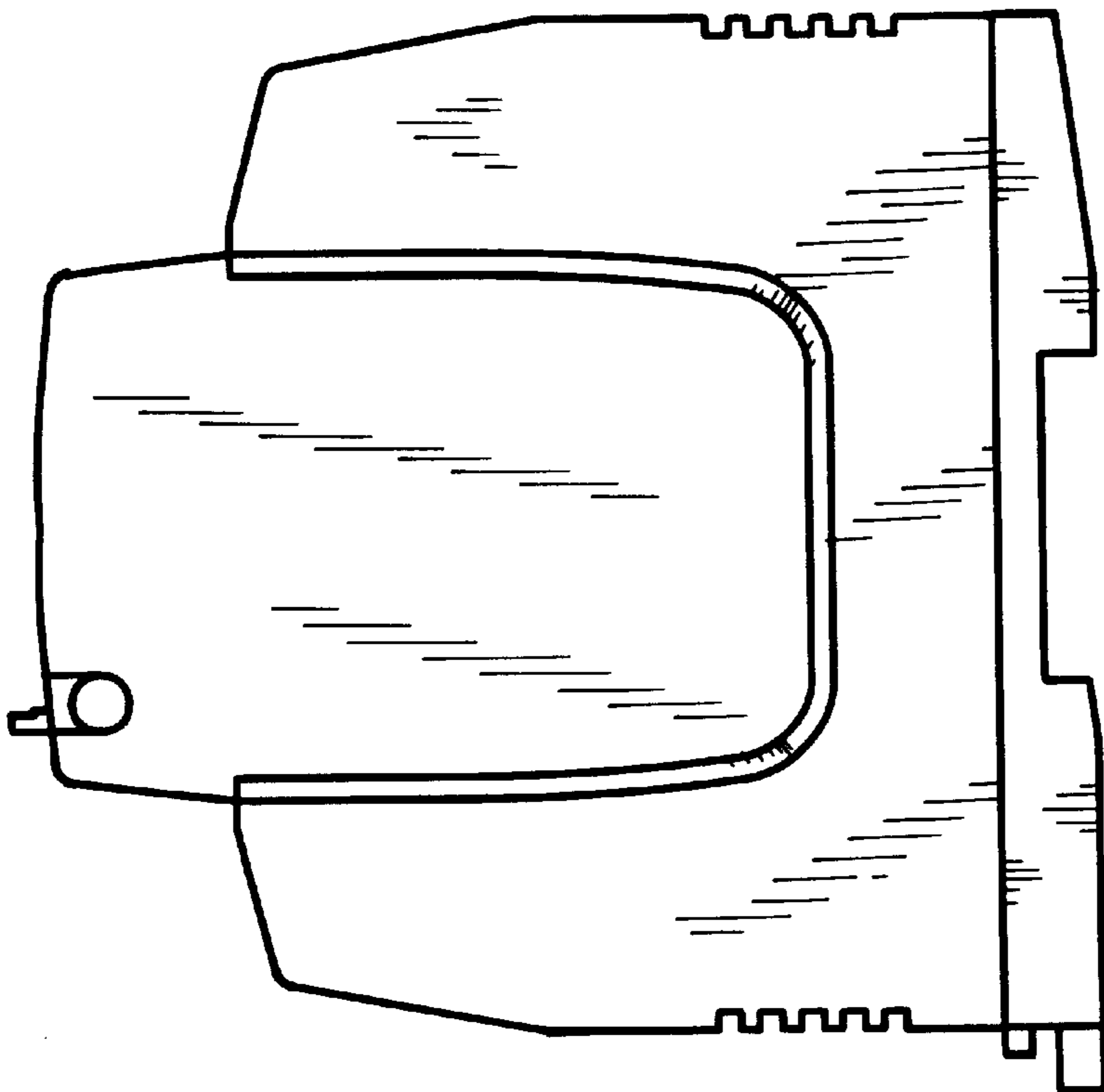


FIG. 7