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United States Patent [19]
Iwasaki

[11] **Patent Number: Des. 427,167**
[45] **Date of Patent: ** Jun. 27, 2000**

[54] **ADAPTER FOR AN IC CARD**

5,986,891 11/1999 Sugimoto 361/737

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FOREIGN PATENT DOCUMENTS

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

923611 4/1995 Japan .

[**] Term: **14 Years**

OTHER PUBLICATIONS

[21] Appl. No.: **29/107,611**

Toshiba, pp. 1-32, "MOS Digital Integrated Circuit Silicon Gate CMOS 128Mbit (16M × 8 bit) CMOS NAND E²PROM (16M Byte SmartMedia™)", Nov. 6, 1998.

[22] Filed: **Jul. 12, 1999**

Toshiba, pp. 1-32, "MOS Digital Integrated Circuit Silicon Gate CMOS 64Mbit (8M × 8 bit) CMOS Nand E²PROM (8M Byte SmartMedia™)", Nov. 6, 1998.

[30] **Foreign Application Priority Data**

Jan. 22, 1999 [JP] Japan 11-1433

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Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[51] **LOC (7) Cl.** **14-02**

[52] **U.S. Cl.** **D14/117**

[58] **Field of Search** D14/114, 117;
D13/182; 235/441-3, 487-92, 486; 361/737,
686; 439/76.1

[57] **CLAIM**

The ornamental design for an adapter for an IC card, as shown.

[56] **References Cited**

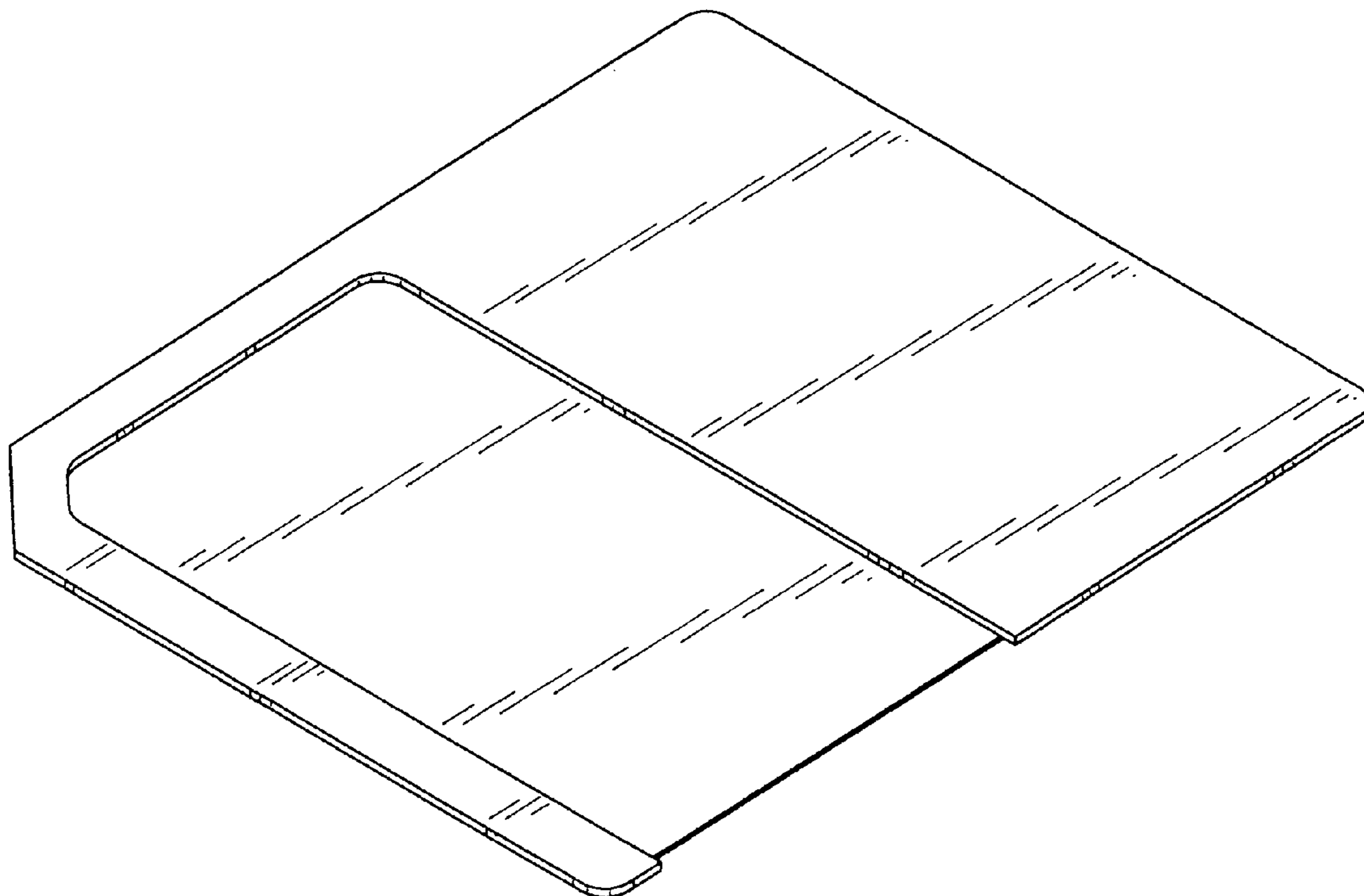
DESCRIPTION

U.S. PATENT DOCUMENTS

| | | | | |
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| D. 267,009 | 11/1982 | Doi | | D14/117 |
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FIG. 1 is a front, bottom and right side perspective view of an adapter for an IC card, showing my new design;
FIG. 2 is a top plan view thereof;
FIG. 3 is a right side elevational view thereof;
FIG. 4 is a front elevational view thereof;
FIG. 5 is a bottom plan view thereof;
FIG. 6 is a left side elevational view thereof; and,
FIG. 7 is a rear elevational view thereof.

1 Claim, 2 Drawing Sheets



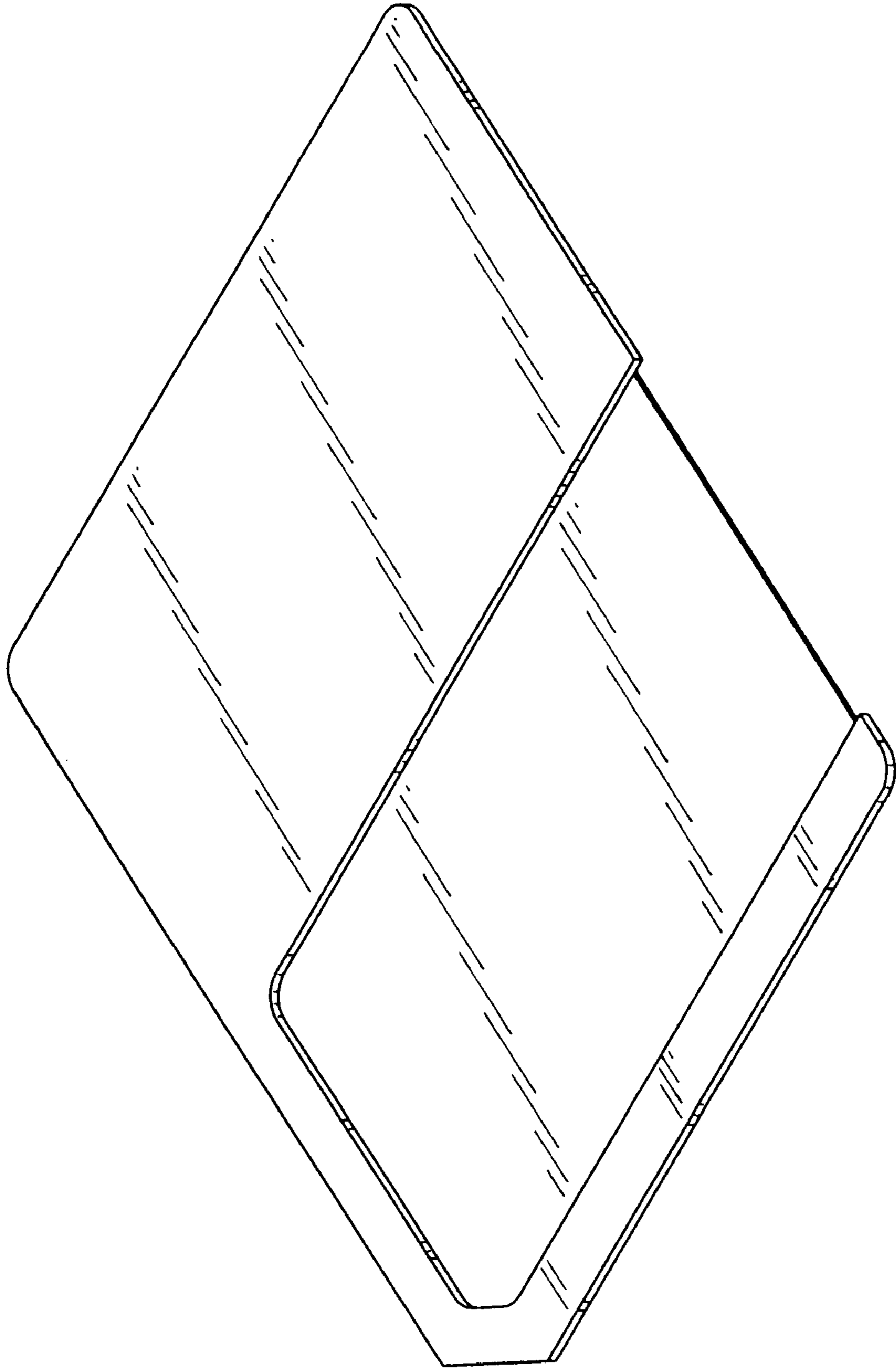


Fig. 1



Fig. 2

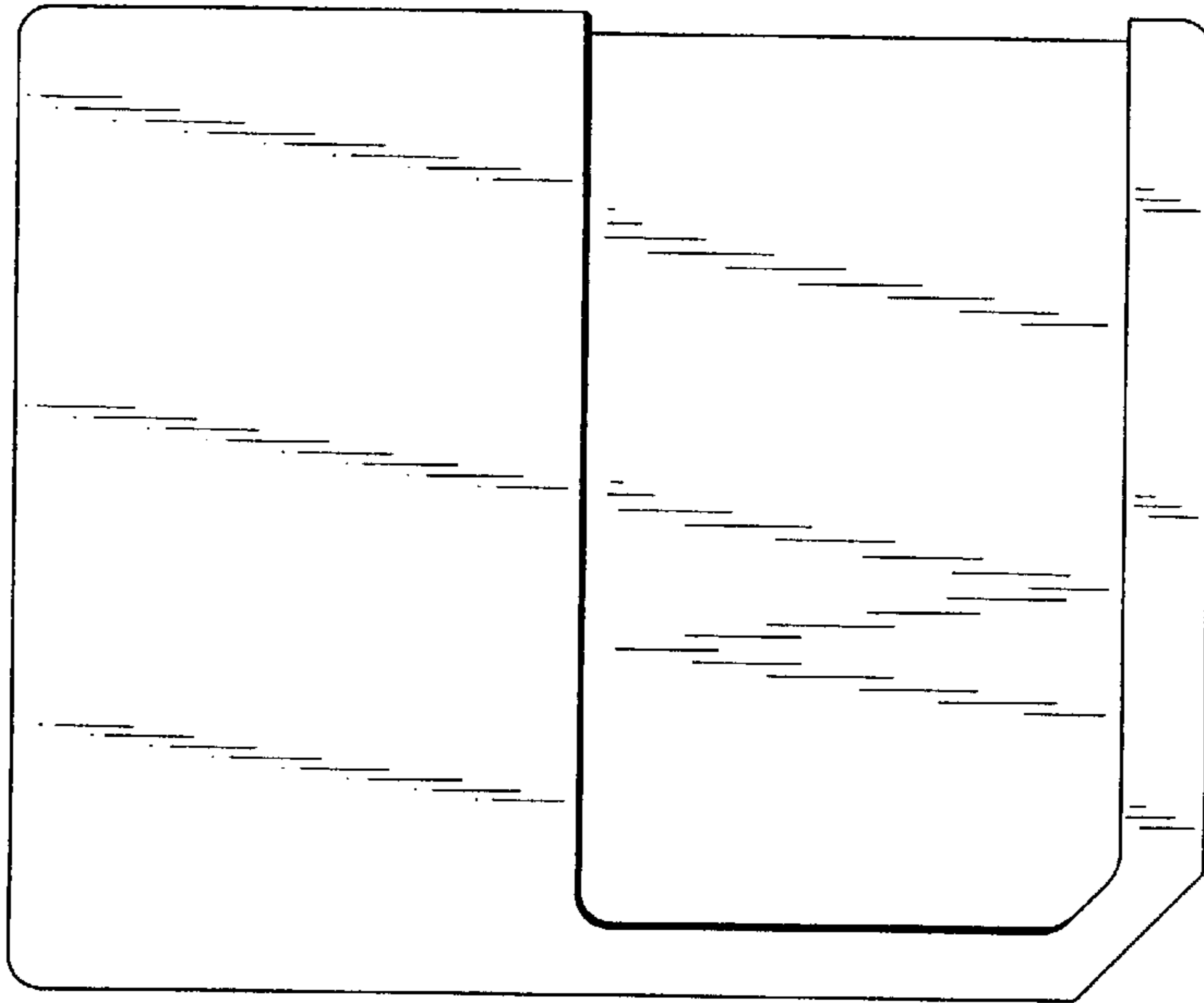


Fig. 4

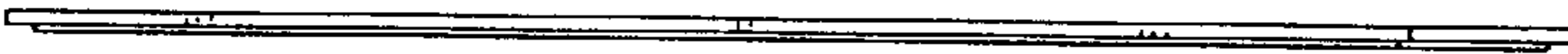


Fig. 6

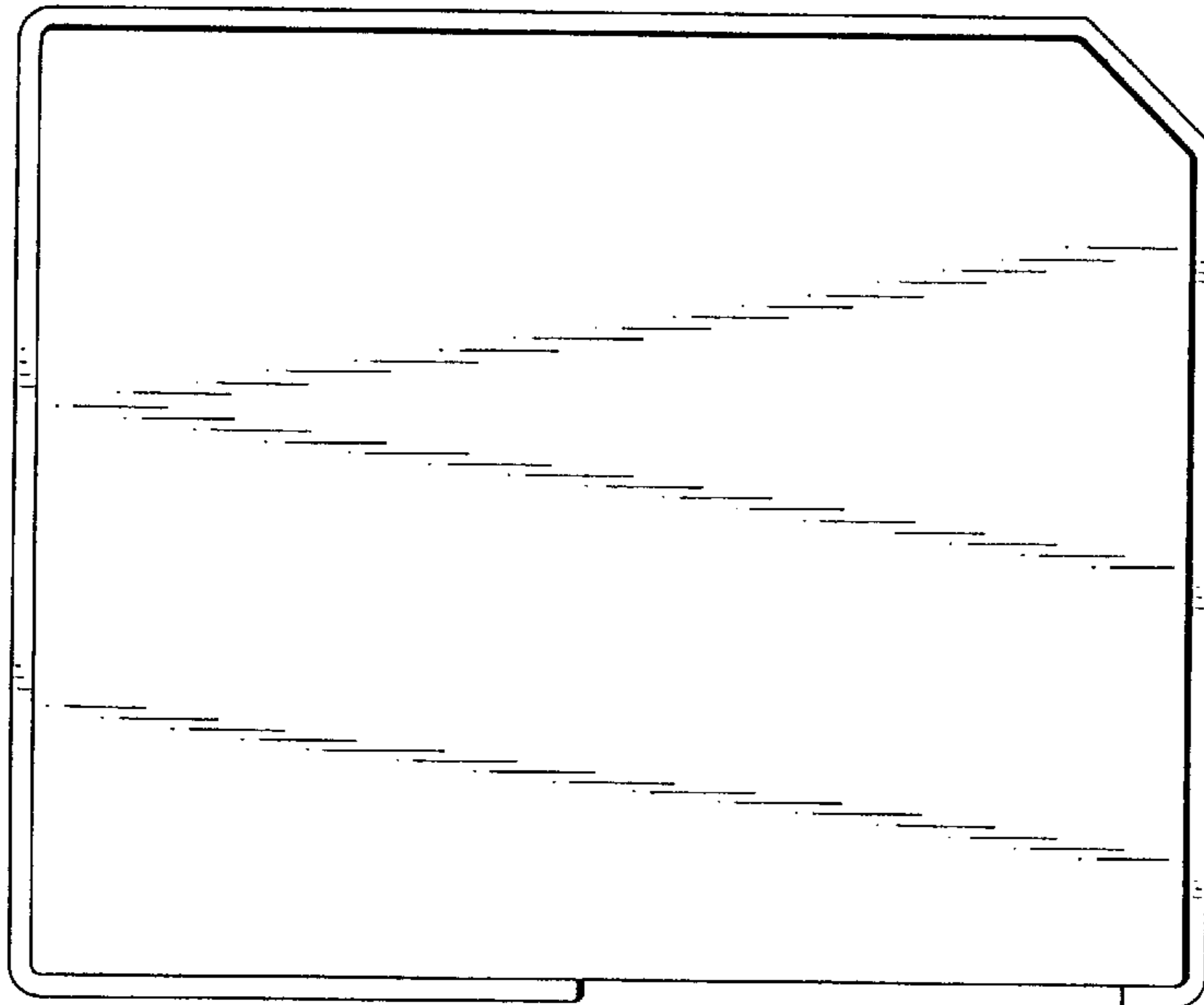


Fig. 7

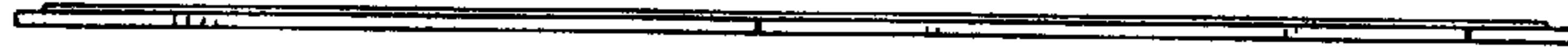


Fig. 3



Fig. 5