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United States Patent [19]

Asai et al.

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[54] **WAFER LEVEL BURN-IN TESTER**

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[73] Assignee: **Matsushita Electric Industrial Co., Ltd., Japan**

[**] Term: **14 Years**

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[30] Foreign Application Priority Data

Jul. 9, 1999 [JP] Japan 11-18322

[51] **LOC (7) Cl.** **10-04**

[52] **U.S. Cl.** **D10/75**

[58] **Field of Search** D10/46, 75; D15/199;
324/754, 765, 755, 758, 763

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[57] CLAIM

The ornamental design for a wafer level burn-in tester, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of the top, front and right side of a wafer level burn-in tester showing our new design; FIG. 2 is a front view thereof; FIG. 3 is a right side view thereof; FIG. 4 is a top plan view thereof; FIG. 5 is a bottom view thereof; and, FIG. 6 is a rear view thereof.

1 Claim, 5 Drawing Sheets

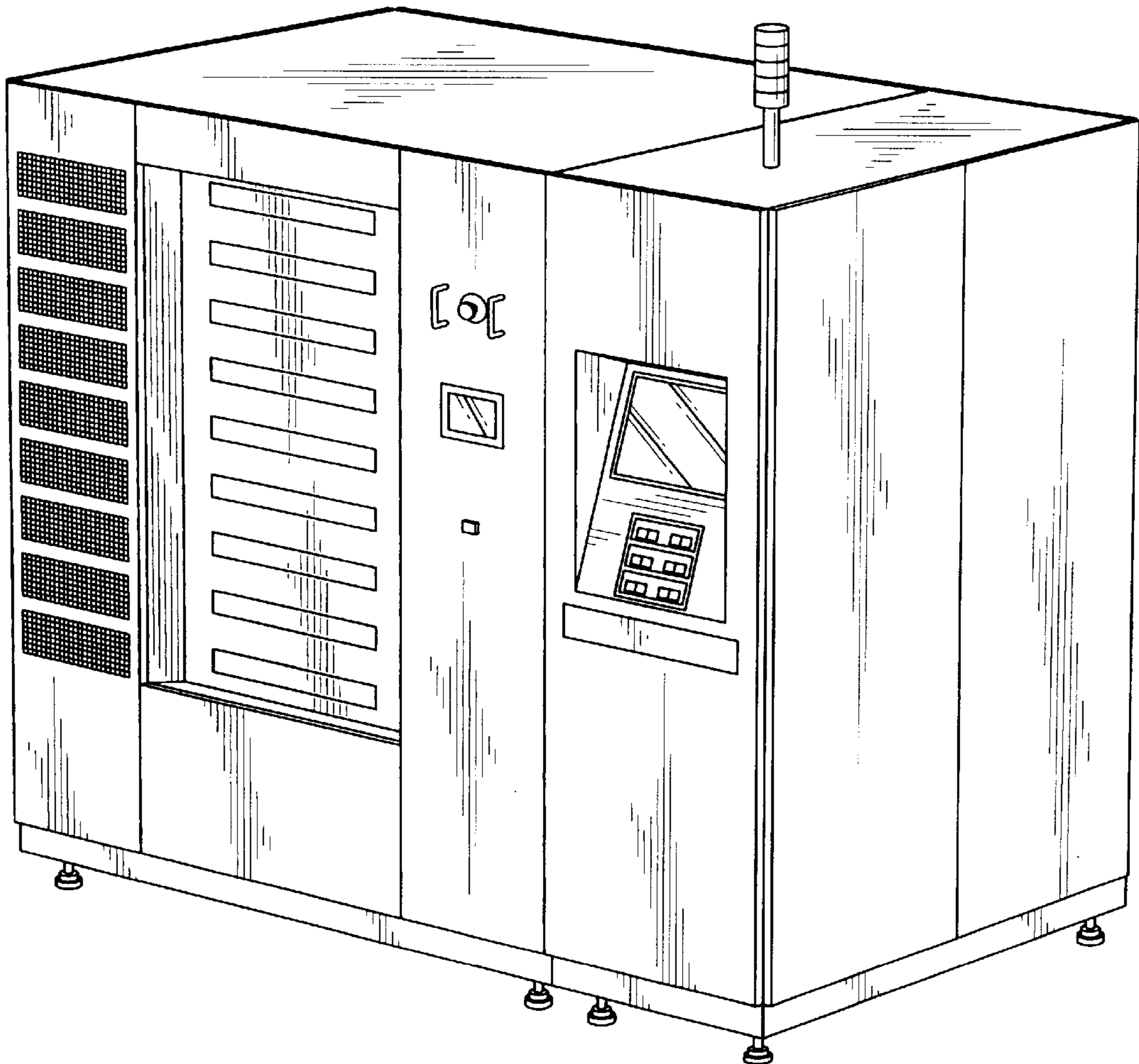


FIG. 1

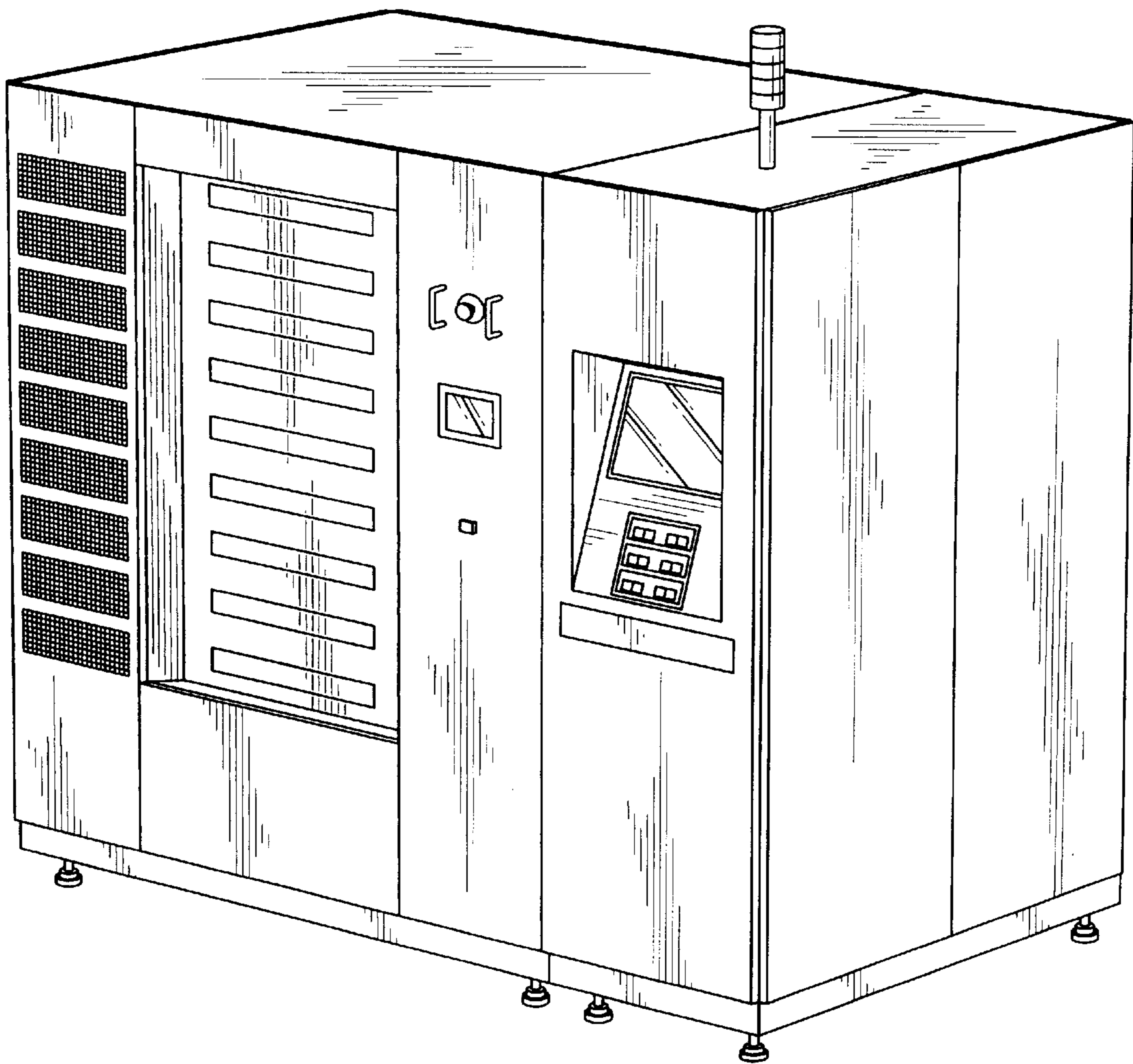


FIG. 2

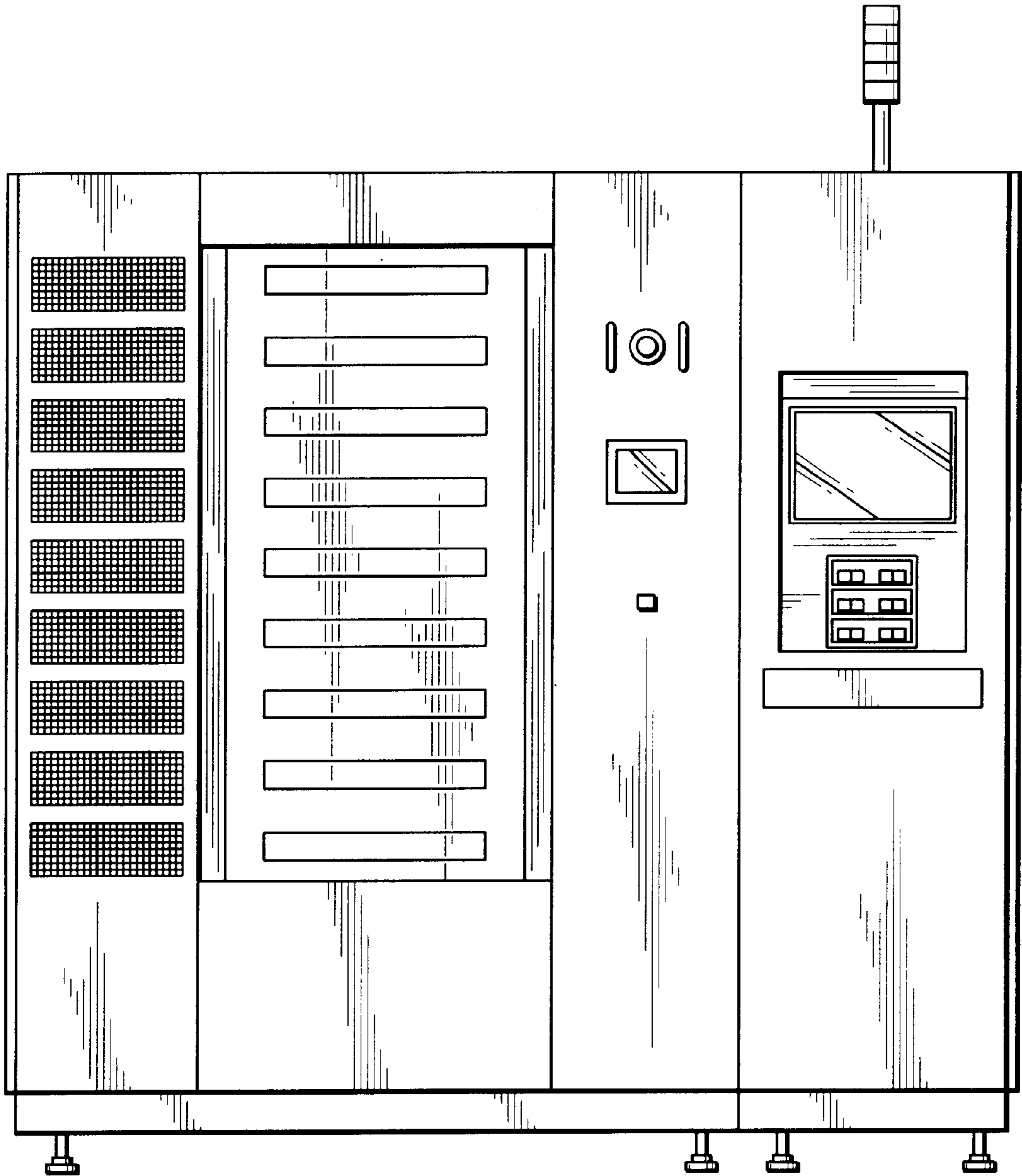


FIG. 3

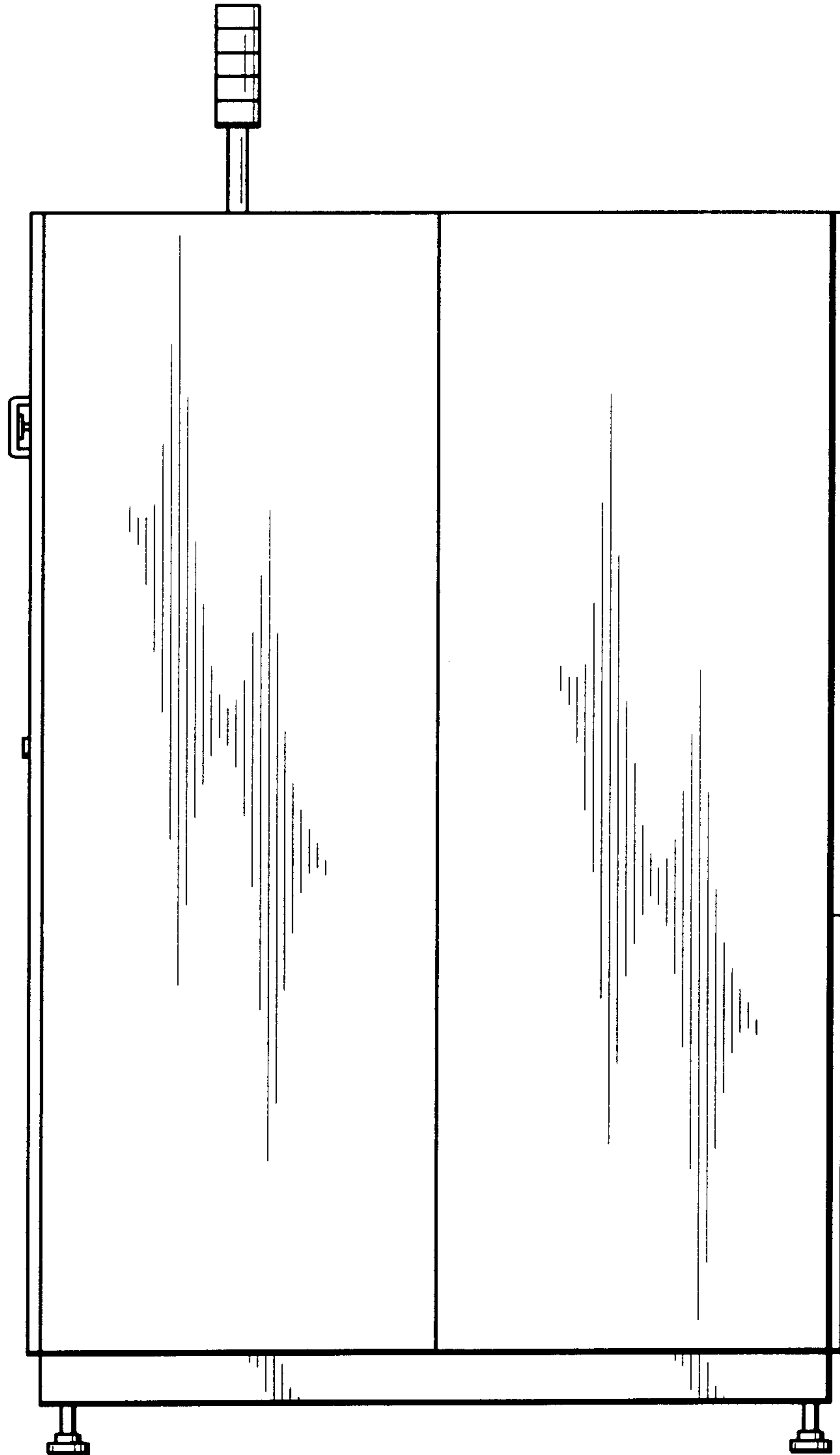


FIG. 4

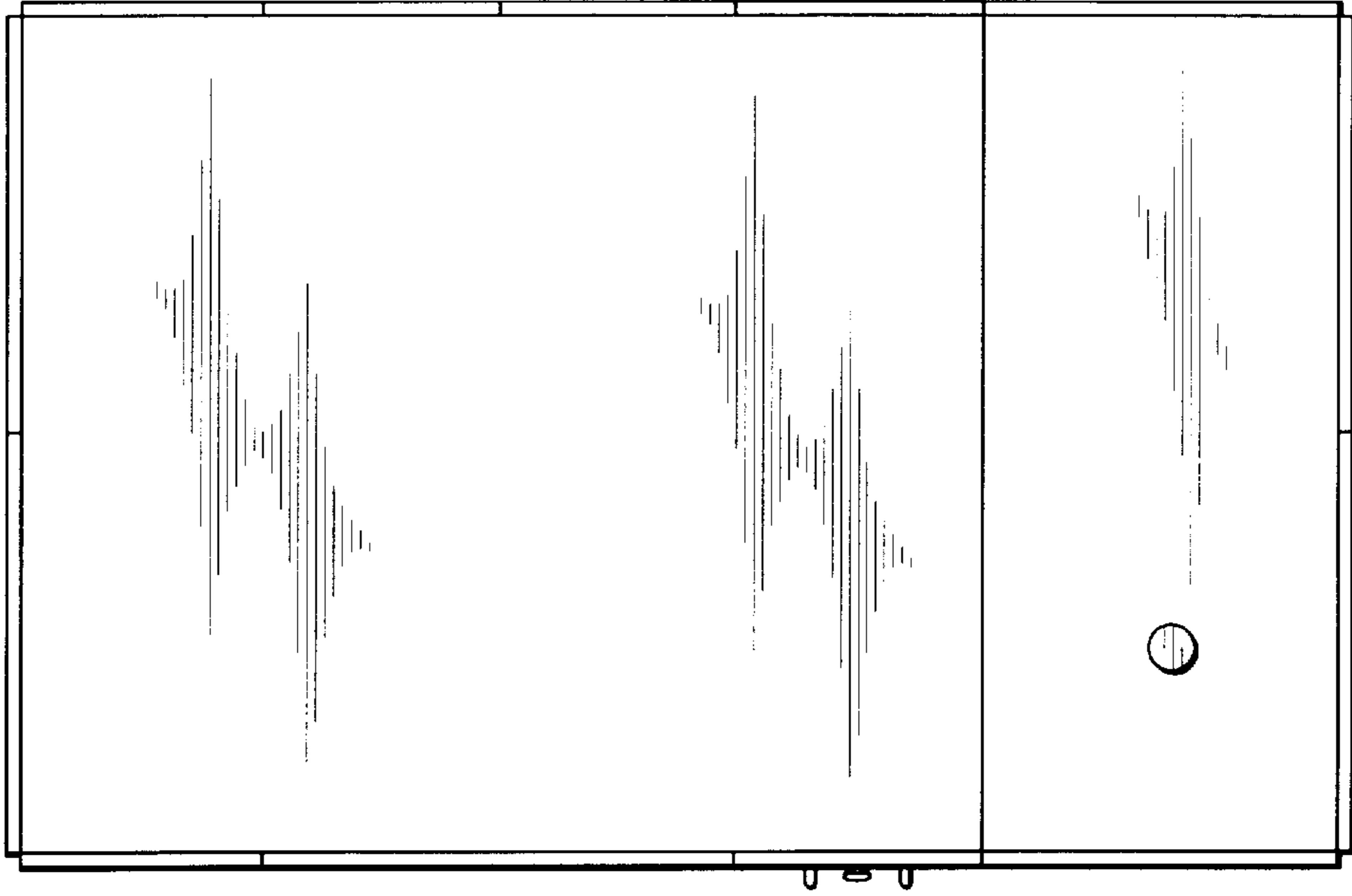


FIG. 5

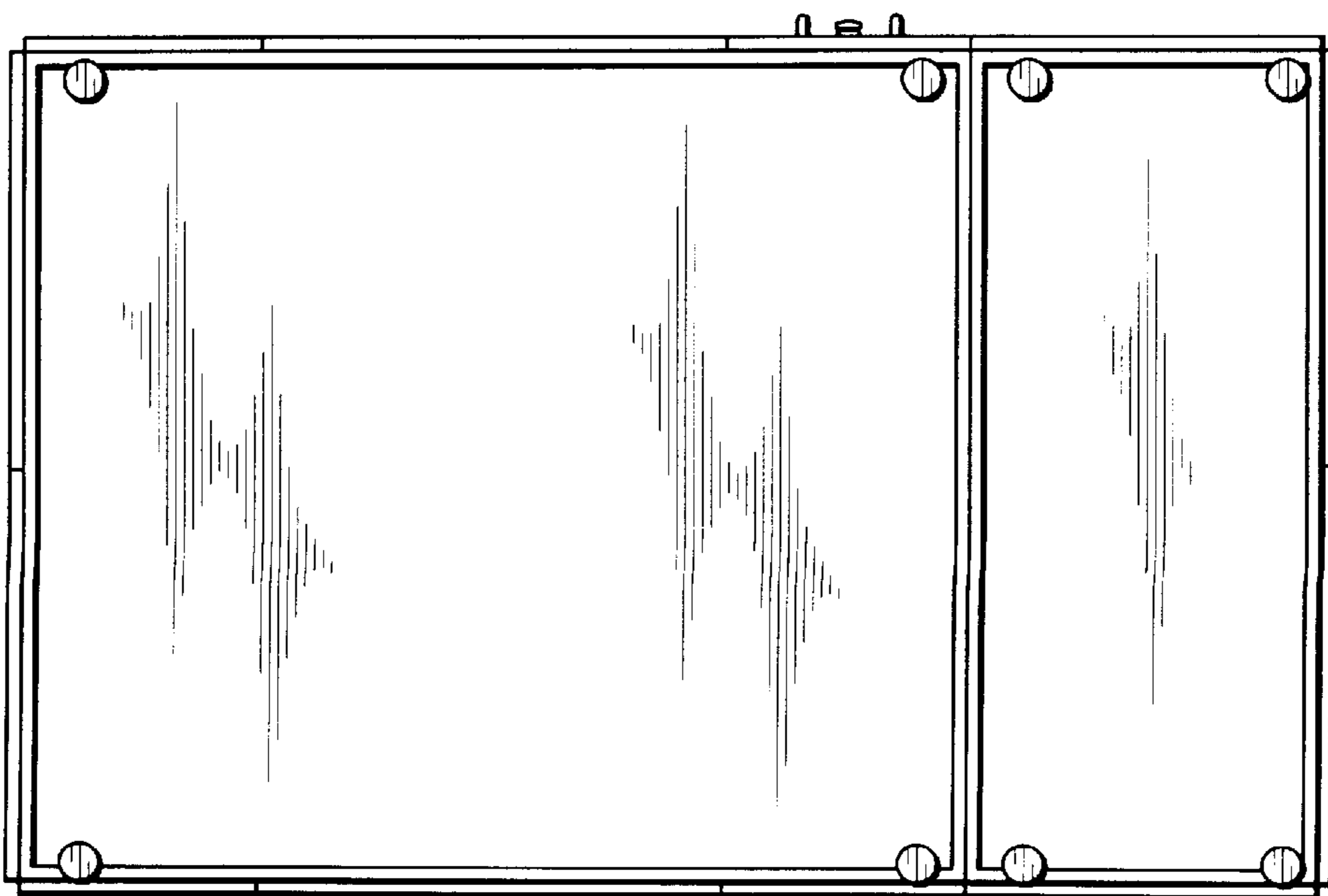


FIG. 6

